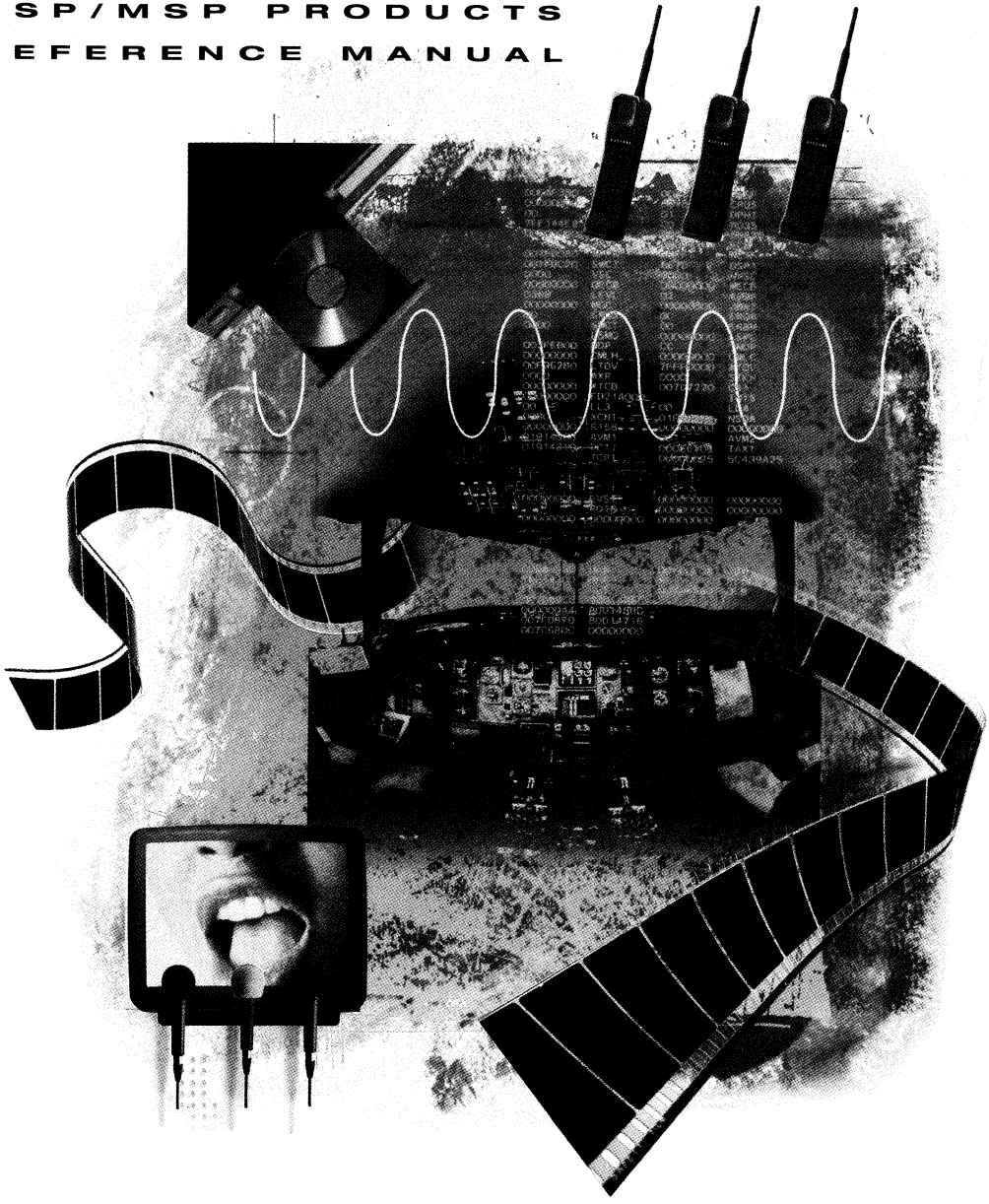
DSP/MSP PRODUCTS
REFERENCE MANUAL



DSP/MSP PROCESSORS • DEVELOPMENT TOOLS •
SOUND PRODUCTS • APPLICATION NOTES

ANALOG DEVICES

How to Find Product Data in This Reference Manual

THIS VOLUME

Contains Data Sheets, Selection Guides and a wealth of background information on state-of-the-art DSP/MSP products that are suitable for new equipment design. This volume is one member of a seven-volume set of reference manuals describing and specifying Special Linear, Amplifier, Converter, Military/Aerospace and DSP/MSP products from Analog Devices, Inc.

IF YOU KNOW THE MODEL NUMBER

Turn to the product index at the back of the book and look up the model number. You will find the Section-Page location of any data sheet in this volume. You will find additional references for all other Analog Devices products currently available.

If you're looking for a form-and-function-compatible version of a product originally brought to market by some other manufacturer (second source), you may find it by adding our "AD" prefix and looking it up in the index. Or call our nearest sales office.

IF YOU DON'T KNOW THE MODEL NUMBER

Find your functional group in the list on the opposite page. Turn directly to the appropriate Section. You will find a functional Selection Guide at the beginning of the Section. The Selection Guide will help you find the products that are the closest to satisfying your need. Use the Selection Guide to compare all products in the category by salient criteria. A comprehensive Table of Contents is provided for your convenience on pages 1–7 and 1–8.

IF YOU CAN'T FIND IT HERE . . . ASK

If you can't find the product you are looking for in this reference manual, please contact your local Analog Devices sales office or phone our Applications Department at 617-937-1428 or 1-800-262-5643 (U.S.A. only).

See the Worldwide Sales Directory on pages 8-16 and 8-17 at the back of this volume for our sales office phone numbers.

DSP BULLETIN BOARD SERVICE

You can obtain the most complete, current version of any preliminary or abridged data sheet included in this volume by calling our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

In addition, Analog Devices offers complete codec support for the Microsoft Windows 3.1, Windows NT, Win95, and the IBM OS/2 environments. SoundPort drivers and demonstration applets that control full duplex capture and playback operation, data formatting, and mixing functions are available on the BBS.

Contents of Other Reference Manuals

DATA CONVERTER REFERENCE MANUAL (VOLUME I)
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- Voltage References

DESIGN-IN REFERENCE MANUAL
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- Sensors & Signal Conditioners
- Signal Compression Components
- Special Function Components

If you don't already own these volumes, you can have them FREE by getting in touch with Analog Devices or the nearest sales office, or phoning 1-800-262-5643.

1995 DSP/MSP PRODUCTS REFERENCE MANUAL

ANALOG DEVICES

1995

DSP/MSP PRODUCTS REFERENCE MANUAL

U.S.A.:
RE29,992, RE30,586, RE31,850, 3,729,660, 3,793,563, 3,803,590, 3,842,412, 3,868,583, 3,890,611, 3,906,486, 3,909,908, 3,932,863, 3,940,760, 3,942,173, 3,946,324, 3,950,603, 3,961,326, 3,978,473, 3,979,688, 4,016,559, 4,020,486, 4,029,974, 4,034,366, 4,054,829, 4,055,773, 4,056,740, 4,068,254, 4,088,905, 4,092,639, 4,092,698, 4,109,215, 4,118,699, 4,123,698, 4,131,884, 4,136,349, 4,138,671, 4,141,004, 4,142,117, 4,168,528, 4,210,830, 4,213,806, 4,228,367, 4,250,445, 4,260,911, 4,268,759, 4,270,118, 4,272,656, 4,285,051, 4,286,225, 4,309,693, 4,313,083, 4,323,795, 4,333,047, 4,338,591, 4,340,851, 4,349,811, 4,363,024, 4,374,314, 4,374,335, 4,383,222, 4,395,647, 4,399,345, 4,400,689, 4,400,690, 4,404,529, 4,427,973, 4,439,724, 4,444,309, 4,449,067, 4,454,413, 4,460,891, 4,471,321, 4,475,103, 4,475,169, 4,476,538, 4,481,708, 4,484,149, 4,485,372, 4,491,825, 4,503,381, 4,511,413, 4,521,764, 4,538,115, 4,542,349, 4,543,560, 4,543,561, 4,547,766, 4,547,961, 4,556,870, 4,558,242, 4,562,400, 4,565,000, 4,572,975, 4,583,051, 4,586,019, 4,586,155, 4,590,456, 4,596,976, 4,601,760, 4,604,532, 4,608,541, 4,622,512, 4,626,769, 4,633,165, 4,639,683, 4,644,253, 4,646,056, 4,646,238, 4,675,561, 4,677,369, 4,678,936, 4,683,423, 4,684,922, 4,685,200, 4,687,984, 4,694,276, 4,697,151, 4,703,283, 4,707,682, 4,709,167, 4,717,883, 4,722,910, 4,739,281, 4,742,331, 4,751,455, 4,752,900, 4,757,274, 4,761,636, 4,769,564, 4,771,011, 4,774,685, 4,791,318, 4,791,551, 4,800,524, 4,804,960, 4,808,908, 4,811,296, 4,814,767, 4,833,345, 4,839,653, 4,855,585, 4,855,618, 4,855,684, 4,857,862, 4,859,944, 4,862,073, 4,864,454, 4,866,505, 4,878,770, 4,879,505, 4,884,075, 4,885,585, 4,888,589, 4,891,533, 4,891,645, 4,899,152, 4,902,959, 4,904,921, 4,924,227, 4,926,178, 4,928,103, 4,928,934, 4,929,909, 4,933,572, 4,940,980, 4,957,583, 4,962,325, 4,969,823, 4,970,470, 4,973,978, 4,978,871, 4,980,634, 4,983,929, 4,985,739, 4,990,797, 4,990,803, 4,990,916, 5,008,671, 5,010,297, 5,010,337, 5,014,056, 5,021,120, 5,026,667, 5,027,085, 5,030,849, 5,036,298, 5,036,322, 5,039,945, 5,041,795, 5,043,295, 5,043,657, 5,043,675, 5,043,732, 5,053,653, 5,055,723, 5,055,843, 5,065,144, 5,065,214, 5,070,331, 5,075,633, 5,075,677, 5,077,494, 5,077,541, 5,084,753, 5,086,370, 5,087,894, 5,087,889, 5,091,701, 5,095,274, 5,097,223, 5,101,126, 5,103,281, 5,111,431, 5,113,362, 5,115,202, 5,119,094, 5,120,990, 5,124,596, 5,124,648, 5,126,586, 5,126,653, 5,132,931, 5,134,401, 5,136,184, 5,141,898, 5,146,181, 5,150,074, 5,159,341, 5,166,637, 5,170,335, 5,175,550, 5,179,293, 5,184,130, 5,192,922, 5,195,827, 5,196,422, 5,196,834, 5,198,785, 5,208,559, 5,210,537, 5,220,206, 5,225,811, 5,227,670, 5,233,309, 5,237,209, 5,243,319, 5,252,908, 5,258,757, 5,262,345, 5,262,934, 5,272,395, 5,283,515, 5,283,554, 5,284,047, 5,285,173, 5,289,113, 5,291,222, 5,295,158, 5,298,811, 5,301,295, 5,302,848, 5,313,165, 5,313,205, 5,314,572, 5,317,199, 5,321,404, 5,323,121, 5,323,122, 5,323,158, 5,326,726, 5,327,030, 5,331,221, 5,339,018, 5,339,021, 5,341,033, 5,341,403, 5,343,196, 5,345,185, 5,345,824, 5,347,224, 5,352,973, 5,353,026

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General Information
Contents

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LEVERAGING NEW TECHNOLOGIES WITH A LEADER

The evolution of Digital Signal Processing (DSP) has resulted in a technical revolution among traditional analog applications. Markets that were once the exclusive domain of analog technologies are being refashioned as digital markets, with products like CDs and Digital Cellular Radios leading the wholesale conversion. In addition, entirely new markets are emerging, encouraging innovative DSP applications in area such as noise cancellation, multimedia systems and many others.

As DSP grows more prevalent, its applications and markets no longer remain the province of specialized analog designers. In fact, today DSP opportunities are open to digital designers everywhere. But only one company is delivering digital signal processing solutions founded on nearly 30 years of real-world signal processing experience—Analog Devices.

ANALOG DEVICES: A SOLUTIONS APPROACH TO SIGNAL PROCESSING

At Analog Devices, Inc. (ADI), our extensive signal processing experience has helped position us as a DSP market leader. More than just an IC component company, Analog Devices focuses on complete signal processing solutions.

Our products encompass the complete range of signal processing operations, from input and conditioning to conversion, processing and signal return. The cornerstone of our development efforts is a history of signal processing advancements. In 1982 ADI introduced the first DSPs in CMOS technology with fixed- and floating-point building blocks, program sequencers, data address generators and register files. In 1986 ADI introduced the first single-chip CMOS DSP, the ADSP-2100. In 1993 ADI introduced the SHARC Super Harvard Architecture Computer—a breakthrough in processor on-chip integration. Our innovations in the area of DSP are simply a natural evolution of our ongoing signal processing leadership—an advantage no microcontroller manufacturer can offer.

We define our digitally integrated approach to analog systems as Signal Computing. Just as today's data computers process vast amounts of diverse integrated information, tomorrow's signal computers will address the synergy of sound, images and other media applications. As a result, signal computers will be as pervasive in the future as embedded microcontrollers and PCs are at present.

DECREASED DEVELOPMENT TIME, INCREASED COST EFFICIENCY

At Analog Device, we ensure that all our products are backed by broad scale, high quality support. We offer innovative hardware and software tools and applications assistance to accelerate development cycles. What's more, our worldclass manufacturing capabilities ensure excellent reliability and service.

Best of all, we're dedicated to a strong, customer oriented approach, extending the limits of technology with every application.

DIGITAL SIGNAL PROCESSORS: THE FUTURE

As the signal processing market continues to evolve into areas such as communications, computer, and imaging, ADI will address your applications requirements for an increasing variety of Fixed-Point, Floating-Point, and Mixed-Signal Processors.

For the higher volume fixed-point market, you can expect faster, larger memory products to handle increasingly complex algorithms, as well as lower cost, ROM-based products for more cost sensitive applications. For battery powered, portable applications, low power or 3.0 V parts are available. In the performance driven floating-point market, increased levels of processor performance, as well as memory and digital peripheral integration, is available though our SHARCs—Super Harvard Architecture Computer products. Designed to drive the next generation of DSP products, the SHARCs are the first complete signal processing system on one chip.

THE ADSP-2100 AND ADSP-21000 FAMILIES: INHERENT DSP STRENGTHS

The foundation of any signal processing system is the architecture of its processor. The more efficient the processor's design, the more successful the system's operation. Analog Devices offers two digital signal processor families: the 16-bit fixed-point ADSP-2100 Family and the 32-bit floating-point ADSP-21000 Family.

The processors of each family are compatible in both their core architectures and code, providing vital investment protection. Preexisting code remains usable, even as you grow into processors with different memory configurations, greater performance, or new on-chip peripherals. In fact, software development can be totally independent of the system's final hardware design.

Available in a range of performance levels, the ADSP-2100 and ADSP-21000 Families provide the five key capabilities by which all leading-edge signal processing architectures are defined:

Parallel Computation Units for Flexible Numeric Processing
To simplify programming and maximize computational efficiency, Analog Devices' DSP processors provide three parallel computational units—an Arithmetic Logic Unit (ALU), Multiplier-Accumulator (MAC), and Barrel Shifter. Consequently, complex computations may be performed in any order, with the output of one unit being directly input to any other. This not only provides programming flexibility, but also eliminates the wasted cycles of register-to-register data transfers.

Furthermore, Analog Devices processors are adept at handling complex algorithms and high-level programming languages. Our ADSP-21000 Family features a general purpose 9-port register file, while our ADSP-2100 Family provides separate input and output registers for all arithmetic units. Additionally, the computation units feature a complete set of alternate background registers that provide a single-cycle context switch to quickly service interrupts or subroutines.

Extended Dynamic Range for Overflow Protection
Numerically intensive applications require extended dynamic range. Protection against overflow in successive computations ensures that no loss of data occurs. Our DSP processors supply extended dynamic range within the computational units to minimize scaling, truncation, and clipping. The dynamic range is provided by a 40-bit accumulator in our fixed-point processors and an 80-bit accumulator in the floating-point processors.

Unconstrained Data Flow for Dual Operand Fetch
In order to maximize the power and flexibility of any processor's arithmetic units, data must be supplied to each unit as quickly as possible. On Analog Devices' DSP processors, it is. Our Harvard architecture maintains the flow of single-cycle arithmetic operations through three-bus performance, allowing instruction fetch and access of two data operands per cycle, an absolute requirement for the arithmetically-intensive calculations found in digital signal processing algorithms.

Powerful Data Address Generators for Hardware Circular Buffers
Many classes of DSP algorithms, including filters and FFTs, require complex manipulation of data—data most easily managed in circular arrays. Analog Devices' DSP processors simplify this type of data manipulation with two independent data address generators that provide hardware-based circular buffers. Using this capability, eight circular data buffers can be simultaneously maintained on ADSP-2100 Family processors, and sixteen on the ADSP-21000 Family processors.

Program Sequencing for Efficient Looping and Branching
Because repetitive DSP algorithms are best expressed as program loops, the processors' program sequencers support looped code with zero overhead. Single-cycle conditional arithmetic instructions are provided on all processors, as well as 4 (ADSP-2100) and 6 (ADSP-21000) levels of nested loops. This provides maximum execution efficiency, resulting in optimum performance, more efficient management of interrupts, simplified program implementation, and smaller memory requirements.

ALGEBRAIC INSTRUCTION SYNTAX

To help you develop applications and take advantage of the strengths of our base architecture, ADI offers two easy to use algebraic assembly languages. Each is easy to read, debug and maintain, and is common to all members of each processor family. For example, the algebraic R = X × Y codes as MR = MXO × MYO in our Fixed-Point Family and as F1 = F2 × F3 in our Floating-Point Family.

FFT: MEASURING SIGNAL PROCESSING PERFORMANCE

Over the past several years, the Fast Fourier Transform (FFT) has become the benchmark of choice for measuring signal processor performance. The FFT extends beyond simple cycle rate performance indicators to measure a processor's architectural efficiency. In doing so, the FFT exercises all of the key architectural requirements necessary for general purpose signal processing: fast, flexible arithmetic, two powerful address generators, extended arithmetic precision, an efficient program sequencer, and unconstrained data flow of operands. As the table below illustrates, ADI signal processors provide performance superiority, outdistancing competitive products by a considerable margin.

Table I. 1024-Point Complex FFT (In Place)

	Instruction Rate	Instruction Cycle Time	Number of Cycles	Total FFT Time
16-Bit Fixed-Point DSPs				
TMS320C25	12.5 MHz	80 ns	113,467	9.08 ms
ADSP-2105	13.8 MHz	72 ns	34,625	2.50 ms
TMS320C50	40 MHz	25 ns	84,833	2.12 ms
ADSP-2101	20 MHz	50 ns	34,625	1.73 ms
ADSP-2115	20 MHz	50 ns	34,625	1.73 ms
ADSP-2171	33 MHz	30 ns	34,625	1.04 ms
ADSP-2181	33 MHz	30 ns	34,625	1.04 ms
32-Bit Floating-Point DSPs				
TMS320C30	20 MHz	50 ns	60,800	3.04 ms
TMS320C40	40 MHz	25 ns	38,945	0.97 ms
ADSP-21020	33 MHz	30 ns	19,245	0.58 ms
ADSP-21060 SHARC	40 MHz	25 ns	18,221	0.46 ms

Source: Texas Instruments TMS320 Family User's Guides and Data Sheets.

THE ADSP-2100 FIXED-POINT PROCESSOR FAMILY

The processors in our ADSP-2100 Fixed-Point Family all utilize the same base architecture. Providing a highly efficient signal processing engine, this 16-bit, code compatible architecture consists of an ALU, MAC, Barrel Shifter, two Address Generators and a Program Sequencer, all interconnected via a Harvard bus structure.

While ensuring the most efficient implementation of complex DSP algorithms, our ADSP-2100 Family also provides the benefits of efficient power consumption, increased performance and lower system costs. And, like all our processors, the ADSP-2100 Family is supported by a host of tools that rank among the best in the industry.

Table II. ADSP-2100 Family Performance Benchmarks

	ADSP-2101 ADSP-2115 ADSP-2111	ADSP-2171 ADSP-2181
Clock Speed (MIPS)	20 MHz	33.3 MHz
Instruction Cycle Time	50 ns	30 ns
FIR Filter	50 ns per Tap	30 ns per Tap
Complex FIR Filter	200 ns per Tap	120 ns per Tap
IIR Biquad Filter Section	350 ns per Section	210 ns per Section
Lattice Filter Section	250 ns per Section	150 ns per Section
256-Point Complex FFT 1024-Point Complex FFT	0.37 ms 1.73 ms	0.22 ms 1.04 ms
256-Tap LMS Adaptive Filter Coefficient Update	25.8 µs	15.5 µs
10th Order LPC Analysis (240-Point Rectangular Window)	0.23 ms	0.14 ms
ADPCM-Full Transcode (CCITT G.721, ANSI T1.301-1987)	44.6 µs	26.8 µs
GSM Speech Coding	3.29 ms (16% Loading)	1.98 ms (10% Loading)
RPE-LTP LTC Encoder	2.47 ms (12% Loading)	1.48 ms (8% Loading)
RPE-LTP LTC Decoder	0.72 ms (3.6% Loading)	0.43 ms (2.2% Loading)
Voice Activity Detector	0.11 ms (0.5% Loading)	0.07 ms (0.4% Loading)

Table III. ADSP-21000 Family Performance Benchmarks

	ADSP-21020	ADSP-21060 SHARC ADSP-21062 SHARC
Clock Speed	33.3 MHz	40 MHz
Instruction Cycle Time	30 ns	25 ns
MFLOPS Sustained	66.6 MFLOPS	80 MFLOPS
MFLOPS Peak	100 MFLOPS	120 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	0.58 ms	0.46 ms
FIR Filter (per Tap)	30 ns	25 ns
IIR Filter (per Biquad)	120 ns	100 ns
Matrix Multiply (Pipelined) (3×3) × (3×1) (4×4) × (4×1)	 270 ns 480 ns	 225 ns 400 ns
Divide (y/x)	180 ns	150 ns
Inverse Square Root ($1/\sqrt{x}$)	270 ns	225 ns
Whetstones/ms (C Compiler)	44,245	53,094
Drystones/s (C Compiler)	68,411	82,987

THE ADSP-21000 FLOATING-POINT PROCESSOR FAMILY

The ADSP-21000 Family extends upon our sophisticated ADSP-2100 Family, enhancing the strengths of our DSP architecture including fast, flexible, arithmetic; extended precision, free flow of data; data address generation; and program sequencing.

The technological foundation of all members of the ADSP-21000 Family, the powerful Harvard architecture handles 32-bit IEEE floating-point, 40-bit IEEE floating-point (with 32-bit mantissa and 8-bit exponent), and 32-bit fixed-point data formats.

ANALOG DEVICES' SIGNAL PROCESSING ARCHITECTURE

Analog Devices' DSP architecture is designed to satisfy the key requirements of signal processing. The processor core consists of three computational units: an ALU, multiplier-accumulator, and barrel shifter for fast, flexible arithmetic; two data address generators for single-cycle dual operand fetches; and a sophisticated program sequencer for efficient program execution. An on-chip Harvard architecture connects all of these functional units.

A traditional Harvard architecture uses two independent buses to provide both a program instruction and a data operand on each cycle. Analog Devices' implementation of the Harvard architecture enables three-bus performance, with an instruction fetch and two data accesses per cycle. In our DSP microcomputers, i.e., those containing on-chip memory, the on-chip program memory can be accessed twice per cycle, once for the instruction fetch and once for a data operand. The data memory is separately accessed in each cycle for a second data operand.

Programming in assembly language is simplified by the logical, algebraic syntax of the processor instruction sets. A multiply-accumulate instruction of the form $r = r + x \times y$, for example, is coded as

$$MR = MR + MX0 \times MY0$$

in the ADSP-2100 Family assembly language. Both the fixed-point and floating-point instruction sets are easy to read, debug, and maintain, while providing powerful multifunction instructions and simple, concise branching constructs. Both instruction sets are common to all processors of the family.

ADVANCED FEATURES FOR SYSTEM OPTIMIZATION

Analog Devices' DSP processors offer a range of feature integration levels, affording the flexibility to meet a variety of design and cost requirements.

On-Chip Memory

A wide range of on-chip memory options is available on both the fixed-point and floating-point DSP microcomputers. Several of the processors include large on-chip SRAMs for instruction and data storage, allowing single-chip systems with no external memories. Most notable among these products are the ADSP-21060 and ADSP-21062 SHARC—Super Harvard Architecture Computers—that contain an astounding 4 megabits and 2 megabits, respectively, of integrated SRAM. The memory can be configured as any combination of program and data memory, providing a maximum of 128K words of 32-bit data storage and 80K words of 48-bit program storage on the ADSP-21060. In the fixed-point ADSP-2100 Family, the ADSP-2181 offers the largest on-chip memory, with 16K each of program and data memory.

One advantage of on-chip RAM is its ability to be boot loaded from external EPROM; this allows easy revising of code and low production *costs* without committing to the large production runs necessary for ROM masking. EPROM booting also allows dynamic loading and reconfiguration during system operation. Custom ROM solutions are offered by the ADSP-216x fixed-point processors.

Serial Ports

The high-performance serial ports (SPORTs) are bidirectional, double-buffered I/O interfaces that feature user-configurable clocking, framing, and word length. The SPORTs also include μ-law and A-law companding circuitry and automatic data buffering to and from internal memory. The SPORTs' flexible features dramatically reduce the number of cycles associated with managing serial data transfers, minimizing overhead while maximizing computation speed. One of serial ports also supports a T1-style multichannel capability.

Host Interface Port

System costs associated with parallel I/O may also be minimized with the use of the Host Interface Port (HIP) featured on many of our DSPs. The HIP serves as an asynchronous interface between the DSP and host processor, allowing the host to use the DSP as a powerful coprocessor for real-time signals such as speech and digital audio. User-configurable as either an 8- or 16-bit interface, the HIP provides simple, direct access to most popular microprocessors and microcontrollers.

Power-Up Boot

Many of our processors support two methods of power-up boot—through the external memory interface, from a single, byte-wide EPROM, or through the Host Interface Port. This dual booting capability minimizes component count and helps reduce system costs.

Timer

A programmable interval timer allows for a wide range of periodic interrupt options.

Efficient Power Consumption

Analog Devices' DSP processors meet today's growing requirement for power conservation in several ways: with integrated functions like processor idle and power-down which dramatically reduce power consumption from normal operation levels, with the efficient execution of DSP algorithms provided by our core architecture, and with 3-volt versions of our processors used in battery-powered applications.

Analog I/O for Mixed-Signal Processors

Building on our reputation as the world's leading supplier of signal conversion components, Analog Devices offers high performance analog I/O peripherals that are available both as individual components and integrated onto a DSP. We call these products Mixed-Signal Peripherals (MSPeripherals™) and Mixed-Signal Processors (MSProcessors®).

The ADSP-21msp55, for example, integrates a 16-bit sigma-delta ADC and DAC onto the ADSP-2100 Family DSP core to form a complete voice processing system on a chip. This revolutionary integration of analog and digital functionality on a single device is achieved through our proprietary ALLCMOS process.

TECHNICAL SUPPORT

Our extensive technical literature discusses the technology and applications of products for real-world signal processing. Besides tutorial material and comprehensive data sheets, including a large number in our reference manuals, we offer application notes, application guides, technical handbooks (at reasonable prices), and several free serial publications. For example, *Analog Briefings*® provides current information about products for military/avionics, and *Analog Dialogue*, our technical magazine, provides in-depth discussions of new developments in analog and digital circuit technology as applied to data acquisition, signal processing, control, and test. *DSPatch*® is a quarterly newsletter that brings its readers up-to-date applications information on our DSP products and the general field of digital signal processing. We maintain a mailing list of engineers, scientists, and technicians with a serious interest in our products. In addition to these reference manual catalogs—and general short-form selection guides—we also publish several short-form catalogs on specific product families. You will find typical publications described on pages 8–16 to 8–17 at the back of the book.

ADI COMPUTER PRODUCTS CUSTOMER SUPPORT

For factory and marketing support on DSP, Signal Computing, and Computer Products:
Phone: (617) 461-3881
Fax: (617) 461-3010
email: cpd_support@analog.com

ADI CUSTOMER SERVICE/SALES

For general product availability, pricing, and order placement:
Phone: (617) 461-3000
Toll Free: 1-800-ANALOG-5
In California: (714) 641-9391

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THE ADSP-2100 FAMILY: 16-BIT FIXED-POINT DSPS

All *processors* of our ADSP-2100 Fixed-Point Family are based on a common core architecture. Providing a highly efficient signal processing engine, this architecture consists of an ALU, Multiplier/Accumulator, Barrel Shifter, two Data Address Generators and a Program Sequencer, all connected by a Harvard bus structure. Various processors of the family add differentiating *features such as* on-chip program and data memory, a programmable timer, serial ports, host interface port, and analog signal conversion.

While ensuring the most efficient implementation of complex DSP algorithms, our ADSP-2100 Family also provides the benefits of low power consumption, high-speed performance, and reduced system component costs. And, like all our DSP processors, the ADSP-2100 Family is supported by a set of development tools that rank among the best in the industry.

ADSP-2101

The ADSP-2101 builds upon benefits of the ADSP-2100 core architecture, adding integrated SRAM memory, boot loading hardware, two serial I/O ports, and a programmable interval timer. The on-chip SRAM consists of 2K × 24-bit program memory and 1K × 16-bit data memory. In addition, the processor's serial ports feature μ-law and A-law companding circuitry, automatic data buffering, and a multichannel interface. While the ADSP-2101 allows programs to be stored on-chip and booted from a single, low-cost EPROM, an even lower system chip count is available with the use of the ADSP-2161 or ADSP-2163 custom ROM-programmed DSPs.

Application Examples: *Cellular telephone base stations, modems, medical ultrasound, voice mail systems*

ADSP-2105

The ADSP-2105 is the lowest-cost member of the ADSP-2100 Family. It provides an economical entry point to digital signal processing, allowing even the most cost-sensitive applications to take advantage of state-of-the-art DSP technology. The ADSP-2105 adds 1K × 24-bit on-chip program memory, 512 × 16-bit data memory, and a single serial port to the core architecture and computation units. Like the ADSP-2101, it also includes boot loading hardware and an on-chip timer. The ADSP-2105 offers code and pin-compatibility for a simple upgrade path to higher performance and functionality, making the processor an ideal choice for both high and low volume consumer applications.

Application Examples: *Audio compression, power line monitoring, nondestructive testing, acoustic echo cancellation, theft detection*

ADSP-2115

The ADSP-2115 offers yet another price/feature/performance combination within the ADSP-2100 Family, providing the same amount of on-chip memory as the ADSP-2105 but with the two serial ports of the ADSP-2101. In addition, the ADSP-2115 can run at the fastest operating speed of the processor family, like the ADSP-2101. Code and pin-compatibility is again maintained, and systems may be easily migrated from the ADSP-2105 to ADSP-2115 to ADSP-2101 or higher, providing ever-increasing levels of feature integration and performance.

Application Examples: *PC-based digital audio systems and software-configurable modems, wavetable music synthesis, digital tapeless answering machines*

ADSP-2103

The ADSP-2103 is a 3.3-volt version of the ADSP-2101. Ideal for use in portable, battery-powered equipment or in any system requiring absolute minimum power consumption, the ADSP-2103 is leading the use of DSPs into personal communications applications. The ADSP-2162 and ADSP-2164 are custom ROM-programmed versions of the 3.3-volt ADSP-2103. Three-volt versions of other fixed- and floating-point processors will also be offered in the future.

Application Examples: *Cordless and cellular telephones, laptop and notebook computers*

ADSP-2111

The ADSP-2111 adds a parallel host processor port to the integrated feature set of the ADSP-2101. The Host Interface Port (HIP) provides user-programmable I/O modes and allows the host processor to boot the ADSP-2111 through the HIP instead of from EPROM. Designed for efficient interprocessor communication, the ADSP-2111 can directly interface to industry-standard microprocessors and microcontrollers.

Application Examples: *Cellular telephones, voice processing and speech recognition in host computers*

ADSP-2171

The newest and fastest member of the ADSP-2100 Family, the ADSP-2171 includes all of the features of the ADSP-2111—host interface port, two serial ports, and timer—plus additional on-chip memory, powerdown mode, and instruction set extensions for bit manipulation, multiplication, biased rounding, and global interrupt masking. With its 33 MIPS, 30 ns instruction cycle performance, the ADSP-2171 allows the use of fixed-point DSP in applications previously requiring more costly solutions.

The ADSP-2171 contains 2K words of program memory RAM, 2K words of data memory RAM, and an optional 8K words of program memory ROM. The processor's powerdown mode, designed to meet the needs of low-power battery-operated equipment, features 0.5 mW power dissipation with a hundred cycle recovery time. The biased rounding capability simplifies coding of bit-specified algorithms such as GSM digital cellular speech compression.

Application Examples: *Speech compression, echo cancellation, digital cellular telephones, call processing systems*

ADSP-2181

The ADSP-2181 further extends the capabilities and feature set of the ADSP-2100 Family. This 33 MIPS processor integrates the largest amount of memory available on a fixed-point DSP, with 80K bytes of on-chip RAM configured as 16K words of program memory and 16K words of data memory. The large on-chip RAM allows the ADSP-2181 to operate without external memory, reducing system cost.

For efficient access to the on-chip memory, the ADSP-2181 includes two parallel DMA ports. The Internal DMA port (IDMA) provides a high-speed 16-bit interface for transferring data to and from system buses or host processors. The IDMA port simplifies communications between the DSP and bus interface ASICs such as those found in ISA-bus PCs. The 8-bit wide Byte DMA port (BDMA) provides a direct, low overhead interface to low cost memories for external storage of large data tables and program overlays.

Features

1. Clock Speed (MIPS)
2. Instruction Cycle Time (ns)
3. Data Memory RAM (1 Bit)
4. Program Memory RAM (24 Bit)
5. Program Memory ROM (24 Bit)
6. Programmable Time
7. Serial Ports
8. Host Interface Port
9. Internal DMA Port & Byte DMA Port
10. Analog Interface (ADC, DAC)
11. Powerdown Mode
12. Package Types–PQFP, TQFP, PGA, PLCC

MIXED-SIGNAL DSP PROCESSORS

ADSP-21msp55

The ADSP-21msp55 is a completely integrated voiceband processing system on a single device. It incorporates all the features of the ADSP-2111 plus an analog signal interface and hardware powerdown function. The analog interface consists of a 16-bit Sigma Delta ADC and DAC, antialiasing and anti-imaging filters, and programmable gain stages for both input and output. (This voiceband codec is also available as a separate peripheral component, the AD28msp02—one of our many signal conversion devices designed for use with DSP processors.)

Application Examples: *Digital cellular telephones, cordless telephones, voice mail systems*

ADSP-21msp56

Augmenting the capabilities of the ADSP-21msp55, the ADSP-21msp56 adds an additional 2K of on-chip program memory ROM. This allows complex functions requiring larger amounts of code storage to be implemented on a single chip. The ADSP-21msp56 is used in digital cellular telephones, for example, to handle not only voice processing functions but also noise cancellation and speech recognition algorithms for hands-free dialing and operation.

Table I. ADSP-2100 Family DSP Processors—Key Features

	1	2	3	4	5	6	7	8	9	10	11	12
ADSP-2100A	12.5	80	—	—	—	—	—	—	—	—	—	PGA, PQFP
ADSP-2101	20	50	1K	2K	—	•	2	—	—	—	—	PGA, PQFP, PLCC
ADSP-2103 (3.3 V)	10.24	98	1K	2K	—	•	2	—	—	—	—	PQFP, PLCC
ADSP-2105	13.8	72	512	1K	—	•	1	—	—	—	—	PLCC
ADSP-2115	20	50	512	1K	—	•	2	•	—	—	—	PQFP, PLCC, TQFP
ADSP-216x	16.7	60	512	—	4K/8K	•	2	—	—	—	—	PQFP, PLCC
ADSP-2171	33	30	2K	2K	8K	•	2	•	—	—	•	PQFP, TQFP
ADSP-2181	33	30	16K	16K	—	•	2	—	•	—	•	PQFP, TQFP
ADSP-21msp55A	13	77	1K	2K	—	•	2	•	—	•	•	PGA, PQFP
ADSP-21msp56A	13	38	1K	2K	4K	•	2	•	—	•	•	PGA, PQFP

VOICE PROCESSING APPLICATIONS: ADVANCEMENTS WORTH TALKING ABOUT

One of the key application areas for mixed-signal technologies is voiceband processing. Here, the ADSP-21msp50 series of Mixed-Signal DSP Processors leads the industry in integration and performance.

Although known primarily for its impact in the digital cellular telephone business, the ADSP-21msp50 series is also being used in other voice processing applications including voice mail systems, digital answering machines, and cordless telephones.

Adaptable to high volume, consumer applications, these unique devices have enough processing power and on-chip memory to perform a wide range of complex tasks. Take, for example, the processor's role in European GSM standard digital cellular telephones. Because the 26 MIPS ADSP-21msp59 requires only 12.5% processor loading for GSM voice coding, its remaining cycles are available to implement other functions such as hands-free operation while still taking advantage of the processor's powerdown mode to preserve battery life.

Furthermore, the processor's programmability allows the use of numerous speech compression algorithms including G.721 ADPCM, G.728 LD-CELP, TIA IS-54 VSELP, and GSM RPE-LTP LPC. Many of these algorithms are available from Analog Devices' third party developers.

THE ADSP-21000 FAMILY: 32-BIT FLOATING-POINT DSPS

The ADSP-21000 Family further extends the signal processing architecture of the fixed-point ADSP-2100 Family, building on its strengths to offer:

Fast, Flexible Arithmetic

The most complete set of arithmetic operations available, including y/x, $1/\sqrt{x}$, *min*, *max*, and *rotate*. The 48-bit instruction word accommodates a variety of parallel operations, for concise programming either in native assembly language or with C source code using the GNU C compiler.

Extended Precision

32- and 40-bit floating-point formats are handled by all computation units, with the processors' 32-bit fixed-point format supported by dual 80-bit accumulators.

Free Flow of Data

A 9-port general purpose register file transfers up to 9 data operands to and from the computation units and memory.

Data Address Generation

Two independent data address generators that provide immediate or indirect addressing, and support modulus and bit-reverse addressing operations.

Program Sequencing

The program sequencer unit supports zero-overhead looping, single-cycle setup and exit for multiple loops (nestable and interruptible), and delayed or nondelayed branches.

Features

1. Clock Speed (MIPS)
2. Instruction Cycle Time (ns)
3. Total On-Chip Memory (RAM)
4. Maximum On-Chip Data Memory (32 Bit)
5. Maximum On-Chip Program Memory (48 Bit)
6. Programmable Timer
7. Serial Ports
8. Host Interface Port
9. DMA Controller
10. Multiprocessing
11. JTAG Test & On-Chip Emulation
12. Package Types

ADSP-21020

The ADSP-21020 offers a traditional off-chip Harvard Architecture combined with the high performance 32-bit floating-point core of the ADSP-21000 Family. The processor's Harvard busing structure, together with the its on-chip instruction cache and data register file, allows two external memory transfers to occur in parallel with the instruction fetch and computation, all in a single cycle. The two-way, set-associative instruction cache enable three bus operation for accessing an instruction plus two data values. The cache is selective—only instructions whose fetches conflict with program memory data accesses are cached, allowing the processor to simultaneously access data in both program memory and data memory.

Table II. ADSP-21000 Family DSP Processors—Key Features

	1	2	3	4	5	6	7	8	9	10	11	12
ADSP-21020	33	30	–	–	–	•	–	–	–	–	•	PGA
ADSP-21060 SHARC	40	25	4 Mbit	128K	80K	•	•	•	•	•	•	PQFP
ADSP-21062 SHARC	40	25	2 Mbit	64K	•	•	•	•	•	•	•	PQFP

The ADSP-21020's independent, parallel computation units—ALU, multiplier, and shifter—perform single-cycle operations with no pipelining. A single multifunction instruction uses the ALU and multiplier to execute multiply/accumulate operations. The computation units can process data in any of three different formats: 32-bit IEEE floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point. The 32-bit floating-point format is the standard IEEE format, while the 40-bit format adds eight LSBs of mantissa for additional accuracy.

Like all ADSP-21000 Family processors, the ADSP-21020 includes a JTAG test access port and on-chip emulation support. The serial JTAG port enables boundary scan testing of circuitry connected to the ADSP-21020's I/O pins. The JTAG port is also used by our EZ-ICE emulator to provide nonintrusive, in-circuit emulation.

Application Examples: *Medical imaging, precision instrumentation, 3-D graphics*

ADSP-21060 SHARC

The ADSP-21060 SHARC—Super Harvard Architecture Computer—is a complete signal processing system on a chip. This device offers the absolute highest performance available in a DSP by adding integrated on-chip memory, I/O peripherals, and multiprocessing features to the ADSP-21000 Family computational core. The ADSP-21060 (and ADSP-21062) provide superior DSP functionality for processing of high-fidelity audio, speech, image, and full-motion video signals.

The ADSP-21060 SHARC has a fast 25 ns instruction cycle time operating at 40 MIPS. Peak performance levels approach 120 MFLOPS, with 80 MFLOPS of sustained performance. Integrated features of the ADSP-21060 include:

- 32-bit Floating-Point DSP Core
- Super Harvard Architecture—Four Independent Buses for Dual Data, Instructions, and I/O
- 4 Megabit SRAM—Configurable as 128K Words Data Memory (32 Bit), 80K Words Program Memory (48 Bit), or Combinations of Both
- DMA Controller—10 Channels
- Host Processor Interface
- Two Serial Ports
- Six Link Ports for Interprocessor Communications and Array Multiprocessing
- Scalable Multiprocessing—Distributed On-Chip Bus Arbitration for Glueless Connection of Up to Six Processors

The processor contains an astounding 4 megabits of on-chip SRAM—the largest amount of memory integrated on any single microcomputer! This allows the ADSP-21060 to store entire applications and associated data internally, reducing system component count, cost, and power dissipation. The memory is arranged in two blocks, each dual-ported for independent access by the processor core and the on-chip DMA controller. All of the I/O peripherals are supported by a dedicated on-chip I/O bus that eliminates bottlenecks and greatly increases the bandwidth of data transfers.

The ADSP-21060's integrated I/O controller conducts data transfers over the link ports and serial ports, simultaneously and independently from the DSP processor core. The nibble-wide link ports provide interprocessor communications and high-speed, point-to-point DMA transfers with neighboring processors. With four link ports operating simultaneously, maximum throughput is 240 megabytes per second.

The processor's external port provides the interface to additional, multiprocessing ADSP-21060s and to a system bus or host processor. The internal memory of each DSP can be directly read and written by either the host or by any other ADSP-21060. This distributed memory simplifies the software communication model of multiprocessing systems.

Application Examples: *Full-motion video, wireless digital networks, radar systems, speech recognition, satellite communications*

ADSP-21062 SHARC

The ADSP-21062 is a reduced-memory version of the ADSP-21060 SHARC, containing a total of 2 megabits of on-chip SRAM. With an outstanding price/performance ratio, the ADSP-21062 is the ideal solution for demanding but cost-sensitive DSP applications.

Both the ADSP-21062 and ADSP-21060 offer two to four times the performance of any other DSP. They provide increased I/O bandwidth, supplying data to the computational core as rapidly as it can process it. The processors' integrated features allow designers to build powerful real-time signal processing systems with a minimum number of components. This simplified system design increases reliability, reduces time-to-market, and maximizes performance per square inch.

Application Examples: *Professional audio, digital cellular base stations, color fax machines, video telephony, digital cable television, text-to-speech and speech-to-text*

Table III. ADSP-21000 Family Performance Benchmarks

	ADSP-21020	ADSP-21060 SHARC ADSP-21062 SHARC
Clock Speed	33.3 MHz	40 MHz
Instruction Cycle Time	30 ns	25 ns
MFLOPS Sustained	66.6 MFLOPS	80 MFLOPS
MFLOPS Peak	100 MFLOPS	120 MFLOPS
1024-Point Complex FFT (Radix 4, with Digit Reverse)	0.58 ms	0.46 ms
FIR Filter (per Tap)	30 ns	25 ns
IIR Filter (per Biquad)	120 ns	100 ns
Matrix Multiply (Pipelined)		
[3 × 3] × [3 × 1]	270 ns	225 ns
[4 × 4] × [4 × 1]	480 ns	400 ns
Divide (y/x)	180 ns	150 ns
Inverse Square Root ($1/\sqrt{x}$)	270 ns	225 ns
Whetstones/ms (C Compiler)	44,245	53,094
Drystones/s (C Compiler)	68,411	82,987

DEVELOPMENT TOOLS

Analog Devices offers one of the industry's most complete lines of hardware and software development tools, from our economical EZ-KIT starter packages to high-level language compilers and source-level debuggers. These tools are easy-to-learn and

easy-to-use, and whether the solution is provided by Analog Devices or by a third party, they share a common goal—to allow you to bring your DSP-based product to market in the fastest, most efficient way.

Your design project is supported by our DSP tools at every stage of the product development cycle, from research and evaluation to debug and test, helping you to:

Develop Algorithms & Define System Architecture
Develop DSP algorithms with third-party digital filter design packages that generate assembly language code. Define the system architecture using our software tools to specify memory configurations and I/O peripherals.

Develop Applications Code
Write code in our algebraic assembly language or in C, taking advantage of ready-to-use libraries of DSP, math, and ANSI-standard functions available both from Analog Devices and from third parties.

Simulate & Debug
Debug your code with a software simulator that lets you monitor all aspects of system operation while single-stepping through a program or pausing execution at breakpoints. Test programs at full speed using a low cost lab board that includes a DSP processor, system RAM, boot EPROM, and analog I/O with support circuitry.

Debug System Hardware with In-Circuit Emulation
Test the system hardware and software/hardware interaction with the use of our EZ-ICE emulators to provide full-speed, real-time emulation.

SOFTWARE TOOLS

Development Software

Analog Devices' Development Software is a complete set of programming tools for the ADSP-2100 Family processors and ADSP-21000 Family processors. Available on both the IBM PC-compatible and Sun workstation platforms, the development software includes:

System Builder module used to define the target system hardware.

Assembler for the processors' algebraic, easy-to-read instruction set.

Linker used to create executable programs from individually-assembled object files.

Librarian utility that combines frequently used subroutines into a single library file, simplifying the task of the linker and streamlining system software.

Simulators that provide an interactive, instruction-level simulation, displaying different portions of the processor and system hardware through a window-based graphical user interface.

PROM Splitter utility that reformats program code for use with a PROM programmer.

C Language Tools

Analog Devices' C language tools allow the coding of applications in ANSI-standard C. Both the fixed-point and floating-point C compilers are based on the industry-standard GNU C Compiler of the Free Software Foundation. They produce reliable, optimized code due to the widespread use and maturity of the GNU compiler, and provide straightforward methods for embedding assembly language instructions within a C program.

The ADSP-21000 Family floating-point compiler includes Numerical C extensions based on the work of the ANSI NCEG committee (Numerical C Extensions Group); these extensions are also incorporated into the GNU compiler, in *gcc* Version 2.4. Numerical C provides extensions to the C language for array selection, vector math operations, complex data types, circular pointers, and variably dimensioned arrays.

The suite of C tools also includes a C-callable library with ANSI-standard and custom DSP functions as well as a C Source-Level Debugger integrated within the simulator and emulator environments. The C library includes functions for simplified interrupt handling with automatic save and restore of registers. Interrupt routines can be written in either assembly language or in C.

Applications Code & 3rd Party Algorithm Developers
To help you develop your DSP system, Analog Devices offers a set of application notes and DSP handbooks with source code for a wide range of applications. The source code is available on diskette or from our computer bulletin board.

Independent Algorithm Vendors (IAVs) are another source for signal processing applications code. IAVs are technical experts in the field of DSP—they develop real-time solutions for specific algorithms, and license their code for integration into your end product.

HARDWARE TOOLS

EZ-LAB® Evaluation Boards

The EZ-LAB evaluation boards are stand-alone hardware platforms that let you test applications programs running in real time. Each EZ-LAB is a complete DSP system containing a 16-bit fixed-point or 32-bit floating-point processor plus memory and I/O. They also include a set of preprogrammed examples which demonstrate various speech and graphics applications.

Each ADSP-21xx EZ-LAB includes a voiceband codec with microphone input and powered speaker output for working with speech processing applications.

A four channel 8-bit DAC port is provided for monitoring of analog signal outputs, typically on an oscilloscope in the laboratory environment. Full memory expansion and additional I/O capabilities are provided by the EZ-LAB's bus expansion connector and serial port interface connector.

The ADSP-21xxx EZ-LABs include a PC host interface for downloading data and code to on-board memory. The ADSP-21020 EZ-LAB board is a stand-alone hardware platform similar to the ADSP-21xx EZ-LABs, while the ADSP-21060

EZ-LAB is a registered trademark of Analog Devices, Inc.

EZ-LAB is an even simpler-to-use PC plug-in card. These 32-bit, floating-point DSP system boards let you experiment with more powerful signal processing applications—each EZ-LAB contains an AD1848 SoundPort® Stereo Codec that provides 16-bit, CD-quality digital audio data with selectable sampling rates from 8 kHz to 48 kHz. General purpose analog I/O is provided by an AD7769 dual-channel ADC/DAC.

EZ-ICE® Emulators

The EZ-ICE emulators provide nonintrusive, target-based debugging of your DSP system. Compact and easy-to-use, these in-circuit emulators perform a wide range of emulation functions including single-step and full-speed execution with predefined breakpoints, viewing and/or altering of register and memory contents, and host PC upload/download operations. They can also be used in stand-alone mode for software-only debugging. By providing the same graphical user interface as the processor simulators, the EZ-ICEs require no additional learning or start-up time.

The ADSP-21000 Family EZ-ICE uses the JTAG test interface and on-chip emulation circuitry of each ADSP-21xxx processor to control the target system. Additional EZ-ICE features include emulator overlay memory, source-level symbolic debugging in either assembly language or C, plotting of memory data, and direct modification of code in the emulator's program memory window.

EZ-KIT STARTER PACKAGES

Our economical, entry-level EZ-KIT packages provide everything you need to start designing your DSP system. Each EZ-KIT contains an EZ-LAB Evaluation Board and a complete set of Development Software tools that let you define, code, debug, and demonstrate your design. With a single, comprehensive kit, you can explore the tremendous potential of DSP technology without a tremendous investment.

The software provided with each EZ-KIT includes both the basic assembler/linker and simulator tools as well as the C compiler, C library, and C source debugger. The EZ-LAB board provides a hardware platform for running and testing your applications in real-time. The EZ-KITs also include a DSP applications handbook (with source code diskette), a laboratory handbook with introductory DSP experiments, and a discount coupon for our training workshops.

THIRD PARTY DEVELOPMENT TOOLS

Our full line of DSP development tools is complemented by a broad range of third-party products including:

- Real-time operating systems
- Software packages for signal analysis, algorithm development, and filter design
- Software libraries in assembly and C
- PC plug-in boards and VMEbus boards
- Behavioral models

A comprehensive listing of our third-party partners—a list that continues to grow—is available upon request from your local sales office.

Selection Guides–Digital Signal Processing Products

Digital Signal Processors

		Features					On-Chip Memory		Peripherals				Packaging		
	Generic Model #	Cycle (ns)	Time (MHz)	Low Power Mode	Ext Inter	Input Volt Supply	Program RAM	Data RAM	Serial Ports	Program Timer	Host Inter Port	On-Chip A/D + D/A	# of Pins	Pkg Type	Temperature Range
Floating Point	ADSP-21020	50 40 33.3	20 25 30	–	4	5	Internal Program Cache: 32 × 48		–	–	–	–	223	PGA	0°C to +70°C –40°C to +85°C –55°C to +125°C
	ADSP-21060	25	40	–	3	3.3/5	Internal Program Cache: 32 × 48 4 MBit Total Internal						240	PQFP	0°C to +70°C –55°C to +125°C
	ADSP-21062	25	40	–	3	3.3/5	Internal Program Cache: 32 × 48 2 MBit Total Internal						240	PQFP	0°C to +70°C –55°C to +125°C
Fixed Point	ADSP-2101	80 60 50	12.5 16.67 20	2	3	5	2K × 24	1K × 16	2	√	–	–	68 80 68	PGA PQFP PLCC	0°C to +70°C –40°C to +85°C –55°C to +125°C
	ADSP-2103	100	10.24	2	3	3.3	2K × 24	1K × 16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2105	72	13.82	2	3	5	1K × 24	512 × 16	1	√	–	–	68	PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2111	77 60 50	13 16.67 20	2	3	5	2K × 24	1K × 16	2	√	√	–	100 100	PGA PQFP	0°C to +70°C –40°C to +85°C –55°C to +125°C
	ADSP-2115	72 60 50	13.82 16.67 20	2	3	5	1K × 24	512 × 16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-21msp55A ADSP-21msp50A	77	13.75	3	3	5	2K × 24	1K × 16	2	√	√	√	100 144	PQFP PGA	0°C to +70°C –40°C to +85°C
	ADSP-2161	60	16.67	2	3	5	8K × 24 ROM	512 × 16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2162	100	10.24	2	3	3.3	4K × 24 ROM	512 ×16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2163	60	16.67	2	3	5	8K × 24 ROM	512 × 16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2164	100	10.24	2	3	3.3	4K × 24 ROM	512 × 16	2	√	–	–	80 68	PQFP PLCC	0°C to +70°C –40°C to +85°C
	ADSP-2165	50	20	3	3	5	12K × 24-RAM 1K × 24-ROM	4K × 16	2	√	–	–	80	PQFP	0°C to +70°C –40°C to +85°C
	ADSP-2166	72	13.82	3	3	3.3	12K × 24-RAM 1K × 24-ROM	4K × 16	2	√	–	–	80	PQFP	0°C to +70°C –40°C to +85°C
	ADSP-2171	30	16.67	3	3	5	2K × 24	2K × 16	2	√	√	–	128 128	TQFP PQFP	0°C to +70°C –40°C to +85°C
	ADSP-2173	50	10	3	3	3.32	2K × 24	2K × 16	2	√	√	–	128 128	TQFP PQFP	–40°C to +85°C
	ADSP-2181	30	16.67	3	6	5	16K × 24 RAM	16K × 16	2	√	–	–	128 128	PQFP TQFP	0°C to +70°C –40°C to +85°C

PLCC: Plastic Leaded Chip Carrier. PQFP Plastic Quad Flatpack. PGA: Pin Grid Array.
ADSP-2161, 62, 63, 64, 66: Custom ROM Coded DSPs with 10,000 pcs. minimum and $10,000 NRE.

Within each family, all processors are code-compatible, allowing additional features and performance while protecting software development investment.

Digital Signal Processing Products–Selection Guides

DSP Development Tools

		ADSP-2101	ADSP-2103	ADSP-2105	ADSP-2111	ADSP-2115	ADSP-216x Series	ADSP-217x Series	ADSP-2181	ADSP-21msp50A/55A	ADSP-21020	ADSP-2106x/SHARC
Complete Software and Hardware Development Kits												
ADDS-2101-EZ-KIT	Includes C-Compiler & 2101-EZ-LAB	✓	✓	✓		✓	✓					
ADDS-2111-EZ-KIT	Includes C-Compiler & 2111-EZ-LAB				✓							
ADDS-21020-EZKITPL	Includes C-Compiler & 21020-EZ-LAB										✓	
ADDS-2106X-EZ-KIT	Includes C-Compiler & 2106x-EZ-LAB											✓
Evaluation/Demonstration Boards												
ADDS-2101-EZ-LAB	Stand-Alone Board for Testing Coded Apps	✓	✓	✓		✓	✓					
ADDS-2111-EZ-LAB	Stand-Alone Board for Testing Coded Apps				✓							
ADDS-2171-EZ-LAB	Stand-Alone Board for Testing Coded Apps							✓				
ADDS-MSP50-EZ-LAB	Stand-Alone Board for Testing Coded Apps									✓		
ADDS-21020-EZ-LAB	Stand-Alone Board for Testing Coded Apps										✓	
ADDS-2106X-EZ-LAB	Stand-Alone Board for Testing Coded Apps											✓
In-Circuit Emulators												
ADDS-2101-EZ-ICE	Compact In-Circuit Emulator for 21xx	✓	✓	✓		✓	✓					
ADDS-2111-EZ-ICE	Compact In-Circuit Emulator for 2111				✓							
ADDS-2171-EZ-ICE	Compact In-Circuit Emulator for 2171							✓				
ADDS-2171-EZ-ICE-P	Compact ICE for 2171 with PQFP Adaptor							✓				
ADDS-2181-EZ-ICE	Compact In-Circuit Emulator for 2181								✓			
ADDS-MSP50-EZ-ICE	Compact In-Circuit Emulator for msp50/55									✓		
ADDS-21020-EZ-ICE	Compact In-Circuit Emulator for 21010/20										✓	
ADDS-2106X-EZ-ICE	Compact In-Circuit Emulator for SHARC											✓
Development Software												
ADDS-21XX-SW-PC	Assembler, Simulator & C Tools for PC	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ADDS-21XX-SW-SUN	Assembler, Simulator & C Tools for SUN	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ADDS-210XX-SW-PC	Assembler, Simulator & C Tools for PC										✓	✓
ADDS-210XX-SW-SUN	Assembler, Simulator & C Tools for SUN										✓	✓
System Programming & Development Workshops					Call (617) 461-3672 for current schedule							
ADDS-21XX-WKSHP	3-Day Fixed-Point Customer Workshop	✓	✓	✓	✓	✓	✓	✓	✓	✓		
ADDS-210XX-WKSHP	3-Day Floating-Point Customer Workshop										✓	✓

ANALOG DEVICES

Mixed-Signal Processors with Host Interface Ports

ADSP-21msp50A/55A/56A

FEATURES

77 ns Instruction Cycle Time from 13.00 MHz Crystal
ADSP-2100 Family Code & Function Compatible
2K Words of On-Chip Program Memory RAM
1K Words of On-Chip Data Memory RAM
2K Words of On-Chip Program Memory ROM (ADSP-21msp56A Only)
8- or 16-Bit Parallel Host Interface Port
Analog Interface Provides
- **16-Bit Sigma-Delta ADC and DAC**
- **Programmable Gain Stages**
- **On-Chip Antialiasing and Anti-Imaging Filters**
- **8 kHz Sampling Frequency**
- **65 dB ADC, SNR and THD**
- **77 dB DAC, SNR and THD**

<1 mW Powerdown Mode with 100 Cycle Recovery
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides:
- **Zero Overhead Looping**
- **Conditional Instruction Execution**

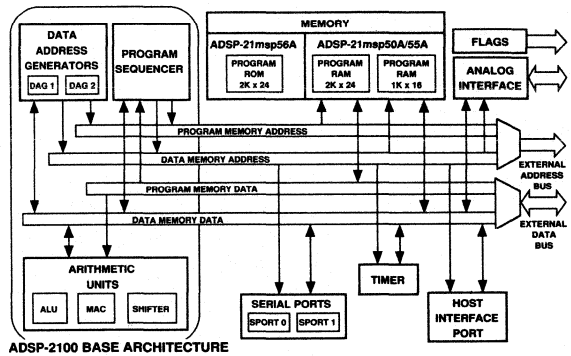
Two Double-Buffered Serial Ports with Companding Hardware, One Serial Port Has Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
100-Lead PQFP and 144-Pin PGA

GENERAL DESCRIPTION

The ADSP-21msp5xA Family of Mixed-Signal Processors (MSProcessors™) are fully integrated, single chip DSPs complete with a high performance analog front end. The ADSP-21msp5x Family is optimized for voice band applications such as Speech Compression, Speech Processing, Speech Recognition, Text-to-Speech, and Speech-to-Text conversion.

MSProcessors is a trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



ADSP-2100 BASE ARCHITECTURE

The ADSP-21msp5xA combines the ADSP-2100 base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a host interface port, an analog front end, a programmable timer, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-21msp50A and ADSP-21msp55A provide 2K words (24-bit) of program RAM and 1K word (16-bit) of data memory. The ADSP-21msp56A provides an additional 2K words (24-bit) of program ROM. All of the products in the ADSP-21msp5xA family integrate a high performance analog front end based on a single chip, voice band front end, the AD28msp02. Powerdown circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-21msp50A is available in a 144-pin PGA package. The ADSP-21msp55A and ADSP-21msp56A, reduced pin versions, are available in a 100-pin PQFP package.

Table I. ADSP-21msp5xA Processor Differences

	Total Pins	V_{CC}	V_{DD}	GND_A	GND	Program Memory	Flags	Powerdown Acknowledge Pin	HIP Width
ADSP-21msp50A	144	1	5	2	7	2K RAM	3	Y	8 or 16 Bits
ADSP-21msp55A	100	1	4	2	5	2K RAM	1	N	8 Bits
ADSP-21msp56A	100	1	4	2	5	2K RAM 2K ROM	1	N	8 Bits

Table I highlights the differences among ADSP-21msp5xA processors.

Fabricated in a high-speed, double poly, double metal, low power, CMOS process, the ADSP-21msp5xA family operates with a 77 ns instruction cycle time. Every instruction executes in a single cycle.

The ADSP-21msp5xA's flexible architecture and comprehensive instruction set allow the processor to perform multiple tasks in parallel. In one cycle the ADSP-21msp5xA can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- perform an analog conversion
- receive and transmit data through the two serial ports
- receive and/or transmit data through the host interface port

In-Circuit Emulation

Analog Devices provides an ADSP-21msp5xA In-Circuit Emulator (ICE) to debug your system. The emulator consists of hardware, host computer resident software, and the emulator probe (the part of the emulator that fits in the ADSP-21msp5xA socket in your system). If you plan to use the emulator, you should consider the following:

- the physical dimensions of the emulator probe (you must leave enough clearance around the ADSP-21msp5xA socket to connect the probe)
- the emulator probe has the same footprint as the 144-pin PGA package; adapter sockets are available to convert the probe to 100-lead PQFP packages
- the emulator's restrictions (differences between emulator and processor operation).

For detailed information about the restrictions, operation, and mechanical specifications of the emulator, see the ADDS-21XX-ICE data sheet, ADSP-21msp50A Emulator release note, and the *ADSP-21msp50A Emulator Manual Addendum* to the *ADSP-2111 Emulator Manual.*

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-21msp5xA. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler produces object code, and the Linker combines object modules and library calls into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface. A PROM Splitter generates PROM programmer compatible files. The C Compiler generates ADSP-21msp5xA assembly source code.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-21msp5xA. The ADSP-21msp50A EZ-ICE® emulator aids in the hardware debugging of ADSP-21msp5xA systems. The emulator performs a full range of emulation functions including stand-alone operation, single-step or full-speed operation in the target, changing register values, and setting breakpoints. The EZ-LAB® demonstration board is a complete ADSP-21msp5xA system that executes EPROM-based programs.

Additional Information

This data sheet provides a general overview of ADSP-21msp5xA functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual.* For more information about the Development System and ADSP-21msp5xA programmer's reference information, refer to the *ADSP-2100 Family Development Software Manuals*, the *ADSP-2111 Emulator Manual*, and the *ADSP-21msp50A Emulator Manual Addendum.*

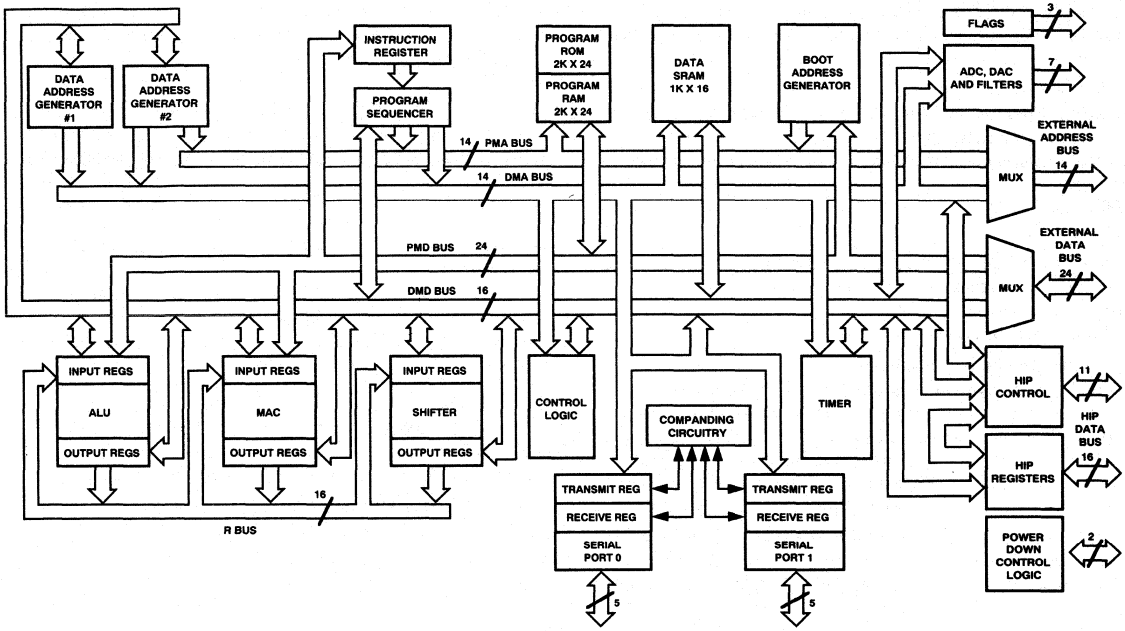


Figure 1. ADSP-21msp5xA Block Diagram

DIGITAL ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-21msp5xA. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21msp5xA executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off chip, and the two data buses (PMD and DMD) share a single external data bus.

Program memory can store both instructions and data, permitting the ADSP-21msp5xA to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-21msp5xA can fetch an operand from on-board program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). Bus grant has two modes of operation. If GoMode is enabled in the MSTAT register, instruction execution continues from internal memory. If GoMode is disabled, the processor stops instruction execution and waits for the deassertion of $\overline{BR}$.

In addition to the address and data bus for external memory connection, the ADSP-21msp5xA has a Host Interface Port (HIP) for easy connection to a host processor. The HIP is made up of 16 data/address pins and 11 control pins (only 8 data/address and 10 control pins on the ADSP-21msp55A/56A). The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000

series, the Intel 80C51 series and the Analog Devices' ADSP-2101 can be easily connected to the HIP. The host processor can boot the ADSP-21msp5xA's on-chip memory through the HIP.

The ADSP-21msp5xA can respond to eleven interrupts. There can be up to three external interrupts, configured as edge or level sensitive, and eight internal interrupts generated by the Timer, the Serial Ports ("SPORTs"), the HIP, the powerdown circuitry, and the analog interface. There is also a master RESET signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 77 ns ADSP-21msp5xA to use an external 250 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware. The on-chip program memory can also be initialized through the HIP.

The ADSP-21msp5xA features three general-purpose flag outputs whose states are controlled through software. (Only one flag output is available on the ADSP-21msp55A/56A.) You can use these outputs to signal an event to an external device. In addition, the data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n-1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-21msp5xA instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-21msp5xA assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-21msp5xA incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-21msp5xA SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORTs receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORT0 can receive and transmit an entire circular buffer of data with only one overhead cycle per data word (Autobuffering Mode). An interrupt is generated after a completed data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be reconfigured for two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-21msp5xA is available in a 100-lead PQFP and a 144-pin PGA package. Table II contains the pin descriptions. Pins marked with an asterisk (*) differ according to the package.

Table II. ADSP-21msp5xA Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Digital Pins			
Address	14	O	Address output for program, data and boot memory spaces
Data	24	I/O	Data I/O pins for program and data memories. Input only for boot memory space, with two MSBs used as boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor reset input
$\overline{\text{IRQ2}}$	1	I	External interrupt request #2
$\overline{\text{BR}}$	1	I	External bus request input
$\overline{\text{BG}}$	1	O	External bus grant output
$\overline{\text{PMS}}$	1	O	External program memory select
$\overline{\text{DMS}}$	1	O	External data memory select
$\overline{\text{BMS}}$	1	O	Boot memory select
$\overline{\text{RD}}$	1	O	External memory read enable
$\overline{\text{WR}}$	1	O	External memory write enable
MMAP	1	I	Memory map select
CLKIN, XTAL	2	I	External clock or quartz crystal input
CLKOUT	1	O	Processor clock output
$\overline{\text{HSEL}}$	1	I	HIP select input
$\overline{\text{HACK}}$	1	O	HIP acknowledge output
HSIZE	*	I	8/16 bit host select input 0 = 16-bit; 1 = 8-bit ADSP-21msp50A only
BMODE	1	I	Boot mode select input 0 = EPROM/data bus; 1 = HIP
HMD0	1	I	Bus strobe select input 0 = RD, WR; 1 = RW, DS

Table II. 21msp5x Pin List (Continued)

Pin Group Name	# of Pins	Input/ Output	Function
HMD1	1	I	HIP address/data mode select input 0 = separate; 1 = multiplexed
$\overline{HRD}/\overline{HRW}$	1	I	HIP read strobe/ read/write select input
$\overline{HWR}/\overline{HDS}$	1	I	HIP write strobe/ host data strobe select input
HD15-0/ HAD15-0	*	I/O	HIP data/data and address Only HD7-0 on ADSP-21msp55A/56A
HA2/ALE	1	I	Host address 2/ Address latch enable input
HA1-0/ unused	2	I	Host addresses 1 and 0 inputs
SPORT0	5	I/O	Serial port 0 I/O pins (TFS0, RFS0, DT0, DR0, SCLK0)
SPORT1 or	5	I/O	Serial port 1 I/O pins
$\overline{IRQ1}$ (TFS1)	1	I	External interrupt request #1
$\overline{IRQ0}$ (RFS1)	1	I	External interrupt request #0
SCLK1	1	O	Programmable clock output
FO (DT1)	1	O	Flag Output pin
FI (DR1)	1	I	Flag Input pin
FL2-0	*	O	General purpose flag output pins, Only FL0 on ADSP-21msp55A/ 56A
V_{DD}	*		Digital power supply, 4 on 100-lead PQFP, 5 on 144-pin PGA
GND	*		Digital ground, 5 on 100-lead PQFP, 7 on 144-pin PGA
$\overline{PWD}$	1	I	Powerdown pin
PWDACK	*	O	Powerdown acknowledge pin, ADSP-21msp50A only
Analog Pins			
VIN_{NORM}	1	I	Input terminal of the NORM amplifier for the encoder section (ADC)
VIN_{AUX}	1	I	Input terminal of the AUX amplifier for the encoder section (ADC)
DECOUPLE	1	I	Ground reference of the NORM and AUX amplifiers for the encoder section (ADC)
$VOUT_P$	1	O	Noninverting output terminal of the differential amplifier from the decoder section (DAC)
$VOUT_N$	1	O	Inverting output terminal of the differential amplifier from the decoder section (DAC)
V_{REF}	1	O	Output voltage reference
REF_FILTER	1	O	Voltage reference external bypass filter node
V_{CC}	1		Analog power supply, 1 on 100-lead PQFP and 144-pin PGA
GND_A	2		Analog ground, 2 on 100-lead PQFP and 144-pin PGA

2

Host Interface Port

The ADSP-21msp5xA host interface port is a parallel I/O port that allows for an easy connection to a host processor. Through the HIP, the ADSP-21msp5xA can be used as a memory-mapped peripheral to a host computer. The HIP can be thought of as an area of dual-ported memory, or mailbox registers, that allow communication between the computational core of the ADSP-21msp5x and the host computer.

The HIP is completely asynchronous. The host processor can write data into the HIP while the ADSP-21msp5xA is operating at full speed.

The HIP can be configured with the following pins:

- HSIZE (ADSP-21msp50A only) configures HIP for 8-bit or 16-bit communication with the host processor.
- BMODE determines whether the ADSP-21msp5xA boots from the host processor (through the HIP) or external EPROM (through the data bus).
- HMD0 configures the bus strobes as separate read and write strobes, or a single read/write select and a host data strobe.
- HMD1 selects separate address (3-bit) and data (16-bit) buses, or a multiplexed, 16-bit address/data bus with address latch enable.

Tying these pins to appropriate values configures the ADSP-21msp5x for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

In 8-bit reads, the ADSP-21msp5xA tristates the upper eight bits of the bus. When the host processor writes an 8-bit value to the HIP, the upper eight bits are all zeros. For additional information refer to the *ADSP-2100 Family User's Manual*, Chapter 7, Host Interface Port.

HIP Operation

The HIP contains six data registers (HDR5–0) and two status registers (HSR7–6) with an associated HMASK register for masking interrupts from individual HIP data registers. All HIP data registers are memory-mapped into the internal data memory of the ADSP-21msp5xA. HIP transfers can be managed using either interrupts or a polling scheme. These registers are shown in the section "ADSP-21msp5xA Registers."

The HIP allows a software reset to be performed by the host processor. The internal software reset signal is asserted for five ADSP-21msp5xA cycles.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-21msp5xA provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, and the flags. The ADSP-21msp5xA also supports internal interrupts from the timer, the host interface port, the two serial ports, the analog interface, and the powerdown control circuit. The interrupt levels are internally prioritized and individually maskable (except powerdown and reset). The input pins can be programmed to be either level- or edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table III, and the interrupt registers are shown in Figure 2.

Table III. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)	
Reset (or Power-Up with PUCR = 1)	0000	(*highest priority*)
Powerdown (Nonmaskable)	002C	
$\overline{IRQ2}$	0004	
HIP Write	0008	
HIP Read	000C	
SPORT0 Transmit	0010	
SPORT0 Receive	0014	
Analog Interface Transmit	0018	
Analog Interface Receive	001C	
SPORT1 Transmit or $\overline{IRQ1}$	0020	
SPORT1 Receive or $\overline{IRQ0}$	0024	
Timer	0028	(*lowest priority*)

Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The powerdown interrupt is nonmaskable.

The interrupt control register, ICNTL, allows the external interrupts to be either edge- or level-sensitive. Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially.

The IFC register is a write-only register used to force an interrupt or clear a pending edge-sensitive interrupt.

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt nesting.

System Interface

Figure 3 shows a basic system configuration with the ADSP-21msp5x, two serial devices, a host processor, a boot EPROM, optional external program and data memories, and an analog interface. Up to 15K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories. The ADSP-21msp5xA also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

The ADSP-21msp5xA can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated at any frequency other than the one specified. Operating the ADSP-21msp5xA at any other frequency changes the analog performance, which is not tested or supported.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

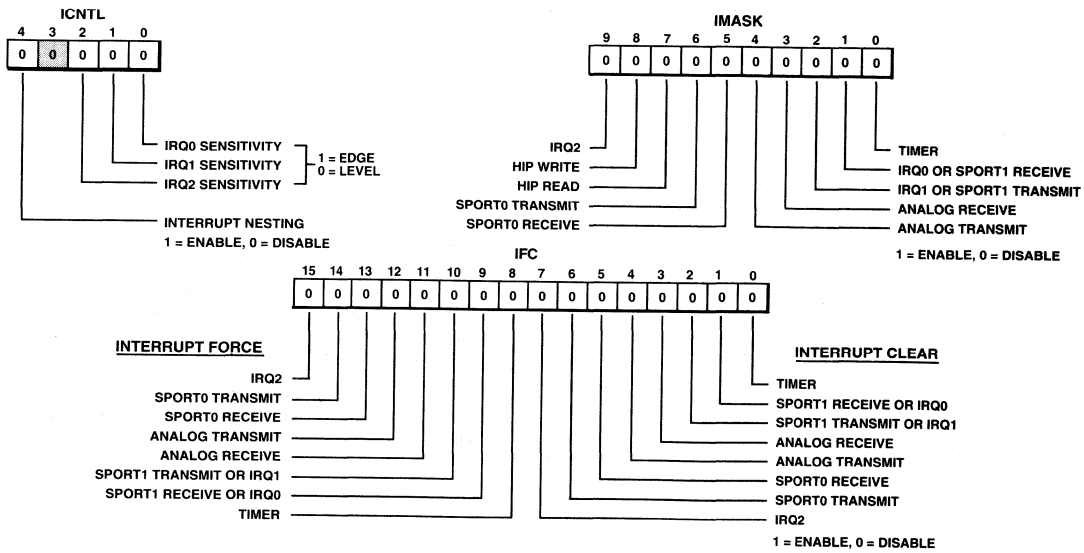
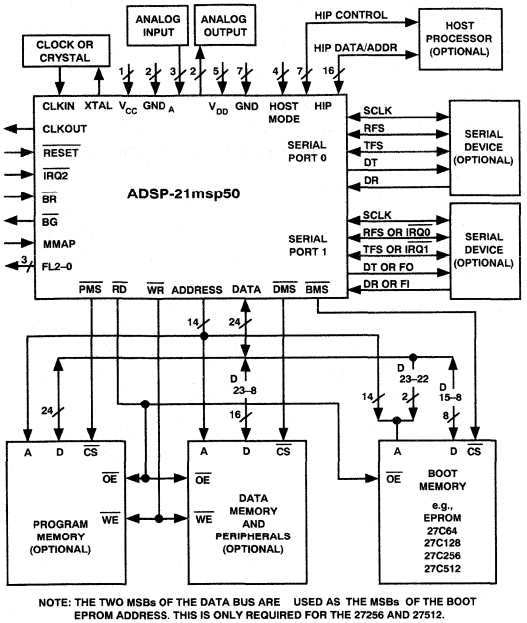


Figure 2. Interrupt Registers



NOTE: THE TWO MSBs OF THE DATA BUS ARE USED AS THE MSBs OF THE BOOT EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-21msp5xA Basic System Configuration

Because the ADSP-21msp5xA includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

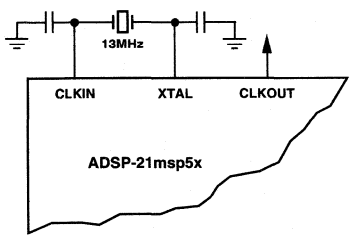


Figure 4. External Crystal Connections

A clock output (CLKOUT) signal is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-21msp5xA. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000 and execution begins.

Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words. 4K words of memory for the ADSP-21msp5xA with optional 2K words ROM and 2K words of RAM memory for non-ROM versions are on chip.

The program memory data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe.

The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal. An external program memory access should always be qualified with the $\overline{\text{PMS}}$ signal.

The ADSP-21msp5xA writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

ADSP-21msp50A/55A

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the two configurations. When MMAP = 0, internal RAM occupies 2K words beginning at address 0x0000; external program memory uses the remaining 14K words beginning at address 0x0800. In this configuration, the boot loading sequence (described in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of external program memory begin at address 0x0000 and internal RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, the boot loading sequence does not take place; execution begins immediately after RESET.

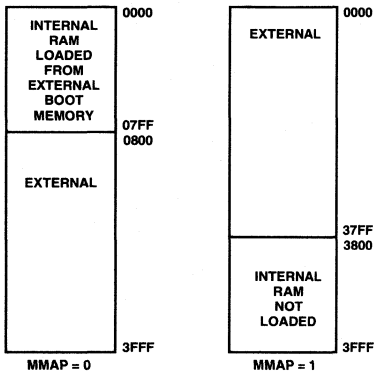


Figure 5. ADSP-21msp50A/55A Program Memory Maps

ADSP-21msp56A

The ADSP-21msp56A is functionally identical to the ADSP-21msp50A/55A. The ADSP-21msp56A includes an additional 2K by 24-bit mask programmable ROM (see Figure 6). The ROM can be used to hold program instructions or data and can be accessed twice in one instruction cycle if necessary. The ROM always resides at locations PM[0x0800] through PM[0x1000] regardless of the state of the MMAP pin. The ROM is enabled by setting the ROMENABLE bit in the Data Memory Wait State control register, DM[0x3FFE]. When the ROMENABLE bit is set to 1, addressing program memory in this range will access the on-chip ROM. When set to zero, addressing program memory in this range will access external program memory. The ROMENABLE bit is set to 0 on chip reset.

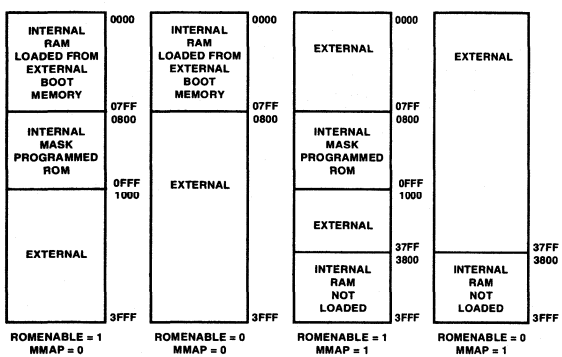


Figure 6. ADSP-21msp56A Program Memory Maps

The program memory interface can generate 0 to 7 wait states for external memory devices; default is 7 wait states after $\overline{\text{RESET}}$.

Data Memory Interface

The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{\text{DMS}}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21msp5xA supports memory-mapped I/O, with the peripherals memory mapped into the data or program memory address spaces and accessed by the processor in the same manner.

Data Memory Map

The on-chip data memory RAM resides in the lK words of data memory beginning at address 0x3800, as shown in Figure 7. In addition, data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration, host interface port, codec, and serial port operations are located in this region of memory.

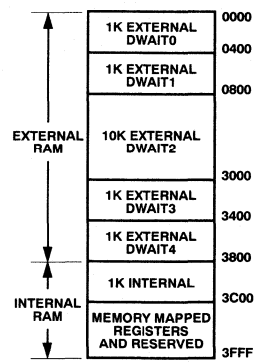


Figure 7. ADSP-21msp5xA Data Memory Map

The remaining 14K of data memory is external. External data memory is divided into five zones, each associated with its own wait state generator. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{\text{RESET}}$.

Boot Memory Interface

The ADSP-21msp5xA can load on-chip memory from external boot memory space. The boot memory space consists of 64K by 8-bit space, divided into eight separate 8K by 8-bit pages. Three bits in the system control register select which page is loaded by the boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{\text{RESET}}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 3 wait states after $\overline{\text{RESET}}$. This allows the ADSP-21msp5x to boot from a single low cost EPROM such as a 27256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{\text{BMS}}$ and $\overline{\text{RD}}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate addressing up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

The ADSP-2100 Family Assembler and Linker support the creation of programs and data structures requiring multiple boot pages during execution.

$\overline{\text{RD}}$ and $\overline{\text{WR}}$ must always be qualified by $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, or $\overline{\text{BMS}}$ to ensure the correct program, data, or boot memory accessing.

HIP Booting

The ADSP-21msp5xA can also boot programs through its Host Interface Port. If BMODE = 1, the ADSP-21msp5xA boots from the HIP. If BMODE = 0, the ADSP-21msp5xA boots through the data bus (in the same way as the ADSP-2101), as described above in "Boot Memory Interface." For additional information about HIP booting, refer to the *ADSP-2100 Family User's Manual*, Chapter 7, "Host Interface Port."

The ADSP-2100 Family Development Software includes a utility program called the HIP Splitter. This utility allows the creation of programs that can be booted via the ADSP-21msp5xA's HIP, in a similar fashion as EPROM-bootable programs generated by the PROM Splitter utility.

Bus Request and Bus Grant

The ADSP-21msp5xA can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{\text{BR}}$) signal. If the ADSP-21msp5xA is not performing an external memory access, then it responds to the active $\overline{\text{BR}}$ input in the following cycle by

- tristating the data and address buses and the $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$ output drivers,
- asserting the bus grant ($\overline{\text{BG}}$) signal, and
- halting program execution.

If the Go mode is enabled, the ADSP-21msp5xA will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21msp5xA is performing an external memory access when the external device asserts the $\overline{\text{BR}}$ signal, then it will not tristate the memory interfaces or assert the $\overline{\text{BG}}$ signal until the cycle after the access completes, which can be up to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{\text{BR}}$ signal is released, the processor releases the $\overline{\text{BG}}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{\text{RESET}}$ is active.

ANALOG INTERFACE

The analog interface contains encoding circuitry (ADC), decoding circuitry (DAC), and processor interface logic. A block diagram of the ADSP-21msp5xA analog section is shown in Figure 8.

The analog interface is configured through the Analog Control Register and the Analog Autobuffer/Powerdown Register (refer to "ADSP-21msp5xA Registers"). The Analog Control Register DM[0x3FEE] configures the programmable gain stages, the analog input multiplexer and the analog interface powerdown state. Note that unused bits in this register must be cleared to zero.

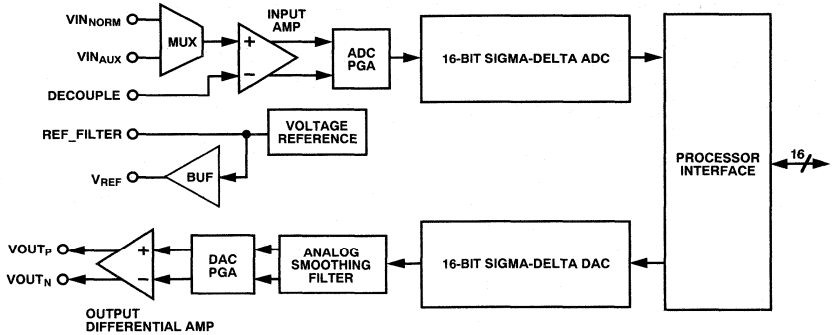


Figure 8. Analog Interface Block Diagram

A/D Conversion
The A/D conversion circuitry of the ADSP-21msp5xA consists of an analog multiplexer, an input amplifier, a programmable gain amplifier (ADC PGA), and a 16-bit sigma-delta ADC.

Analog Input Amplifiers and Multiplexer
The analog multiplexer selects either the NORM or AUX channel as the input to the ADC's sigma-delta modulator. The analog inputs should be ac coupled.

The ADC PGA may be used to additionally increase the signal level by +6 dB, +20 dB, or +26 dB. This gain is selected by Bit 9 and Bit 0 (IG0, IG1) of the analog control register. Input signal level to the sigma-delta ADC should not exceed the V_{INMAX} specification.

ADC
The analog interface's ADC consists of a 2nd-order analog sigma-delta modulator, an antialiasing decimation filter, and an optional digital high-pass filter. For a detailed description of the ADC components, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

D/A Conversion
The D/A conversion circuitry of the ADSP-21msp5xA's analog interface consists of a sigma-delta digital-to-analog converter (DAC), an analog smoothing filter, a programmable gain amplifier (DAC PGA), and a differential output amplifier.

DAC
The DAC consists of an optional digital high-pass filter, an anti-imaging interpolation filter, and a digital sigma-delta modulator. The digital filters and sigma-delta modulator have the same characteristics as the filters and modulator of the ADC. For a detailed description of the DAC components, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

Analog Smoothing Filter & Programmable Gain Amplifier
The analog smoothing filter consists of a 2nd-order Sallen-Key continuous-time filter and a 3rd-order switched capacitor filter. The Sallen-Key filter has a 3 dB point at approximately 80 kHz.

The DAC's programmable gain amplifier (DAC PGA) can be used to adjust the output signal level by −15 dB to +6 dB in 3 dB increments. This gain is selected by Bits 2–4 (OG0, OG1, OG2) of the of the analog control register.

Differential Output Amplifier
The ADSP-21msp5xA's analog output signal ($VOUT_P$–$VOUT_N$) is produced by a differential amplifier. The differential amplifier meets specifications for loads greater than 2 kΩ, it can drive loads as small as 50 Ω with degraded performance, and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The output signal is dc-biased to the ADSP-21msp5xA's on-chip voltage reference (V_{REF}) and can be ac coupled directly to a load or dc-coupled to an external amplifier.

The $VOUT_P$–$VOUT_N$ outputs must be used as a differential signal; do not use either pin as a single-ended output.

OPERATING THE ANALOG INTERFACE
The analog interface of the ADSP-21msp5xA is operated with several memory-mapped control and data registers. The ADC and DAC I/O data is received and transmitted through two memory-mapped data registers. The data can also be autobuffered directly into (or from) on-chip memory. In both cases, the I/O processing is interrupt-driven: two ADSP-21msp5xA interrupts are dedicated to the analog interface, one for ADC receive data and one for DAC transmit data.

The ADSP-21msp5xA must have an input clock frequency of 13 MHz. At this frequency, analog-to-digital and digital-to-analog converted data is transmitted at an 8 kHz rate with a single 16-bit word transmitted every 125 μs.

For detailed information about the Analog Interface, refer to the *ADSP-2100 Family User's Manual*, Chapter 8, "Analog Interface."

Autobuffering
In some applications it is advantageous to perform block data transfers between the analog converters and processor memory. Analog interface autobuffering enables the automatic transfer of data blocks directly from the ADC to on-chip processor data memory or from on-chip processor data memory to the DAC.

ADC & DAC Interrupts
The analog interface generates two interrupts that signal either: 1) that a 16-bit, 8 kHz analog-to-digital or digital-to-analog conversion has been completed, or 2) that an autobuffer block transfer has been completed (i.e. the data buffer contents have been received or transmitted).

When an analog interrupts occurs, the processor vectors to the addresses listed in *Table III, Interrupt Priority and Interrupt Vector Address*.

The ADC receive and DAC transmit interrupts occur at an 8 kHz rate, indicating when the data registers should be accessed. On the receive side, the ADC interrupt is generated each time an A/D conversion cycle is completed and the 16-bit data word is available in the ADC receive register. On the transmit side, the DAC interrupt is generated each time a D/A conversion cycle is completed and the DAC transmit register is ready for the next 16-bit data word.

Both interrupts are generated simultaneously at an 8 kHz rate, occurring every 1625 instruction cycles with a 13.00 MHz processor clock. The interrupts are generated continuously, starting when the analog interface is powered up by setting the APWD bits (Bits 5, 6) to ones in the analog control register. Because both interrupts occur simultaneously, only one should be enabled (in IMASK) to vector to a single service routine which handles both transmit and receive data. However, when using autobuffer transfers, both interrupts should be enabled.

POWERDOWN

The ADSP-21msp5xA processors contain a low power feature that allows the processor to enter a very low power dormant state through hardware or software control. Here is a brief list of powerdown features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9, "System Interface" for detailed information about the powerdown features.

- Powerdown mode holds the processor in CMOS standby with a maximum current of less than 100 μA in some modes.
- Quick recovery from powerdown. In some modes, the processor can begin executing instructions in less than 100 cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during powerdown without affecting the lowest power rating and 100 cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 cycle startup.
- Powerdown is initiated by either the powerdown pin ($\overline{PWD}$) or the software powerdown force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering-down. The powerdown interrupt also can be used as a nonmaskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the powerdown state.
- The $\overline{RESET}$ pin also can be used to terminate powerdown, and the host software reset feature can be used to terminate powerdown under certain conditions.
- Powerdown acknowledge pin (on ADSP-21msp50A only) indicates when the processor has entered powerdown.

Idle

When the ADSP-21msp5xA is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction.

Slow Idle

The IDLE instruction is enhanced on the ADSP-21msp5xA to slow the processor's internal clock, which further reduces power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the IDLE instruction. The format of the instruction is

IDLE(n);

where: n = 16, 32, 64, or 128.

The instruction keeps the processor fully functional, operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK and timer clock, are reduced by the same ratio. CLKOUT remains at normal rate; it is not reduced. The default form of the instruction, when no clock divisor is given, is the standard IDLE instruction.

When the IDLE(n) instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts—the 1-cycle response time of the standard idle state—is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-21msp5xA remains in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the IDLE(n) instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processors cycles).

ADSP-21msp5xA Registers

Figure 9 summarizes all the registers in the ADSP-21msp5xA. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

A secondary set of registers in all computational units allows a single-cycle context switch.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT register, timer registers, HIP control registers, HIP data registers, and SPORT control registers are all mapped into data memory; that is, you access these registers by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

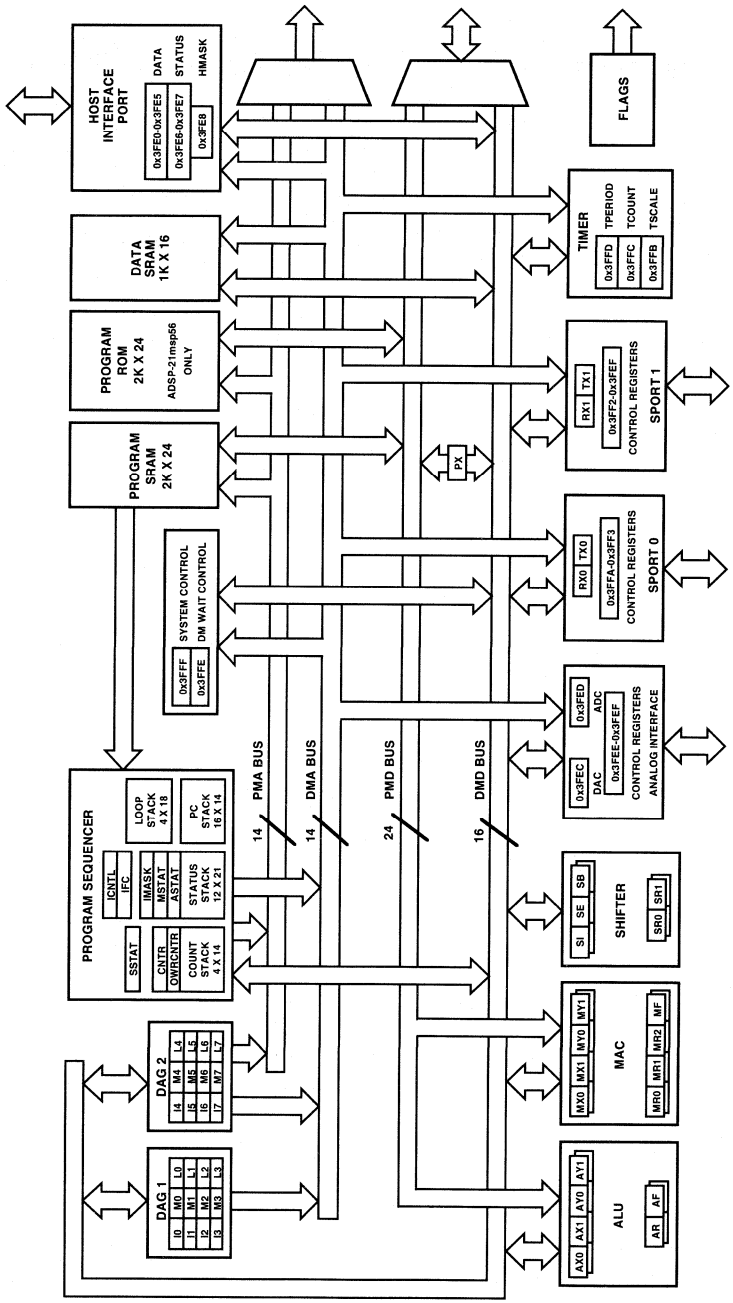
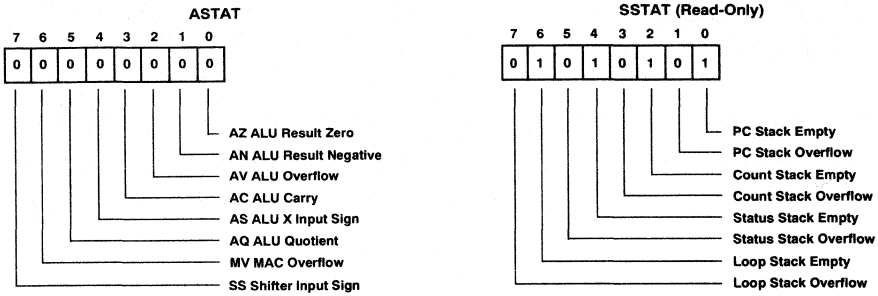
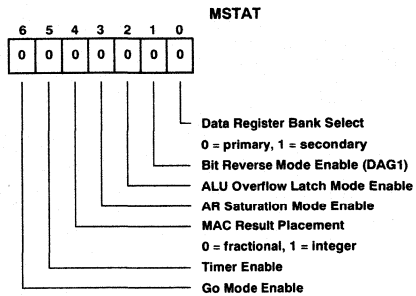
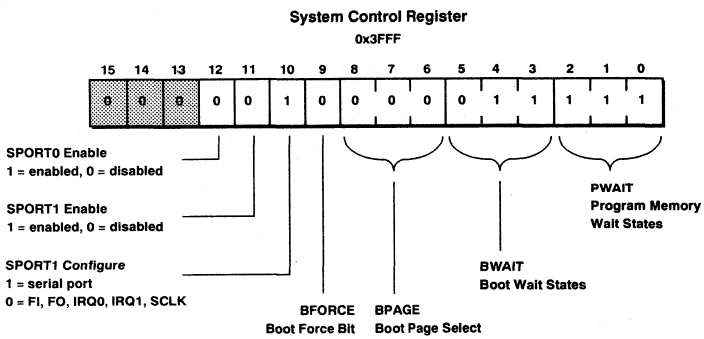
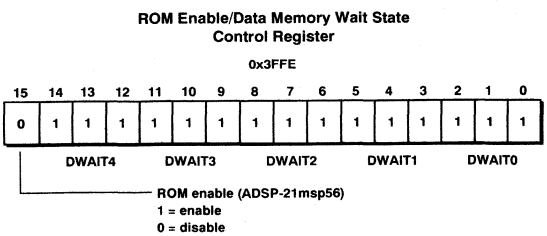


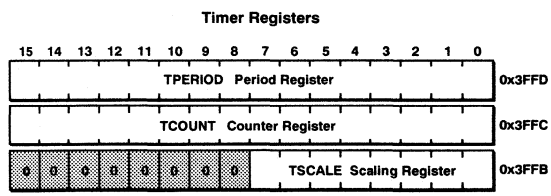
Figure 9. ADSP-21msp5xA Registers











Control Registers

SPORT0 Multichannel Receive Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FFA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0x3FF9

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Multichannel Transmit Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FF8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

0x3FF7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Control Register

0x3FF6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Multichannel Enable MCE
- Internal Serial Clock Generation ISCLK
- Receive Frame Sync Required RFSR
- Receive Frame Sync Width RFSW
- Multichannel Frame Delay MFD
  Only If Multichannel Mode Enabled
- Transmit Frame Sync Required TFSR
- Transmit Frame Sync Width TFSW
- ITFS Internal Transmit Frame Sync Enable
  (or MCL Multichannel Length; 1 = 32 words, 0 = 24 words
  Only If Multichannel Mode Enabled)
- SLEN Serial Word Length
- DTYPE Data Format
  00 = right justify, zero-fill unused MSBs
  01 = right justify, sign extend into unused MSBs
  10 = compand using μ-law
  11 = compand using A-law
- INVRFS Invert Receive Frame Sync
- INVTFS Invert Transmit Frame Sync
  (or INVTDV Invert Transmit Data Valid
  Only If Multichannel Mode Enabled)
- IRFS Internal Receive Frame Sync Enable

SPORT0 SCLKDIV
Serial Clock Divide Modulus

0x3FF5

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 RFSDIV
Receive Frame Sync Divide Modulus

0x3FF4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT0 Autobuffer Control Register

0x3FF3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0											0	0

TIREG TMREG RIREG RMREG

- TBUF Transmit Autobuffering Enable
- RBUF Receive Autobuffering Enable

SPORT1 Control Register

0x3FF2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- Flag Out (Read Only)
- Internal Serial Clock Generation ISCLK
- Receive Frame Sync Required RFSR
- Receive Frame Sync Width RFSW
- Transmit Frame Sync Required TFSR
- Transmit Frame Sync Width TFSW
- ITFS Internal Transmit Frame Sync Enable
- SLEN Serial Word Length
- DTYPE Data Format
  00 = right justify, zero-fill unused MSBs
  01 = right justify, sign extend into unused MSBs
  10 = compand using μ-law
  11 = compand using A-law
- INVRFS Invert Receive Frame Sync
- INVTFS Invert Transmit Frame Sync
- IRFS Internal Receive Frame Sync Enable

Control Registers

Analog Autobuffer/Powerdown Control Register

0x3FEF

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0											0	0

- **XTALDIS** — XTAL pin disable during powerdown; 1 = disabled, 0 = enabled (disable XTAL pin when no external crystal connected)
- **XTALDELAY** — Delay startup from powerdown 4096 cycles; 1 = delay, 0 = no delay
- **PDFORCE** — Powerdown force
- **PUCR** — Exit from powerdown context; 1 = soft reset, 0 = resume execution
- **ARBUF** — ADC Receive Autobuffer Enable
- **ATBUF** — DAC Transmit Autobuffer Enable
- **ARMREG** — Receive M register
- **ARIREG** — Receive I register
- **ATMREG** — Transmit M register
- **ATIREG** — Transmit I register

SPORT1 SCLKDIV
Serial Clock Divide Modulus

0x3FF1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

SPORT1 RFSDIV
Receive Frame Sync Divide Modulus

0x3FF0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Analog Control Register

0x3FEE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
										0G2	0G1	0G0			

- **IG0** — ADC Input Gain
- **DABY** — DAC High Pass Filter Bypass; 1 = bypass, 0 = insert
- **ADBY** — ADC High Pass Filter Bypass; 1 = bypass, 0 = insert
- **APWD** — Analog Interface Powerdown; 0 = powerdown, 1 = enable (set both bits to 1 to enable interface)
- **IG1** — ADC Input Gain
- **IMS** — ADC Input Multiplexer Select; 1 = AUX input, 0 = NORM input
- **0G2, 0G1, 0G0** — DAC Output Gain (for PGA)

IG1,IG0 — ADC Input Gain (for PGA)

Gain	IG1	IG0
0dB	0	0
+6dB	0	1
+20dB	1	0
+26dB	1	1

Gain	0G2	0G1	0G0
+6dB	0	0	0
+3dB	0	0	1
0dB	0	1	0
–3dB	0	1	1
–6dB	1	0	0
–9dB	1	0	1
–12dB	1	1	0
–15dB	1	1	1

All bits are set to 0 at processor reset.
(Reserved bits 9-15 must always be set to 0)

HIP Data Registers

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
HDR5																	0x3FE5
HDR4																	0x3FE4
HDR3																	0x3FE3
HDR2																	0x3FE2
HDR1																	0x3FE1
HDR0																	0x3FE0

HMASK Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x3FE8

- HOST HDR5 READ
- HOST HDR4 READ
- HOST HDR3 READ
- HOST HDR2 READ
- HOST HDR1 READ
- HOST HDR0 READ
- HOST HDR0 WRITE
- HOST HDR1 WRITE
- HOST HDR2 WRITE
- HOST HDR3 WRITE
- HOST HDR4 WRITE
- HOST HDR5 WRITE

INTERRUPT ENABLES
1 = enable
0 = disable

HSR6 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

0x3FE6

- 21msp5x HDR5 WRITE
- 21msp5x HDR4 WRITE
- 21msp5x HDR3 WRITE
- 21msp5x HDR2 WRITE
- 21msp5x HDR1 WRITE
- 21msp5x HDR0 WRITE
- HOST HDR0 WRITE
- HOST HDR1 WRITE
- HOST HDR2 WRITE
- HOST HDR3 WRITE
- HOST HDR4 WRITE
- HOST HDR5 WRITE

HSR7 Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

0x3FE7

- OVERWRITE MODE
- SOFTWARE RESET
- 21msp5x HDR0 WRITE
- 21msp5x HDR1 WRITE
- 21msp5x HDR2 WRITE
- 21msp5x HDR3 WRITE
- 21msp5x HDR4 WRITE
- 21msp5x HDR5 WRITE

Control Registers

INSTRUCTION SET DESCRIPTION

The ADSP-21msp5xA assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize internal memory and conform to the ADSP-21msp5x's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
MF=MX0*MY1 (RND), MX0=DM (I2,M1); {MF=error*beta}
MR=MX0*MF (RND), AY0=PM (I6,MS);
DO adapt UNTIL CE;
      AR=MR1 + AY0, MX0=DM (I2,M1), AY0=PM (I6,M7);
adapt: PM(I6,M6) =AR, MR=MX0*MF (RND);
MODIFY (I2, M3);                {Point to oldest data}
MODIFY (I6, M7);                {Point to start of data}
```

CIRCUIT DESIGN CONSIDERATIONS

The following sections discuss interfacing analog signals to the ADSP-21msp5xA.

Analog Signal Input

Figure 10 shows the recommended input circuit for the ADSP-21msp5xA's analog input pin (either VIN_{NORM} or VIN_{AUX}). The circuit of Figure 10 implements a first-order low-pass filter (R_1C_1) with a 3 dB point less than 20 kHz. This is the only filter required external to the processor to prevent aliasing of the sampled signal. Since the ADSP-21msp5xA's sigma-delta ADC uses a highly oversampled approach that transfers the bulk of the antialiasing filtering into the digital domain, the off-chip antialiasing need only be of low order.

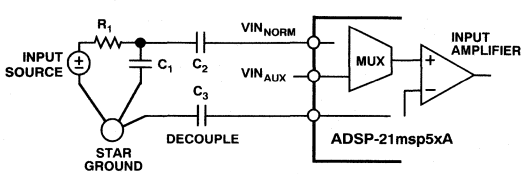


Figure 10. Recommended Analog Input Circuit

The ADSP-21msp5xA's on-chip ADC PGA can be used when there is not enough gain in the input circuit. The PGA gain is set by Bits 9 and 0 (IG1, IG0) of the processor's analog control register. The gain must be chosen to ensure that a full-scale input signal (at R1 in Figure 10) produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed V_{INMAX} (refer to the "Analog Interface Electrical Characteristics" specifications).

VIN_{NORM} and VIN_{AUX} are biased at the Internal Reference Voltage (nominal of 2.5 V) of the msp5xA, which lets the analog section of the msp5xA operate from a single supply. The input signal to the msp5xA should be ac coupled with an external capacitor (C_2). The value of C_2 is determined by the input resistance of the msp5xA (125 kΩ) and the desired cutoff frequency. The cutoff frequency should be ≤30 Hz. The following equations should be used to determine the values for R_1, C_1, C_2; R_1 should be less than or equal to 200 Ω. C_2 should be ≥0.047 µf; C_3 should be equal to C_2.

$$C_2 = \frac{1}{2\,\pi\,f_1\,R_{IN}}$$

R_{IN} = MSP5x input resistance (125 kΩ)
f_1 = cutoff frequency <30 Hz

$$R_1 = \frac{1}{2\,\pi\,f_2\,C_1}$$

$R_1 \leq 200\ \Omega$
f_2 >8 kHz <20 kHz

$$C_1 = \frac{1}{2\,\pi\,f_2\,R_1}$$

Analog Signal Output

The ADSP-21msp5xA's differential analog output ($VOUT_P$–$VOUT_N$) is produced by an on-chip differential amplifier which is part of the processor's analog interface. The differential amplifier meets specifications for loads greater than 2 kΩ, it can drive loads as small as 50 Ω with degraded performance, and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The differential output can be ac coupled directly to a load or dc-coupled to an external amplifier.

Figure 11 shows a simple circuit providing a differential output with ac coupling. The capacitor of this circuit (C_{OUT}) is optional; if used, its value can be chosen as follows:

$$C_{OUT} = \frac{1}{(60\,\pi)\,R_L}$$

The $VOUT_P$, $VOUT_N$ outputs must be used as differential outputs; do not use either as a single-ended output. Figure 12 shows an example circuit which can be used to convert the differential output to a single-ended output. The circuit uses a differential-to-single-ended amplifier, the Analog Devices SSM2141.

Voltage Reference Filter Capacitance

Figure 13 shows the recommended reference filter capacitor connections. The capacitor grounds should be connected to the same star ground point shown in Figure 10.

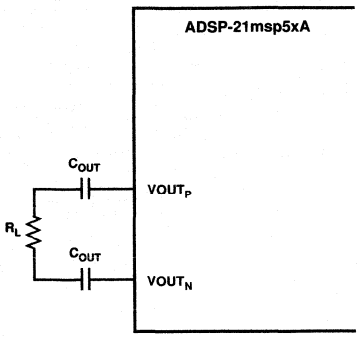


Figure 11. Example Circuit for Differential Output with AC Coupling

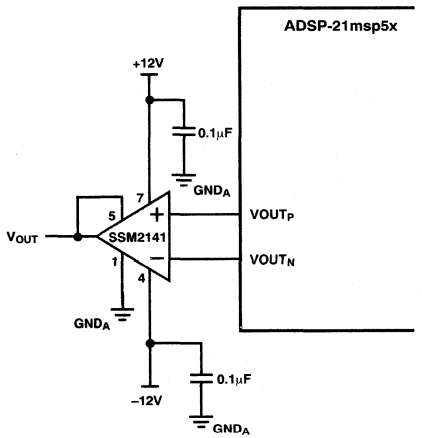


Figure 12. Example Circuit for Single-Ended Output

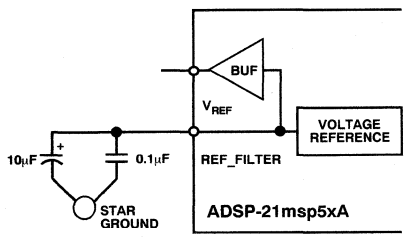


Figure 13. Voltage Reference Filter Capacitor

APPLICATION EXAMPLES

The ADSP-21msp5xA is ideal for speech processing applications where high performance for analog and digital circuitry is required, but board space is severely limited. The cellular radio handset is one application. Here, the ADSP-21msp5xA can digitize the speech, then perform compression algorithms that sufficiently reduce the bit rate for transmission in a limited radio bandwidth.

DEFINITION OF SPECIFICATIONS

Absolute Gain

Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured with a 1.0 kHz sine wave at 0 dBm0. The absolute gain specification is used as a reference for gain tracking error specification.

Gain Tracking Error

Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 1 kHz at 0 dBm0 (equal to absolute gain). Gain tracking error at 0 dBm0 is 0 dB by definition.

SNR + THD

Signal-to-noise ratio plus total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300–3400 Hz, including harmonics but excluding dc.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For final testing, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

Idle Channel Noise

Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300–3400 Hz).

Crosstalk

Crosstalk is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of the same signal which couples onto the adjacent channel. Crosstalk is expressed in dB.

Power Supply Rejection

Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Group Delay

Group delay is defined as the derivative of radian phase with respect to radian frequency, $\partial\phi(\omega)/\partial\omega$. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay away from a constant indicates the degree of nonlinear phase response of the system.

ADSP-21msp50A/55A/56A—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	°C

Refer to Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = −0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = −100 μA[10]	V_{DD} − 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	μA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	μA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	μA
I_{DD}	Digital Supply Current (Idle)[8, 9]	Codec Inactive		16	mA
I_{DD}	Digital Supply Current (Dynamic)[9]	Processor 80% Loaded, Codec Active[11]		90	mA
I_{DD}	Digital Supply Current (Powerdown)[9]	See ADSP-2100 Family User's Manual, Chapter 9		100	μA
I_{CC}	Analog Supply Current (Dynamic)[9]	Codec Active		28	mA
C_I	Input Pin Capacitance[1, 10, 12]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 10, 12, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES

[1]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1–0.

[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, DT0, DT1, CLKOUT, $\overline{\text{HACK}}$, FL2–0.

[3]Bidirectional pins: D0–D23, RFS0, $\overline{\text{RFS1}}$, $\overline{\text{SCLK0}}$, $\overline{\text{SCLK1}}$, $\overline{\text{TFS0}}$, TFS1 HD0–HD15/HAD0–HAD15.

[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RFS1, HD0–HD15/HAD0–HAD15.

[5]$\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 input pins.

[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).

[7]Although specified for TTL outputs, all ADSP-21msp5xA outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc loads.

[8]Idle refers to ADSP-21msp5xA state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND. Refer to chart in back for lower IDLE currents.

[9]Current reflects device operating with no output loads.

[10]Guaranteed but not tested.

[11]V_{CC} = V_{DD} = max, t_{CK} = 77 ns, ambient temperature = +85°C, 80% execution type 1 instructions, with random data. Refer to section titled "Power Dissipation" for typical figures for digital and analog supply currents.

[12]Applies to PGA and PQFP package types.

[13]Output pin capacitance is the capacitive load for any tristated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} +0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} +0.3 V
Operating Temperature Range (Ambient) . . . −40°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-21msp5xA is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-21msp5xA features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-21msp5xA has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-21msp5xA timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	Address Setup to Write End
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

FREQUENCY RESPONSE

Freq (Hz)	ADC Max (dB)	ADC Min (dB)	DAC Max (dB)	DAC Min (dB)
0+	−60.00	N/A	−60.00	N/A
95	−25.00	N/A	−25.00	N/A
150	+0.266	−0.134	+0.015	−0.185
300	+0.272	−0.128	+0.03	−0.17
1000	+0.00	+0.00	+0.00	+0.00
2000	+0.05	−0.35	+0.00	−0.20
3000	−0.20	−0.60	−0.10	−0.30
3400	−0.30	−0.70	−0.14	−0.34
3700	−0.375	−0.775	−0.17	−0.37
3850	−25.00	N/A	−25.00	N/A
4000	−60.00	N/A	−60.00	N/A

NOTES
All specs relative to absolute gain @ 1.0 kHz
Both ADC and DAC high-pass filters *inserted*.
ADC specs *include* input RC filter attenuation (see Analog Test Conditions for RC filter details).

NOISE AND DISTORTION

Parameter	Min	Max	Unit	Test Conditions
ADC Intermodulation Distortion		−55	dB	m, n = 1 and 2; f_a = 984; f_b = 1047
DAC Intermodulation Distortion		−70	dB	m, n = 1 and 2; f_a = 984; f_b = 1047
ADC Idle Channel Noise		65	dBm0	
DAC Idle Channel Noise		72	dBm0	
ADC Crosstalk (DAC to ADC)		−65	dB	DAC signal level: 1.0 kHz, 0 dBm0 ADC at idle
DAC Crosstalk (ADC to DAC)		−65	dB	DAC idle ADC signal level: 1.0 kHz, 0 dBm0
ADC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
DAC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
ADC Group Delay[1]		1	ms	300–3000 Hz
DAC Group Delay[1]		1	ms	300–3000 Hz
ADC SNR + THD		65	dB	1.0 kHz; 0 dBm0
DAC SNR + THD		77	dB	1.0 kHz, 0 dBm0

[1]Guaranteed but not tested.

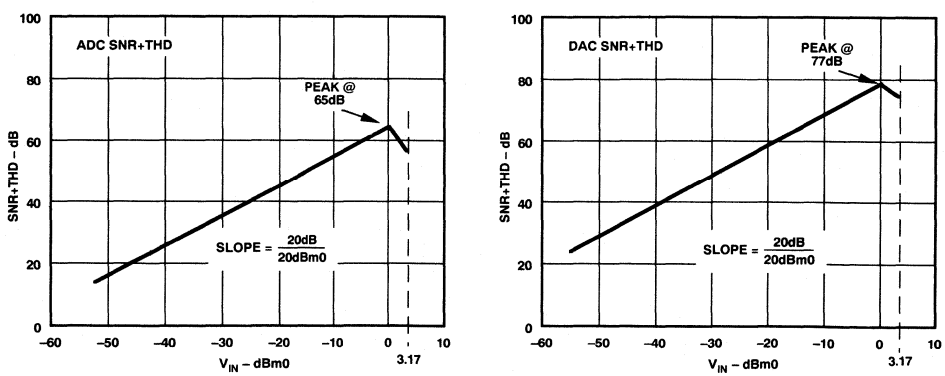


Figure 14. SNR + THD vs. V_{IN}

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ADC:					
R_I	Input Resistance[4] at VIN_{NORM}, VIN_{AUX}		125		kΩ
VIN_{MAX}	Maximum Input Range[1, 4]			3.156	V p-p
DAC:					
R_O	Output Resistance[2, 4]		2.5		Ω
V_{OOFF}	Output DC Offset[3]	−400		400	mV
V_{VREF}	Voltage Reference (V_{REF})	2.25		2.75	V
V_O	Maximum Voltage Output Swing (p–p) Across R_L				
	Single-Ended[4]			3.156	V p-p
	Differential[4]			6.312	V p-p
R_L	Load Resistance[2, 4]	2			kΩ

Test Conditions for all analog interface tests: Unity input gain, ADC PGA bypassed, D/A PGA set for 0 dB gain, no load on analog output ($VOUT_P$–$VOUT_N$).

[1]At input to sigma-delta modulator of ADC.
[2]At $VOUT_P$–$VOUT_N$.
[3]Between $VOUT_P$ and $VOUT_N$.
[4]Guaranteed but not tested.

GAIN

Parameter	Min	Typ	Max	Unit	Test Conditions
ADC Absolute Gain	−0.6	0	0.6	dBm0	1.0 kHz, 0 dBm0
ADC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0
DAC Absolute Gain	−0.6	0	0.6	dBm0	1.0 kHz, 0 dBm0
DAC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0
DAC PGA Relative Gain	−0.6		0.6	dBm0	1.0 kHz
ADC PGA Relative Gain	−0.6		0.6	dBm0	1.0 kHz

Parameter		Min	Max	Unit
Clock Signals				
Timing Requirement:				
t_{CK}[1]	CLKIN Period	76.9	150	ns
t_{CKL}	CLKIN Width Low	20		ns
t_{CKH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CPL}	CLKOUT Width Low	$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{CK}$[2]		ns

NOTES
[1]t_{CK} values within the range of CLKIN period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CPH} = 0.5\ t_{CK} - 10$ ns = 0.5 (76.9) − 10 ns = 28.5 ns.
[2]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 processor cycles assuming stable CLKIN (not including crystal oscillator start-up time).

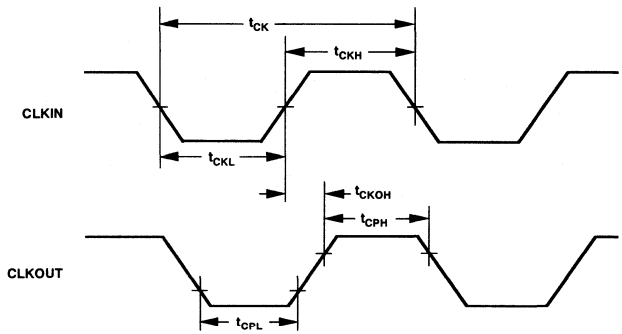


Figure 15. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	IRQx or FI Setup before CLKOUT Low[1, 2]	$0.25t_{CK}$ + 18		ns
t_{IFH}	IRQx or FI Hold after CLKOUT High[1, 2]	$0.25t_{CK}$		ns
	IRQx = $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$			
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT High	0		ns
t_{FOD}	Flag Output Delay from CLKOUT High		15	ns
	Flag Output = FL0, FL1, FL2, and FO			

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.

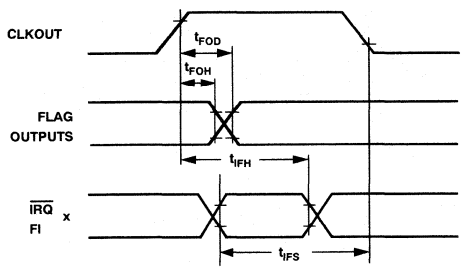


Figure 16. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 20		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ − 10		ns

NOTE
[1]$\overline{BR}$ is a synchronous signal which must meet setup/hold time requirements. Refer to the User's Manual for $\overline{BR}$/$\overline{BG}$ cycle relationships.

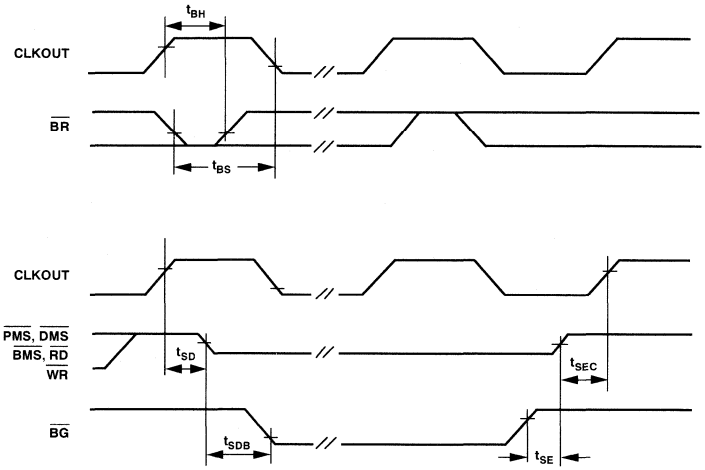


Figure 17. Bus Request – Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 15+w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 20+w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

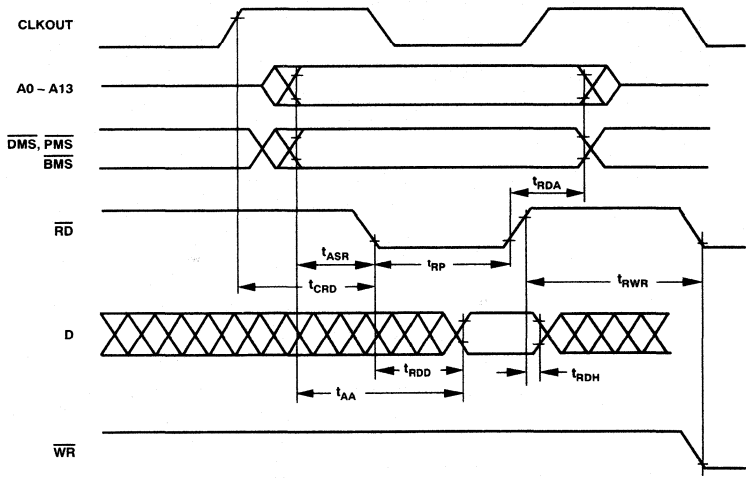


Figure 18. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10+w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5+w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15+w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns
		w = wait states × (t_{CK})		

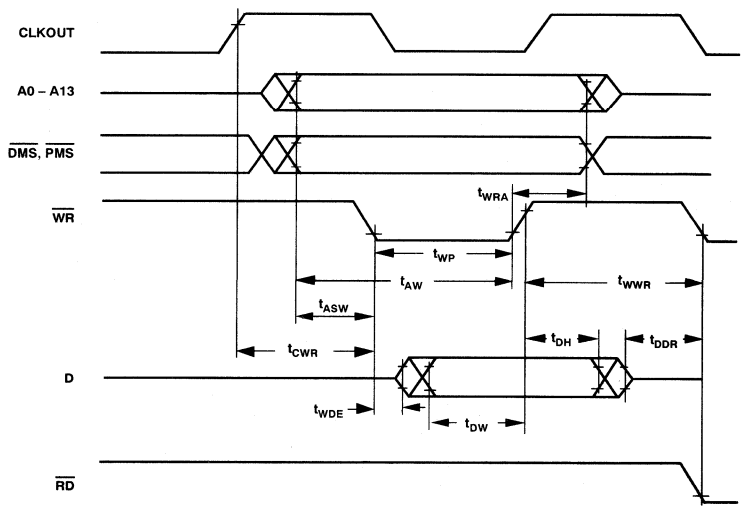


Figure 19. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	76.9		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		ns
t_{SCP}	$SCLK_{in}$ Width	28		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{out}$	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		20	ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		20	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (alt) to DT Enable	0		ns
t_{TDV}	TFS (alt) to DT Valid		18	ns
t_{SCDD}	SCLK High to DT Disable		25	ns
t_{RDV}	RFS (multichannel, frame delay zero) to DT Valid		20	ns

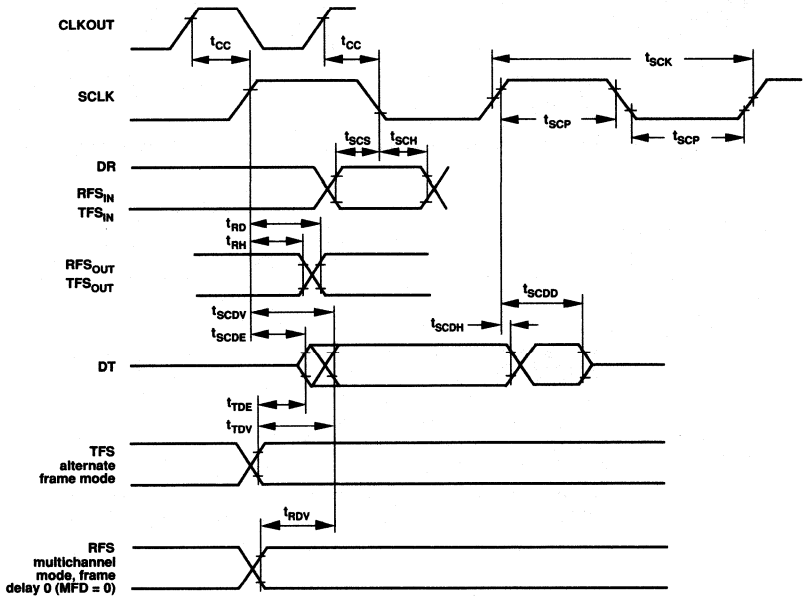
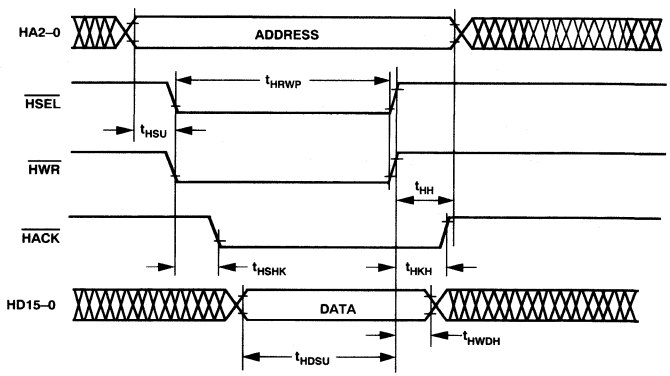


Figure 20. Serial Ports

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HSU}	HA2–0 Setup before Start of Write or Read[1, 2]	8		ns
t_{HDSU}	Data Setup before End of Write[3]	8		ns
t_{HWDH}	Data Hold after End of Write[3]	3		ns
t_{HH}	HA2–0 Hold after End of Write or Read[3, 4]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[2]	0		ns
t_{HDD}	Data Valid after Start of Read[2]		23	ns
t_{HRDH}	Data Hold after End of Read[4]	0		ns
t_{HRDD}	Data Disabled after End of Read[4]		10	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

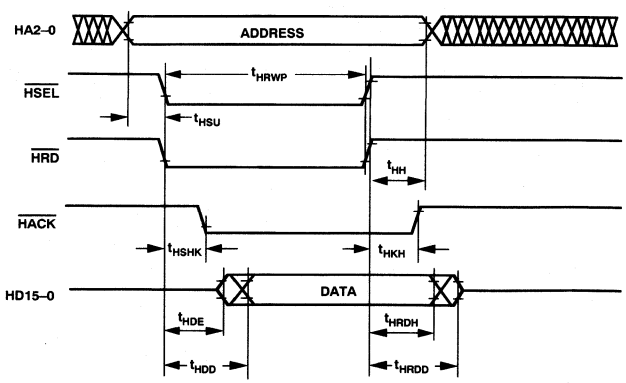
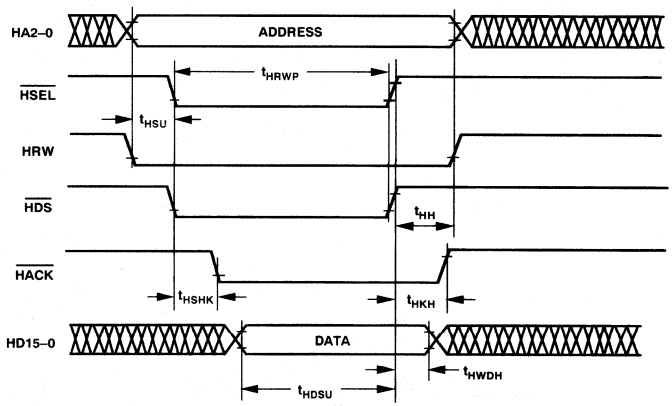


Figure 21. Host Interface Port (HMD1 = 0, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read/Write Strobe and Data Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	Data Setup before End of Write[2]	8		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		23	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		10	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High or $\overline{HSEL}$ High.
[3]Read or Write Pulse Width – $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

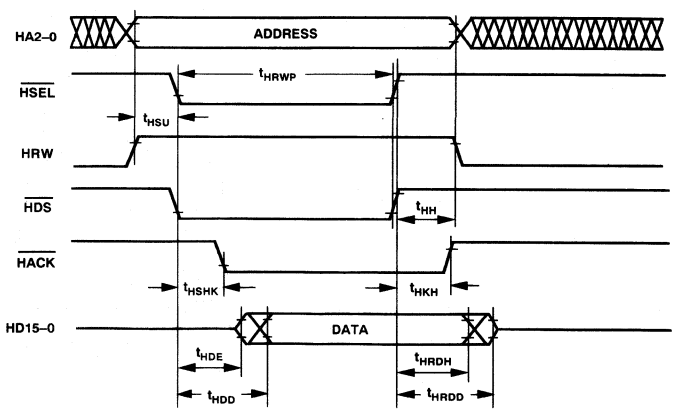
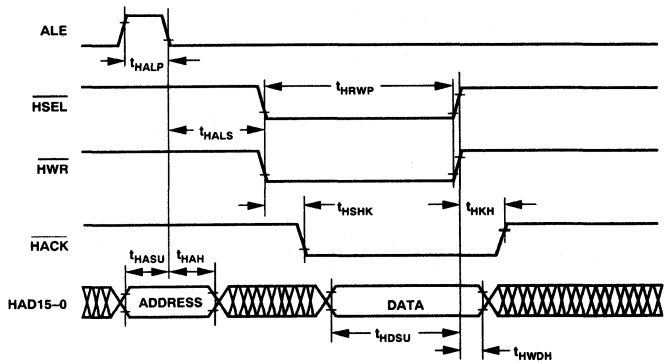


Figure 22. Host Interface Port (HMD1 = 0, HMD0 = 1)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	0		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	12		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	15		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[3]	8		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[4]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[4]		10	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

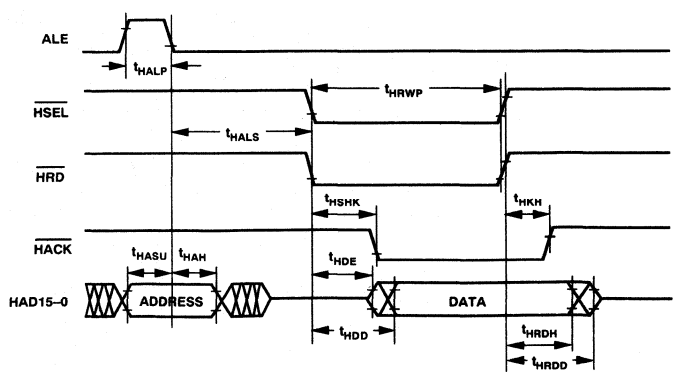
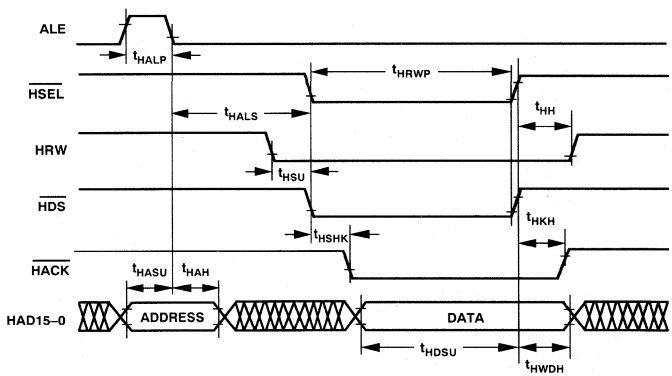


Figure 23. Host Interface Port (HMD1 = 1, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read/Write Strobe and Data Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	15		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	0		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	12		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	15		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	8		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	30		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	20	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	20	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		23	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		10	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High or $\overline{HSEL}$ High.
Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

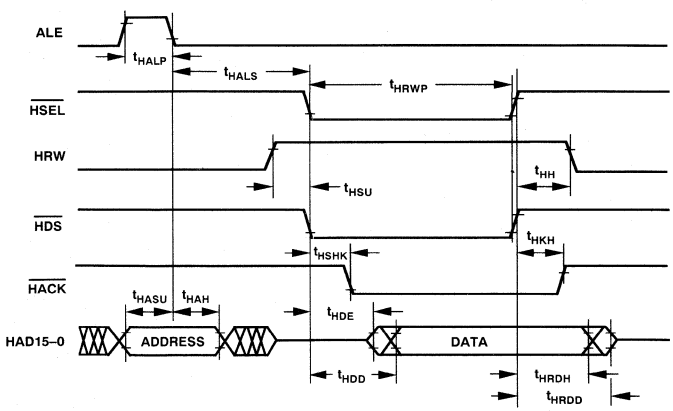


Figure 24. Host Interface Port (HMD1 = 1, HMD0 = 1)

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{amb} = T_{case} - (PD \times \theta_{CA})$

T_{case} = Case temp in °C
PD = Power dissipation in W
θ_{CA} = Thermal resistance (case-to-ambient)
θ_{JA} = Thermal resistance (junction-to-ambient)
θ_{JC} = Thermal resistance (junction-to-case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	20°C/W	6°C/W	14°C/W
PQFP-100 Lead	50°C/W	28°C/W	22°C/W

Power Dissipation

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:

In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows.

Assumptions:

- External data memory is accessed every cycle with 50% of address pins switching.
- External data memory writes occur every other cycle with 50% of address pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 76.9 ns.

Total Power Dissipation = P_{INT} + ($C \times V_{DD}^2 \times f$)

P_{INT} = internal power dissipation, from Power vs. Frequency graph. $C \times V_{DD}^2 \times f$ is calculated for each output:

	# of Pins	× C	$\times V_{DD}^2$	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 13.0 MHz	=	26 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 6.5 MHz	=	15 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 6.5 MHz	=	2 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 13.0 MHz	=	3 mW
						46 mW

Total power dissipation for this example is P_{INT}+46 mW.

Typical Power Consumption

The typical power consumption can be calculated from the following data, taken at 5.0 V and +25°C executing 80% type 1 multifunction instructions, on random data.

Parameter	Typ
I_{DD} Digital Supply Current (IDLE, Codec Powered Up)	20 mA
I_{DD} Digital Supply Current (IDLE)	11 mA
I_{DD} Digital Supply Current (Dynamic, Codec Powered Up)	70 mA
I_{DD} Digital Supply Current (Powerdown)	10 µA
I_{CC}Analog Supply Current (Dynamic)	21 mA

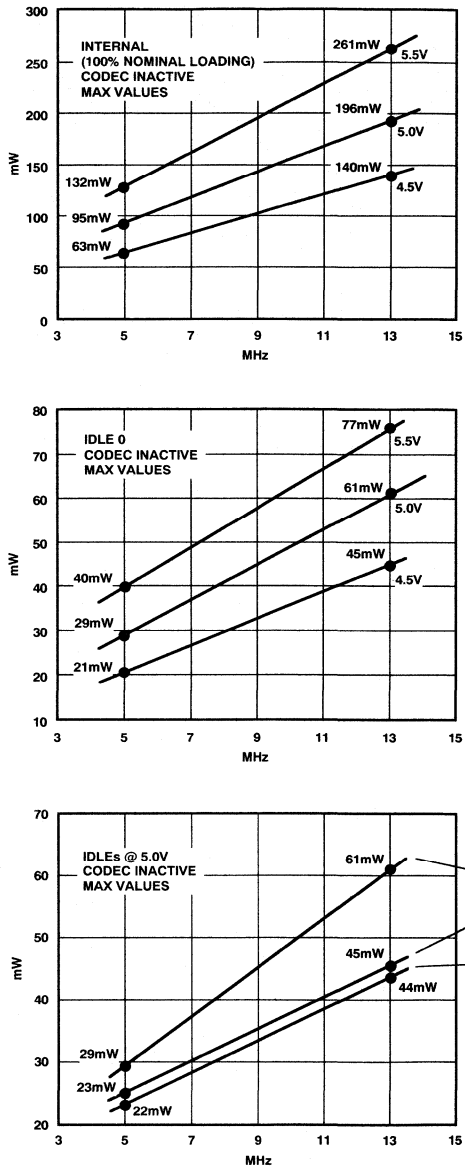


Figure 25. Power vs. Frequency

Analog Devices recommends that the ADSP-21msp5xA is used with a 13.0 MHz input clock. Below this input clock frequency, the codec performance will change and the performance specifications cannot be guaranteed. The codec filter characteristics will, however, scale approximately linearly with frequency.

If the codec is disabled, then the processor can be used at any allowed input clock frequency. The power consumption of the ADSP-21msp5xA at these frequencies is shown above.

CAPACITIVE LOADING

Figures 26 and 27 show capacitive loading characteristics for the ADSP-21msp5xA.

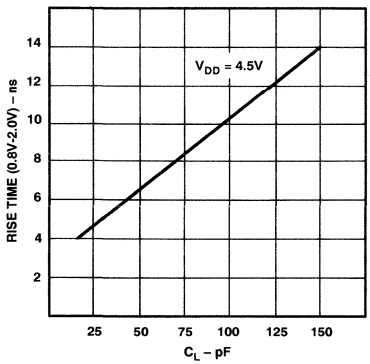


Figure 26. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

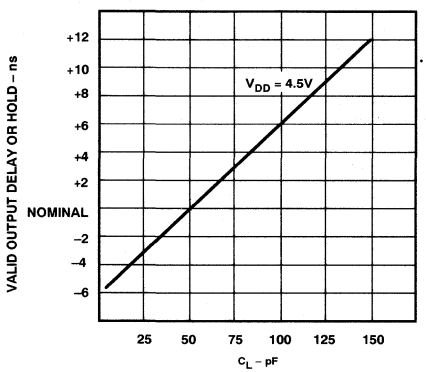


Figure 27. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Digital

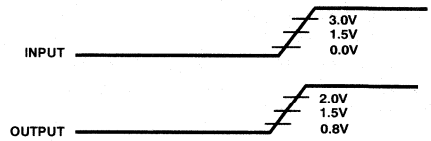


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Analog

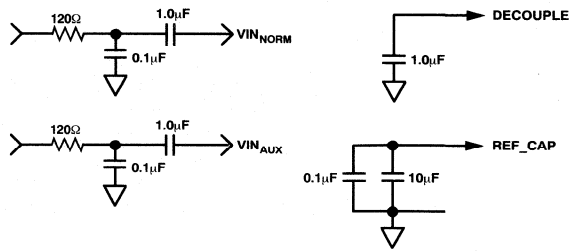


Figure 29. Analog Test Conditions

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time, $t_{MEASURED}$, is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

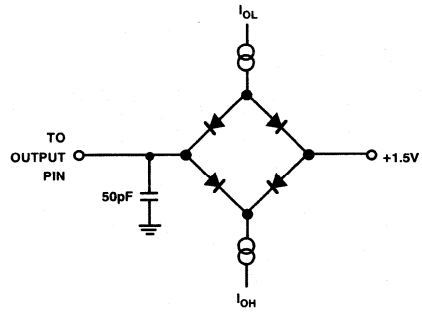


Figure 30. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

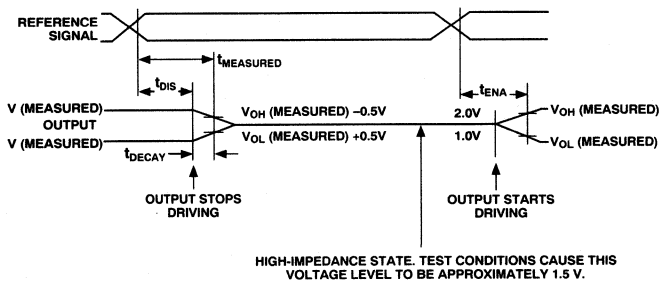
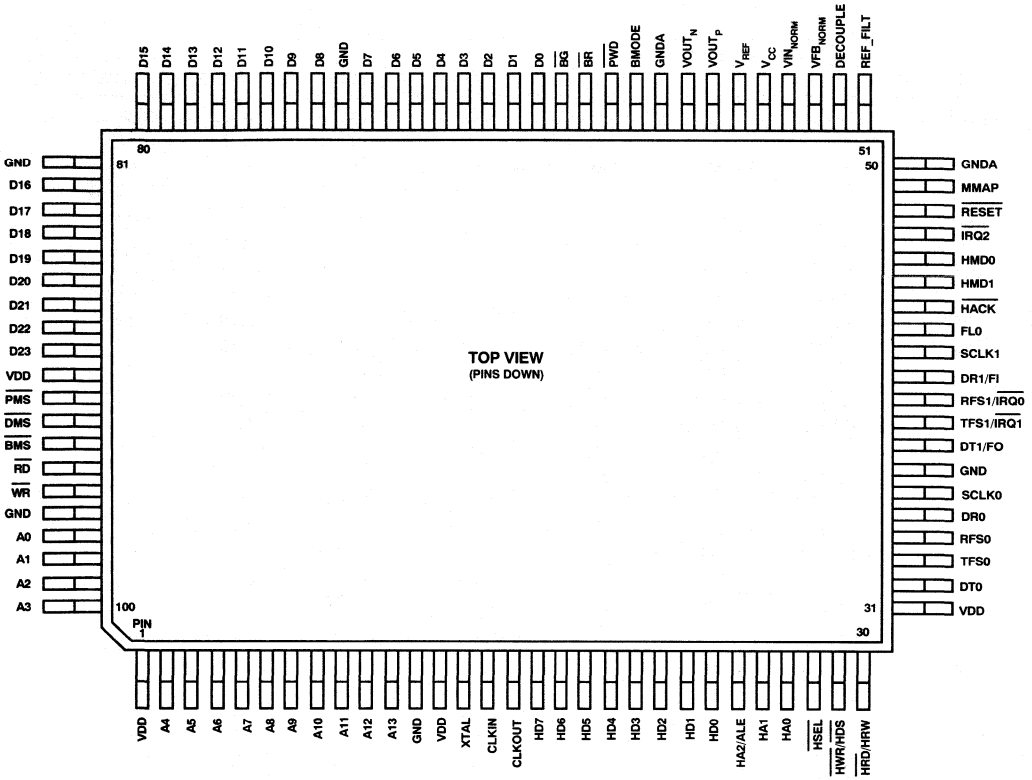


Figure 31. Output Enable/Disable

100-Lead PQFP Pinout



PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME	PQFP NUMBER	PIN NAME
1	VDD	26	HA1	51	REF_FILT	76	D11
2	A4	27	HA0	52	VINAUX	77	D12
3	A5	28	$\overline{\text{HSEL}}$	53	DECOUPLE	78	D13
4	A6	29	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	54	VINNORM	79	D14
5	A7	30	$\overline{\text{HRD}}$/HRW	55	VCC	80	D15
6	A8	31	VDD	56	VREF	81	GND
7	A9	32	DT0	57	VOUTP	82	D16
8	A10	33	TFS0	58	VOUTN	83	D17
9	A11	34	RFS0	59	GNDA	84	D18
10	A12	35	DR0	60	BMODE	85	D19
11	A13	36	SCLK0	61	$\overline{\text{PWD}}$	86	D20
12	GND	37	GND	62	$\overline{\text{BR}}$	87	D21
13	VDD	38	DT1/FO	63	$\overline{\text{BG}}$	88	D22
14	XTAL	39	TFS1/$\overline{\text{IRQ1}}$	64	D0	89	D23
15	CLKIN	40	RFS1/$\overline{\text{IRQ0}}$	65	D1	90	VDD
16	CLKOUT	41	DR1/FI	66	D2	91	$\overline{\text{PMS}}$
17	HD7	42	SCLK1	67	D3	92	$\overline{\text{DMS}}$
18	HD6	43	FL0	68	D4	93	$\overline{\text{BMS}}$
19	HD5	44	$\overline{\text{HACK}}$	69	D5	94	$\overline{\text{RD}}$
20	HD4	45	HMD1	70	D6	95	$\overline{\text{WR}}$
21	HD3	46	HMD0	71	D7	96	GND
22	HD2	47	$\overline{\text{IRQ2}}$	72	GND	97	A0
23	HD1	48	$\overline{\text{RESET}}$	73	D8	98	A1
24	HD0	49	MMAP	74	D9	99	A2
25	HA2/ALE	50	GNDA	75	D10	100	A3

144-Pin PGA Pinout

PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME	PGA NUMBER	PIN NAME
D3	NC	N4	VINAUX	M13	NC	C12	NC
C2	NC	P3	DECOUPLE	N14	NC	B13	VDD
B1	NC	R2	VINNORM	P15	NC	A14	A4
D2	NC	P4	NC	M14	NC	B12	HD10
E3	VDD	N5	VCC	L13	PWDACK	C11	A5
C1	DT0	R3	VREF	N15	NC	A13	HD9
E2	TFS0	P5	VOUTP	L14	GND	B11	A6
D1	RFS0	R4	VOUTN	M15	D16	A12	HD8
F3	NC	N6	GNDA	K13	D17	C10	A7
F2	DR0	P6	BMODE	K14	D18	B10	A8
E1	SCLK0	R5	NC	L15	D19	A11	A9
G2	GND	P7	$\overline{\text{PWD}}$	J14	D20	B9	A10
G3	DT1/FO	N7	NC	J13	D21	C9	A11
F1	NC	R6	NC	K15	D22	A10	A12
G1	TFS1/$\overline{\text{IRQ1}}$	R7	NC	J15	D23	A9	A13
H2	NC	P8	$\overline{\text{BR}}$	H14	VDD	B8	GND
H1	RFS1/$\overline{\text{IRQ0}}$	R8	NC	H15	VDD	A8	GND
H3	NC	N8	$\overline{\text{BG}}$	H13	HSIZE	C8	VDD
J3	DR1/FI	N9	NC	G13	$\overline{\text{PMS}}$	C7	XTAL
J1	SCLK1	R9	D0	G15	$\overline{\text{DMS}}$	A7	NC
K1	FL0	R10	D1	F15	$\overline{\text{BMS}}$	A6	CLKIN
J2	FL1	P9	D2	G14	$\overline{\text{RD}}$	B7	CLKOUT
K2	FL2	P10	D3	F14	$\overline{\text{WR}}$	B6	HD7
K3	$\overline{\text{HACK}}$	N10	D4	F13	GND	C6	HD6
L1	HMD1	R11	D5	E15	GND	A5	HD5
L2	HMD0	P11	D6	E14	HD15	B5	HD4
M1	$\overline{\text{IRQ2}}$	R12	D7	D15	A0	A4	HD3
N1	NC	R13	GND	C15	HD14	A3	HD2
M2	$\overline{\text{RESET}}$	P12	D8	D14	A1	B4	HD1
L3	NC	N11	D9	E13	HD13	C5	HD0
N2	MMAP	P13	D10	C14	A2	B3	HA2/ALE
P1	NC	R14	D11	B15	HD12	A2	HA1
M3	GNDA	N12	D12	D13	A3	C4	HA0
N3	NC	N13	D13	C13	HD11	C3	$\overline{\text{HSEL}}$
P2	NC	P14	D14	B14	NC	B2	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$
R1	REF_FILT	R15	D15	A15	NC	A1	$\overline{\text{HRD}}$/HWR

INDEX D4
NC = NO CONNECT

144-Lead PGA Pinout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
R	REF_FILT	VIN NORM	VREF	VOUT N	NC	NC	NC	NC	D0	D1	D5	D7	GND	D11	D15	R
P	NC	NC	DE-COUPLE	NC	VOUT P	B MODE	$\overline{PWD}$	$\overline{BR}$	D2	D3	D6	D8	D10	D14	NC	P
N	NC	MMAP	NC	VIN AUX	V_{CC}	GNDA	NC	$\overline{BG}$	NC	D4	D9	D12	D13	NC	NC	N
M	$\overline{IRQ2}$	$\overline{RESET}$	GNDA										NC	NC	D16	M
L	HMD1	HMD0	NC										PWD ACK	GND	D19	L
K	FL0	FL2	$\overline{HACK}$										D17	D18	D22	K
J	SCLK1	FL1	DR1/FI										D21	D20	D23	J
H	$\overline{RFS1}$/IRQ0	NC	NC										HSIZE	V_{DD}	V_{DD}	H
G	$\overline{TFS1}$/IRQ1	GND	DT1/FO										$\overline{PMS}$	$\overline{RD}$	$\overline{DMS}$	G
F	NC	DR0	NC										GND	$\overline{WR}$	$\overline{BMS}$	F
E	SCLK0	TFS0	V_{DD}										HD13	HD15	GND	E
D	RFS0	NC	NC	INDEX (NC)									A3	A1	A0	D
C	DT0	NC	$\overline{HSEL}$	HA0	HD0	HD6	XTAL	V_{DD}	A11	A7	A5	NC	HD11	A2	HD14	C
B	NC	$\overline{HWR}$/$\overline{HDS}$	HA2/ALE	HD1	HD4	HD7	CLK OUT	GND	A10	A8	A6	HD10	V_{DD}	NC	HD12	B
A	$\overline{HRD}$/HRW	HA1	HD2	HD3	HD5	CLKIN	NC	GND	A13	A12	A9	HD8	HD9	A4	NC	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

PGA PACKAGE
BOTTOM VIEW
(PINS UP)

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
R	D15	D11	GND	D7	D5	D1	D0	NC	NC	NC	NC	VOUT N	VREF	VIN NORM	REF_FILT	R
P	NC	D14	D10	D8	D6	D3	D2	$\overline{BR}$	$\overline{PWD}$	B MODE	VOUT P	NC	DE-COUPLE	NC	NC	P
N	NC	NC	D13	D12	D9	D4	NC	$\overline{BG}$	NC	GNDA	V_{CC}	VIN AUX	NC	MMAP	NC	N
M	D16	NC	NC										GNDA	$\overline{RESET}$	$\overline{IRQ2}$	M
L	D19	GND	PWD ACK										NC	HMD0	HMD1	L
K	D22	D18	D17										$\overline{HACK}$	FL2	FL0	K
J	D23	D20	D21										DR1/FI	FL1	SCLK1	J
H	V_{DD}	V_{DD}	HSIZE										NC	NC	$\overline{RFS1}$/IRQ0	H
G	$\overline{DMS}$	$\overline{RD}$	$\overline{PMS}$										DT1/FO	GND	$\overline{TFS1}$/IRQ1	G
F	$\overline{BMS}$	$\overline{WR}$	GND										NC	DR0	NC	F
E	GND	HD15	HD13										V_{DD}	TFS0	SCLK0	E
D	A0	A1	A3									INDEX (NC)	NC	NC	RFS0	D
C	HD14	A2	HD11	NC	A5	A7	A11	V_{DD}	XTAL	HD6	HD0	HA0	$\overline{HSEL}$	NC	DT0	C
B	HD12	NC	V_{DD}	HD10	A6	A8	A10	GND	CLK OUT	HD7	HD4	HD1	HA2/ALE	$\overline{HWR}$/$\overline{HDS}$	NC	B
A	NC	A4	HD9	HD8	A9	A12	A13	GND	NC	CLKIN	HD5	HD3	HD2	HA1	$\overline{HRD}$/HRW	A
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

PGA PACKAGE
TOP VIEW
(PINS DOWN)

NC = NO CONNECT

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option*
ADSP-21msp50AKG-52	0°C to +70°C	13	144-Pin Grid Array	G-144A
ADSP-21msp55AKS-52	0°C to +70°C	13	100-Lead PQFP	S-100
ADSP-21msp56AKS-52	0°C to +70°C	13	100-Lead PQFP	S-100
ADSP-21msp55ABS-52	−40°C to +85°C	13	100-Lead PQFP	S-100
ADSP-21msp56ABS-52	−40°C to +85°C	13	100-Lead PQFP	S-100

*G = Ceramic Pin Grid Array; S = Plastic Quad Flatpack. For outline information see Package Information section.

ANALOG DEVICES

ADSP-2100 Family DSP Microcomputers

ADSP-21xx

SUMMARY

16-Bit Fixed-Point DSP Microprocessors with On-Chip Memory
Enhanced Harvard Architecture for Three-Bus Performance: Instruction Bus & Dual Data Buses
Independent Computation Units: ALU, Multiplier/ Accumulator, and Shifter
Single-Cycle Instruction Execution & Multifunction Instructions
On-Chip Program Memory RAM or ROM & Data Memory RAM
Integrated I/O Peripherals: Serial Ports, Timer, Host Interface Port (ADSP-2111 Only)

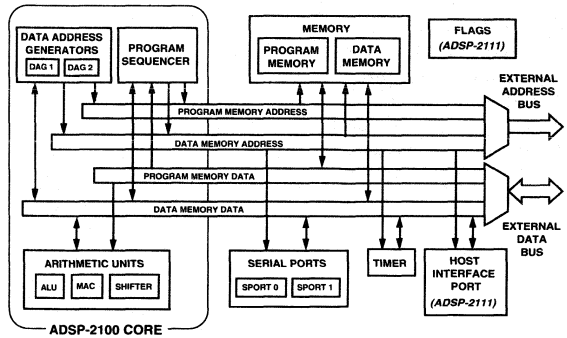
FEATURES

20 MIPS, 50 ns Maximum Instruction Rate
Separate On-Chip Buses for Program and Data Memory
Program Memory Stores Both Instructions and Data (Three-Bus Performance)
Dual Data Address Generators with Modulo and Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory (e.g., EPROM)
Double-Buffered Serial Ports with Companding Hardware, Automatic Data Buffering, and Multichannel Operation
ADSP-2111 Host Interface Port Provides Easy Interface to 68000, 80C51, ADSP-21xx, Etc.
Automatic Booting of ADSP-2111 Program Memory Through Host Interface Port
Three Edge- or Level-Sensitive Interrupts
Low Power IDLE Instruction
PGA, PLCC, PQFP, and TQFP Packages
MIL-STD-883B Versions Available

GENERAL DESCRIPTION

The ADSP-2100 Family processors are single-chip microcomputers optimized for digital signal processing (DSP) and other high speed numeric processing applications. The ADSP-21xx processors are all built upon a common core, the ADSP-2100. Each processor combines the core DSP architecture—computation units, data address generators, and program sequencer—with differentiating features such as on-chip program and data memory RAM, a programmable timer, one or two serial ports, and, on the ADSP-2111, a host interface port.

FUNCTIONAL BLOCK DIAGRAM



This data sheet describes the following ADSP-2100 Family processors:

ADSP-2101	
ADSP-2103	*3.3 V Version of ADSP-2101*
ADSP-2105	*Low Cost DSP*
ADSP-2111	*DSP with Host Interface Port*
ADSP-2115	
ADSP-2161/62/63/64	*Custom ROM-programmed DSPs*

The following ADSP-2100 Family processors are *not* included in this data sheet:

ADSP-2100A	*DSP Microprocessor*
ADSP-2165/66	*ROM-programmed ADSP-216x processors with powerdown and larger on-chip memories (12K Program Memory ROM, 1K Program Memory RAM, 4K Data Memory RAM)*
ADSP-21msp5x	*Mixed-Signal DSP Processors with integrated on-chip A/D and D/A plus powerdown*
ADSP-2171	*Speed and feature enhanced ADSP-2100 Family processor with host interface port, powerdown, and instruction set extensions for bit manipulation, multiplication, biased rounding, and global interrupt masking*
ADSP-2181	*Newest ADSP-21xx processor with ADSP-2171 features plus 80K bytes of on-chip RAM configured as 16K words of program memory and 16K words of data memory.*

Refer to the individual data sheet of each of these processors for further information.

ADSP-21xx

Fabricated in a high speed, submicron, double-layer metal CMOS process, the highest-performance ADSP-21xx processors operate at 20 MHz with a 50 ns instruction cycle time. Every instruction executes in a single cycle. Fabrication in CMOS results in low power dissipation.

The ADSP-2100 Family's flexible architecture and comprehensive instruction set support a high degree of parallelism. In one cycle the ADSP21xx can perform all of the following operations:

- Generate the next program address
- Fetch the next instruction
- Perform one or two data moves
- Update one or two data address pointers
- Perform a computation
- Receive and transmit data via one or two serial ports
- Receive and/or transmit data via the host interface port (ADSP-2111 only)

The ADSP-2101, ADSP-2105, and ADSP-2115 comprise the basic set of processors of the family. Each of these three devices contains program and data memory RAM, an interval timer, and one or two serial ports. The ADSP-2103 is a 3.3 volt power supply version of the ADSP-2101; it is identical to the ADSP-2101 in all other characteristics. Table I shows the features of each ADSP-21xx processor.

The ADSP-2111 adds a 16-bit host interface port (HIP) to the basic set of ADSP-21xx integrated features. The host port provides a simple interface to host microprocessors or microcontrollers such as the 8031, 68000, or ISA bus.

Table I. ADSP-21xx Processor Features

Feature	2101	2103	2105	2115	2111
Data Memory (RAM)	1K	1K	½K	½K	1K
Program Memory (RAM)	2K	2K	1K	1K	2K
Timer	●	●	●	●	●
Serial Port 0 (Multichannel)	●	●	–	●	●
Serial Port 1	●	●	●	●	●
Host Interface Port	–	–	–	–	●
Speed Grades *(Instruction Cycle Time)*					
10.24 MHz *(97.6 ns)*	–	●	–	–	–
12.5 MHz *(80 ns)*	●	–	–	–	–
13.0 MHz *(76.9 ns)*	–	–	–	–	●
13.824 MHz *(72.3 ns)*	–	–	●	●	–
16.67 MHz *(60 ns)*	●	–	–	●	●
20.0 MHz *(50 ns)*	●	–	–	●	●
Supply Voltage	5 V	3.3 V	5 V	5 V	5 V
Packages					
68-Pin PGA	●	–	–	–	–
68-Lead PLCC	●	●	●	●	–
80-Lead PQFP	●	●	–	●	–
80-Lead TQFP	–	–	–	●	–
100-Pin PGA	–	–	–	–	●
100-Lead PQFP	–	–	–	–	●
Temperature Grades					
K *Commercial* 0°C to +70°C	●	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●	●
T *Extended* –55°C to +125°C	●	–	–	–	●

Table II. ADSP-216x ROM-Programmed Processor Features

Feature	2161	2162	2163	2164
Data Memory (RAM)	½K	½K	½K	½K
Program Memory (ROM)	8K	8K	4K	4K
Program Memory (RAM)	–	–	–	–
Timer	●	●	●	●
Serial Port 0 (Multichannel)	●	●	●	●
Serial Port 1	●	●	●	●
Supply Voltage	5 V	3.3 V	5 V	3.3 V
Speed Grades *(Instruction Cycle Time)*				
10.24 MHz *(97.6 ns)*	–	●	–	●
16.67 MHz *(60 ns)*	●	–	●	–
Packages				
68-Lead PLCC	●	●	●	●
80-Lead PQFP	●	●	●	●
Temperature Grades				
K *Commercial* 0°C to +70°C	●	●	●	●
B *Industrial* –40°C to +85°C	●	●	●	●

The ADSP-216x series are memory-variant versions of the ADSP-2101 and ADSP-2103 that contain factory-programmed on-chip ROM program memory. These devices offer different amounts of on-chip memory for program and data storage. Table II shows the features available in the ADSP-216x series of custom ROM-coded processors.

The ADSP-216x products eliminate the need for an external boot EPROM in your system, and can also eliminate the need for any external program memory by fitting the entire application program in on-chip ROM. These devices thus provide an excellent option for volume applications where board space and system cost constraints are of critical concern.

Development Tools

The ADSP-21xx processors are supported by a complete set of tools for system development. The ADSP-2100 Family Development Software includes C and assembly language tools that allow programmers to write code for any of the ADSP-21xx processors. The ANSI C compiler generates ADSP-21xx assembly source code, while the runtime C library provides ANSI-standard and custom DSP library routines. The ADSP-21xx assembler produces object code modules which the linker combines into an executable file. The processor simulators provide an interactive instruction-level simulation with a reconfigurable, windowed user interface. A PROM splitter utility generates PROM programmer compatible files.

EZ-ICE® in-circuit emulators allow debugging of ADSP-21xx systems by providing a full range of emulation functions such as modification of memory and register values and execution breakpoints. EZ-LAB® demonstration boards are complete DSP systems that execute EPROM-based programs.

Additional details and ordering information is available in the *ADSP-2100 Family Software & Hardware Development Tools* data sheet (ADDS-21xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

Additional Information

This data sheet provides a general overview of ADSP-21xx processor functionality. For detailed design information on the architecture and instruction set, refer to the *ADSP-2100 Family User's Manual*, available from both Prentice Hall and Analog Devices.

ARCHITECTURE OVERVIEW

Figure 1 shows a block diagram of the ADSP-21xx architecture. The processors contain three independent computational units: the ALU, the multiplier/accumulator (MAC), and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add, and multiply/subtract operations. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient use of these computational units. The sequencer supports conditional jumps, subroutine calls, and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-21xx executes looped code with zero overhead—no explicit jump instructions are required to maintain the loop.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers. The circular buffering feature is also used by the serial ports for automatic data transfers to (and from) on-chip memory.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA, DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD, DMD) share a single external data bus. The $\overline{\text{BMS}}$, $\overline{\text{DMS}}$, and $\overline{\text{PMS}}$ signals indicate which memory space the external buses are being used for.

Program memory can store both instructions and data, permitting the ADSP-21xx to fetch two operands in a single cycle, one from program memory and one from data memory. The processor can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of the processor's buses with the use of the bus request/grant signals ($\overline{\text{BR}}$, $\overline{\text{BG}}$).

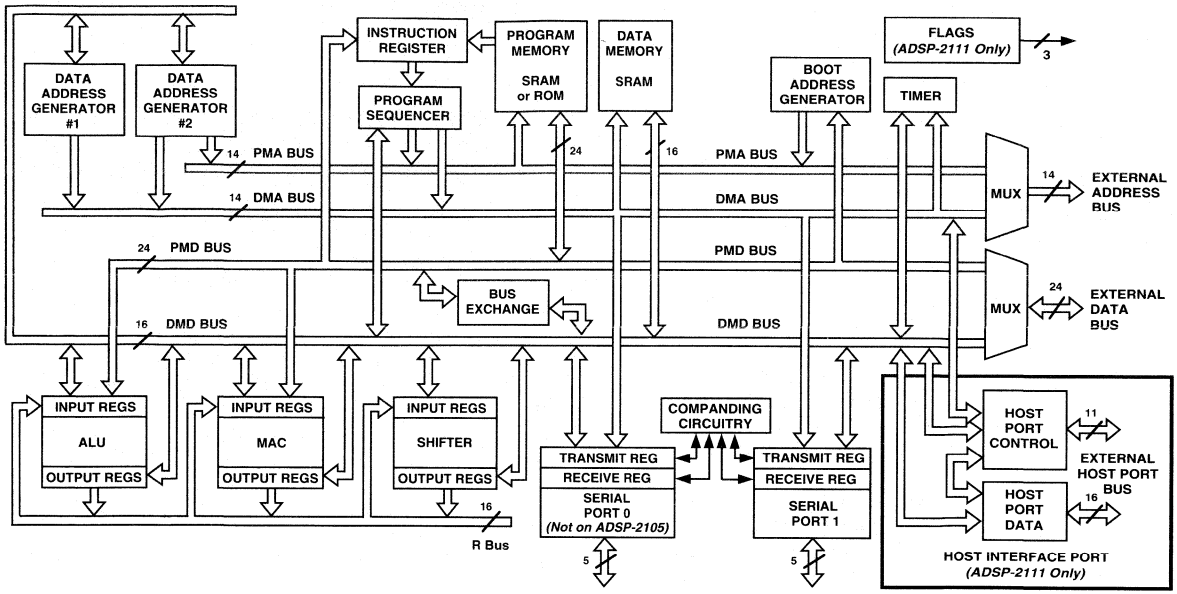


Figure 1. ADSP-21xx Block Diagram

One bus grant execution mode allows the ADSP-21xx to continue running from internal memory. A second execution mode requires the processor to halt while buses are granted.

Each ADSP-21xx processor can respond to several different interrupts. There can be up to three external interrupts, configured as edge- or level-sensitive. Internal interrupts can be generated by the timer, serial ports, and, on the ADSP-2111, the host interface port. There is also a master $\overline{\text{RESET}}$ signal.

Booting circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, three wait states are automatically generated. This allows, for example, a 60 ns ADSP-2101 to use a 200 ns EPROM as external boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware.

The data receive and transmit pins on SPORT1 (Serial Port 1) can be alternatively configured as a general-purpose input flag and output flag. You can use these pins for event signalling to and from an external device. The ADSP-2111 has three additional flag outputs whose states are controlled through software.

A programmable interval timer can generate periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* cycles, where *n–1* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-21xx processors include two synchronous serial ports ("SPORTs") for serial communications and multiprocessor communication. All of the ADSP-21xx processors have two serial ports (SPORT0, SPORT1) except for the ADSP-2105, which has only SPORT1.

The serial ports provide a complete synchronous serial interface with optional companding in hardware. A wide variety of framed or frameless data transmit and receive modes of operation are available. Each SPORT can generate an internal programmable serial clock or accept an external serial clock.

Each serial port has a 5-pin interface consisting of the following signals:

Signal Name	Function
SCLK	Serial Clock (I/O)
RFS	Receive Frame Synchronization (I/O)
TFS	Transmit Frame Synchronization (I/O)
DR	Serial Data Receive
DT	Serial Data Transmit

The ADSP-21xx serial ports offer the following capabilities:

Bidirectional—Each SPORT has a separate, double-buffered transmit and receive function.

Flexible Clocking—Each SPORT can use an external serial clock or generate its own clock internally.

Flexible Framing—The SPORTs have independent framing for the transmit and receive functions; each function can run in a frameless mode or with frame synchronization signals internally generated or externally generated; frame sync signals may be active high or inverted, with either of two pulse widths and timings.

Different Word Lengths—Each SPORT supports serial data word lengths from 3 to 16 bits.

Companding in Hardware—Each SPORT provides optional A-law and μ-law companding according to CCITT recommendation G.711.

Flexible Interrupt Scheme—Receive and transmit functions can generate a unique interrupt upon completion of a data word transfer.

Autobuffering with Single-Cycle Overhead—Each SPORT can automatically receive or transmit the contents of an entire circular data buffer with only one overhead cycle per data word; an interrupt is generated after the transfer of the entire buffer is completed.

Multichannel Capability (SPORT0 Only)—SPORT0 provides a multichannel interface to selectively receive or transmit a 24-word or 32-word, time-division multiplexed serial bit stream; this feature is especially useful for T1 or CEPT interfaces, or as a network communication scheme for multiple processors. (Note that the ADSP-2105 includes only SPORT1, not SPORT0, and thus does not offer multichannel operation.)

Alternate Configuration—SPORT1 can be alternatively configured as two external interrupt inputs ($\overline{IRQ0}$, $\overline{IRQ1}$) and the Flag In and Flag Out signals (FI, FO).

Host Interface Port (ADSP-2111)

The ADSP-2111 includes a Host Interface Port (HIP), a parallel I/O port that allows easy connection to a host processor. Through the HIP, the ADSP-2111 can be accessed by the host processor as a memory-mapped peripheral. The host interface port can be thought of as an area of dual-ported memory, or mailbox registers, that allows communication between the computational core of the ADSP-2111 and the host computer. The host interface port is completely asynchronous. The host processor can write data into the HIP while the ADSP-2111 is operating at full speed.

Three pins configure the HIP for operation with different types of host processors. The HSIZE pin configures HIP for 8- or 16-bit communication with the host processor. HMD0 configures the bus strobes, selecting either separate read and write strobes or a single read/write select and a host data strobe. HMD1 selects either separate address (3-bit) and data (16-bit) buses or a multiplexed 16-bit address/data bus with address latch enable. Tying these pins to appropriate values configures the ADSP-2111 for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

The HIP contains six data registers (HDR5-0) and two status registers (HSR7-6) with an associated HMASK register for masking interrupts from individual HIP data registers. The HIP data registers are memory-mapped in the internal data memory of the ADSP-2111. The two status registers provide status information to both the ADSP-2111 and the host processor. HSR7 contains a software reset bit which can be set by both the ADSP-2111 and the host.

HIP transfers can be managed using either interrupts or polling. The HIP generates an interrupt whenever an HDR register receives data from a host processor write. It also generates an interrupt when the host processor has performed a successful read of any HDR. The read/write status of the HDRs is also stored in the HSR registers.

The HMASK register bits can be used to mask the generation of read or write interrupts from individual HDR registers. Bits in the IMASK register enable and disable all HIP read interrupts or all HIP write interrupts. So, for example, a write to HDR4 will cause an interrupt only if both the *HDR4 Write* bit in HMASK and the *HIP Write* interrupt enable bit in IMASK are set.

The HIP provides a second method of booting the ADSP-2111 in which the host processor loads instructions into the HIP. The ADSP-2111 automatically transfers the data, in this case opcodes, to internal program memory. The BMODE pin determines whether the ADSP-2111 boots from the host processor through the HIP or from external EPROM over the data bus.

Interrupts

The ADSP-21xx's interrupt controller lets the processor respond to interrupts with a minimum of overhead. Up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$, are provided. $\overline{IRQ2}$ is always available as a dedicated pin; $\overline{IRQ1}$ and $\overline{IRQ0}$ may be alternately configured as part of Serial Port 1. The ADSP-21xx also supports internal interrupts from the timer, the serial ports, and the host interface port (on the ADSP-2111). The interrupts are internally prioritized and individually maskable (except for $\overline{RESET}$ which is non-maskable). The $\overline{IRQx}$ input pins can be programmed for either level- or edge-sensitivity. The interrupt priorities for each ADSP-21xx processor are shown in Table III.

The ADSP-21xx uses a vectored interrupt scheme: when an interrupt is acknowledged, the processor shifts program control to the interrupt vector address corresponding to the interrupt received. Interrupts can be optionally nested so that a higher priority interrupt can preempt the currently executing interrupt service routine. Each interrupt vector location is four instructions in length so that simple service routines can be coded entirely in this space. Longer service routines require an additional JUMP or CALL instruction.

Individual interrupt requests are logically ANDed with the bits in the IMASK register; the highest-priority unmasked interrupt is then selected.

The interrupt control register, ICNTL, allows the external interrupts to be set as either edge- or level-sensitive. Depending on bit 4 in ICNTL, interrupt service routines can either be nested (with higher priority interrupts taking precedence) or be processed sequentially (with only one interrupt service active at a time).

The interrupt force and clear register, IFC, is a write-only register that contains a force bit and a clear bit for each interrupt (except for level-sensitive interrupts and the ADSP-2111 HIP interrupts—these cannot be forced or cleared in software).

When responding to an interrupt, the ASTAT, MSTAT, and IMASK status registers are pushed onto the status stack and the PC counter is loaded with the appropriate vector address. The status stack is seven levels deep (nine levels deep on the ADSP-2111) to allow interrupt nesting. The stack is automatically popped when a return from the interrupt instruction is executed.

Pin Definitions

Table IV (on next page) shows pin definitions for the ADSP-21xx processors. Any inputs not used must be tied to V_{DD}.

Table III. Interrupt Vector Addresses & Priority

ADSP-2105 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2101/2103/2115/216x Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
SPORT0 Transmit	0x0008
SPORT0 Receive	0x000C
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0010
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x0014
Timer	0x0018 *(Low Priority)*

ADSP-2111 Interrupt Source	**Interrupt Vector Address**
$\overline{\text{RESET}}$ Startup	0x0000
$\overline{\text{IRQ2}}$	0x0004 *(High Priority)*
HIP Write from Host	0x0008
HIP Read to Host	0x000C
SPORT0 Transmit	0x0010
SPORT0 Receive	0x0014
SPORT1 Transmit *or* $\overline{\text{IRQ1}}$	0x0018
SPORT1 Receive *or* $\overline{\text{IRQ0}}$	0x001C
Timer	0x0020 *(Low Priority)*

SYSTEM INTERFACE

Figure 3 shows a typical system for the ADSP-2101, ADSP-2115, or ADSP-2103, with two serial I/O devices, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable for the ADSP-2101 and ADSP-2103. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2115.

Figure 4 shows a system diagram for the ADSP-2105, with one serial I/O device, a boot EPROM, and optional external program and data memory. A total of 14.5K words of data memory and 15K words of program memory is addressable for the ADSP-2105.

Figure 5 shows a system diagram for the ADSP-2111, with two serial I/O devices, a host processor, a boot EPROM, and optional external program and data memory. A total of 15K words of data memory and 16K words of program memory is addressable.

Programmable wait-state generation allows the processors to easily interface to slow external memories.

The ADSP-2101, ADSP-2103, ADSP-2115, and ADSP-2111 processors also provide either: one external interrupt ($\overline{\text{IRQ2}}$) and two serial ports (SPORT0, SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) and one serial port (SPORT0).

The ADSP-2105 provides either: one external interrupt ($\overline{\text{IRQ2}}$) and one serial port (SPORT1), *or* three external interrupts ($\overline{\text{IRQ2}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ0}}$) with no serial port.

Clock Signals

The ADSP-21xx processors' CLKIN input may be driven by a crystal or by a TTL-compatible external clock signal. The CLKIN input may not be halted or changed in frequency during operation, nor operated below the specified low frequency limit.

If an external clock is used, it should be a TTL-compatible signal running at the instruction rate. The signal should be connected to the processor's CLKIN input; in this case, the XTAL input must be left unconnected.

Because the ADSP-21xx processors include an on-chip oscillator circuit, an external crystal may also be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 2. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

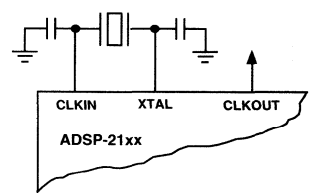


Figure 2. External Crystal Connections

A clock output signal (CLKOUT) is generated by the processor, synchronized to the processor's internal cycles.

Reset

The $\overline{\text{RESET}}$ signal initiates a complete reset of the ADSP-21xx. The $\overline{\text{RESET}}$ signal must be asserted when the chip is powered up to assure proper initialization. If the $\overline{\text{RESET}}$ signal is applied during initial power-up, it must be held long enough to allow the processor's internal clock to stabilize. If $\overline{\text{RESET}}$ is activated at any time after power-up and the input clock frequency does not change, the processor's internal clock continues and does not require this stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 t_{CK} cycles will ensure that the PLL has locked (this does not, however, include the crystal oscillator start-up time). During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

To generate the $\overline{\text{RESET}}$ signal, use either an RC circuit with an external Schmidt trigger or a commercially available reset IC. (Do not use only an RC circuit.)

Table IV. ADSP-21xx Pin Definitions

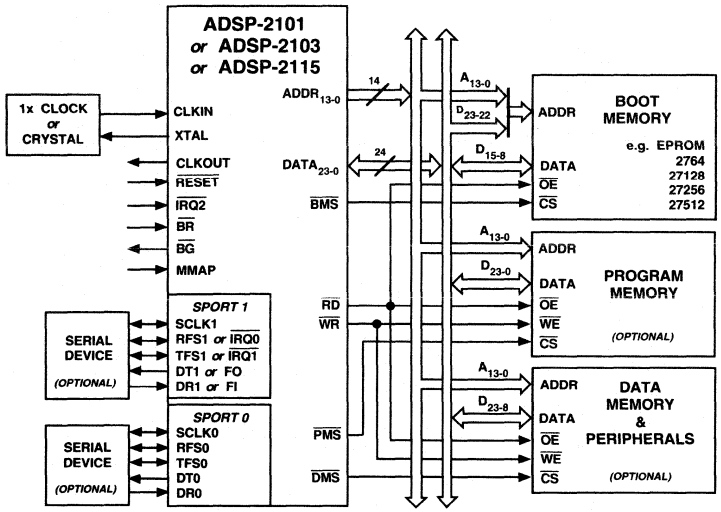
Pin Name(s)	# of Pins	Input / Output	Function
Address	14	O	Address outputs for program, data and boot memory.
Data[1]	24	I/O	Data I/O pins for program and data memories. Input only for boot memory, with two MSBs used for boot memory addresses. Unused data lines may be left floating.
$\overline{\text{RESET}}$	1	I	Processor Reset Input
$\overline{\text{IRQ2}}$	1	I	External Interrupt Request #2
$\overline{\text{BR}}$[2]	1	I	External Bus Request Input
$\overline{\text{BG}}$	1	O	External Bus Grant Output
$\overline{\text{PMS}}$	1	O	External Program Memory Select
$\overline{\text{DMS}}$	1	O	External Data Memory Select
$\overline{\text{BMS}}$	1	O	Boot Memory Select
$\overline{\text{RD}}$	1	O	External Memory Read Enable
$\overline{\text{WR}}$	1	O	External Memory Write Enable
MMAP	1	I	Memory Map Select Input
CLKIN, XTAL	2	I	External Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
V_{DD}			Power Supply Pins
GND			Ground Pins
SPORT0[3]	5	I/O	Serial Port 0 Pins *(TFS0, RFS0, DT0, DR0, SCLK0)*
SPORT1	5	I/O	Serial Port 1 Pins *(TFS1, RFS1, DT1, DR1, SCLK1)*
or Interrupts & Flags:			
$\overline{\text{IRQ0}}$ *(RFS1)*	1	I	External Interrupt Request #0
$\overline{\text{IRQ1}}$ *(TFS1)*	1	I	External Interrupt Request #1
FI *(DR1)*	1	I	Flag Input Pin
FO *(DT1)*	1	O	Flag Output Pin
FL2–0 *(ADSP-2111 Only)*	3	O	General Purpose Flag Output Pins
Host Interface Port (ADSP-2111 Only)			
$\overline{\text{HSEL}}$	1	I	HIP Select Input
$\overline{\text{HACK}}$	1	O	HIP Acknowledge Output
HSIZE	1	I	8/16-Bit Host Select *(0 = 16-Bit, 1 = 8-Bit)*
BMODE	1	I	Boot Mode Select *(0 = Standard EPROM Booting, 1 = HIP Booting)*
HMD0	1	I	Bus Strobe Select *(0 =* $\overline{\text{RD}}$/$\overline{\text{WR}}$*, 1 =* RW/$\overline{\text{DS}}$*)*
HMD1	1	I	HIP Address/Data Mode Select *(0 = Separate, 1 = Multiplexed)*
$\overline{\text{HRD}}$/HRW	1	I	HIP Read Strobe *or* Read/Write Select
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP Write Strobe *or* Host Data Strobe Select
HD15–0/HAD15-0	16	I/O	HIP Data *or* HIP Data and Address
HA2/ALE	1	I	Host Address 2 Input *or* Address Latch Enable Input
HA1–0/Unused	2	I	Host Address 1 and 0 Inputs

NOTES

[1]Unused data bus lines may be left floating.

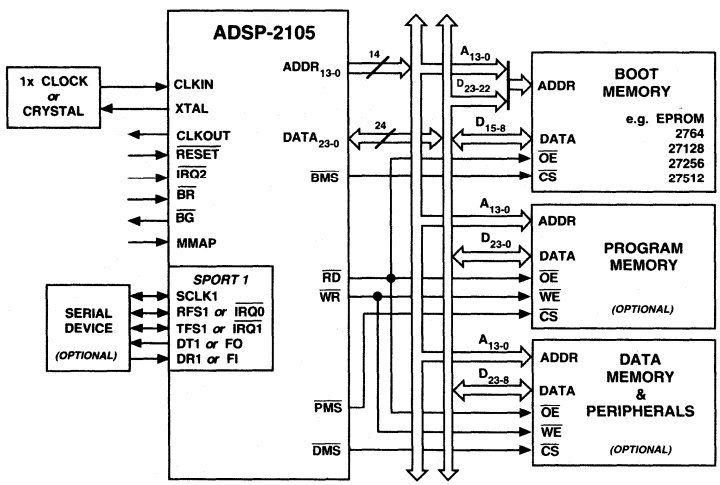
[2]$\overline{\text{BR}}$ must be tied high (to V_{DD}) if not used.

[3]ADSP-2105 does not have SPORT0. (SPORT0 pins are No Connects on the ADSP-2105.)



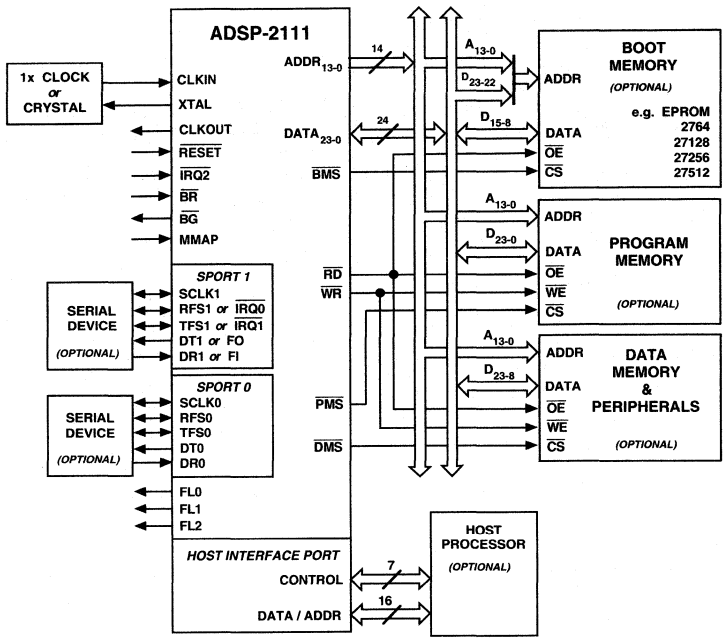
THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 3. ADSP-2101/ADSP-2103/ADSP-2115 System



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 4. ADSP-2105 System



THE TWO MSBs OF THE DATA BUS (D_{23-22}) ARE USED TO SUPPLY THE TWO MSBs OF THE BOOT MEMORY EPROM ADDRESS. THIS IS ONLY REQUIRED FOR THE 27256 AND 27512.

Figure 5. ADSP-2111 System

The $\overline{\text{RESET}}$ input resets all internal stack pointers to the empty stack condition, masks all interrupts, and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, the boot loading sequence is performed (provided there is no pending bus request and the chip is configured for booting, with MMAP = 0). The first instruction is then fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and on-chip program memory data bus (PMD) are multiplexed with the on-chip data memory buses (DMA, DMD), creating a single external data bus and a single external address bus. The external data bus is bidirectional and is 24 bits wide to allow instruction fetches from external program memory. Program memory may contain code and data.

The external address bus is 14 bits wide. For the ADSP-2101, ADSP-2103, and ADSP-2111, these lines can directly address up to 16K words, of which 2K are on-chip. For the ADSP-2105 and ADSP-2115, the address lines can directly address up to 15K words, of which 1K is on-chip.

The data lines are bidirectional. The program memory select ($\overline{\text{PMS}}$) signal indicates accesses to program memory and can be used as a chip select signal. The write ($\overline{\text{WR}}$) signal indicates a write operation and is used as a write strobe. The read ($\overline{\text{RD}}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-21xx processors write data from their 16-bit registers to 24-bit program memory using the PX register to provide the lower eight bits. When the processor reads 16-bit data from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{\text{RESET}}$.

Program Memory Maps

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 6 shows the two program memory maps for the ADSP-2101, ADSP-2103, and ADSP-2111. Figure 8 shows the program memory maps for the ADSP-2105 and ADSP-2115. Figures 7 and 9 show the program memory maps for the ADSP-2161/62 and ADSP-2163/64, respectively.

ADSP-2101/ADSP-2103/ADSP-2111

When MMAP = 0, on-chip program memory RAM occupies 2K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not booted although it can be written to and read under program control.

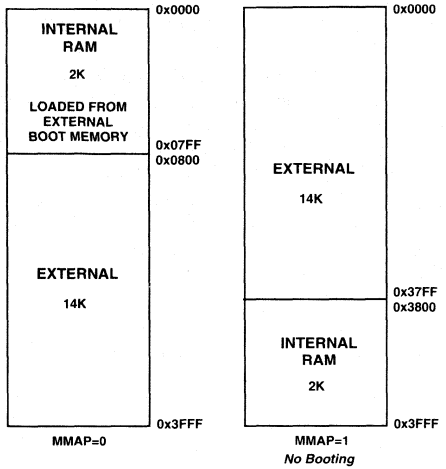


Figure 6. ADSP-2101/ADSP-2103/ADSP-2111 Program Memory Maps

ADSP-2105/ADSP-2115

When MMAP = 0, on-chip program memory RAM occupies 1K words beginning at address 0x0000. Off-chip program memory uses the remaining 14K words beginning at address 0x0800. In this configuration–when MMAP = 0–the boot loading sequence (described below in "Boot Memory Interface") is automatically initiated when $\overline{\text{RESET}}$ is released.

When MMAP = 1, 14K words of off-chip program memory begin at address 0x0000 and on-chip program memory RAM is located in the 1K words between addresses 0x3800–0x3BFF. In this configuration, program memory is not booted although it can be written to and read under program control.

2

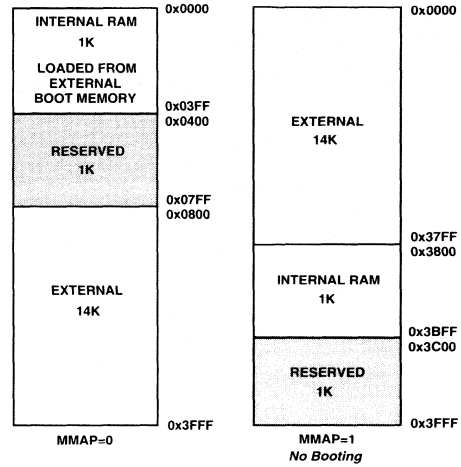


Figure 8. ADSP-2105/ADSP-2115 Program Memory Maps

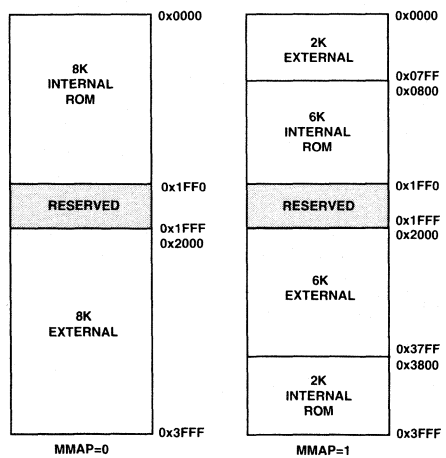


Figure 7. ADSP-2161/62 Program Memory Maps

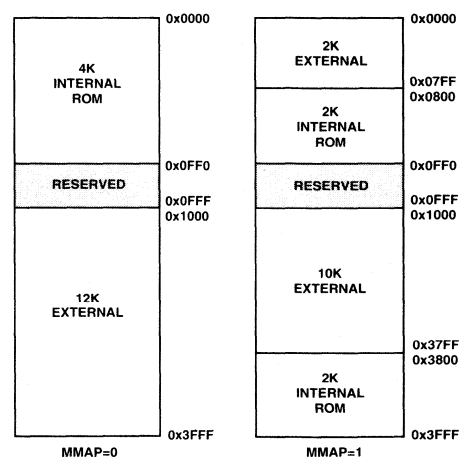


Figure 9. ADSP-2163/64 Program Memory Maps

Data Memory Interface
The data memory address bus (DMA) is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-21xx processors support memory-mapped I/O, with the peripherals memory-mapped into the data memory address space and accessed by the processor in the same manner as data memory.

Data Memory Map
ADSP-2101/ADSP-2103/ADSP-2111
For the ADSP-2101, ADSP-2103, and ADSP-2111, on-chip data memory RAM resides in the 1K words beginning at address 0x3800, as shown in Figure 10. Data memory locations from 0x3C00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

ADSP-2105/ADSP-2115
For the ADSP-2105 and ADSP-2115, on-chip data memory RAM resides in the 512 words beginning at address 0x3800, also shown in Figure 10. Data memory locations from 0x3A00 to the end of data memory at 0x3FFF are reserved. Control and status registers for the system, timer, wait-state configuration, and serial port operations are located in this region of memory.

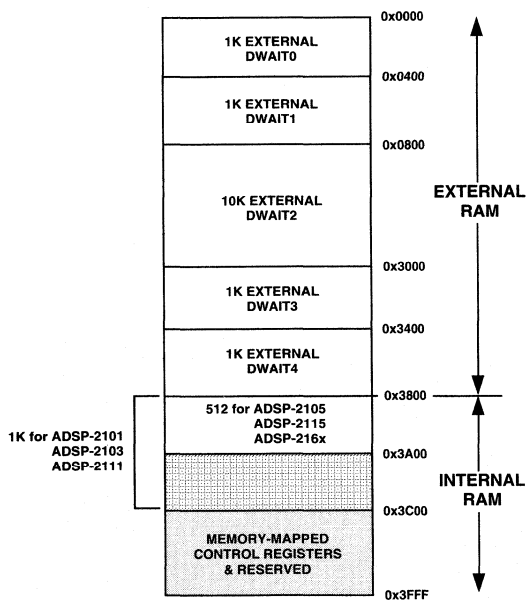


Figure 10. Data Memory Map (All Processors)

All Processors
The remaining 14K of data memory is located off-chip. This external data memory is divided into five zones, each associated with its own wait-state generator. This allows slower peripherals to be memory-mapped into data memory for which wait states are specified. By mapping peripherals into different zones, you can accommodate peripherals with different wait-state requirements. All zones default to seven wait states after $\overline{RESET}$.

Boot Memory Interface
On the ADSP-2101, ADSP-2103, and ADSP-2111, boot memory is an external 64K by 8 space, divided into eight separate 8K by 8 pages. On the ADSP-2105 and ADSP-2115, boot memory is a 32K by 8 space, divided into eight separate 4K by 8 pages. The 8-bit bytes are automatically packed into 24-bit instruction words by each processor, for loading into on-chip program memory.

Three bits in the processors' System Control Register select which page is loaded by the boot memory interface. Another bit in the System Control Register allows the forcing of a boot loading sequence under software control. Boot loading from Page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate zero to seven wait states; it defaults to three wait states after $\overline{RESET}$. This allows the ADSP-21xx to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8-D15. To accommodate up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot memory address: D23, D22, and A13 supply the boot page number.

The ADSP-2100 Family Assembler and Linker allow the creation of programs and data structures requiring multiple boot pages during execution.

The $\overline{BR}$ signal is recognized during the booting sequence. The bus is granted after loading the current byte is completed. $\overline{BR}$ during booting may be used to implement booting under control of a host processor.

Bus Interface
The ADSP-21xx processors can relinquish control of their data and address buses to an external device. When the external device requires control of the buses, it asserts the bus request signal ($\overline{BR}$). If the ADSP-21xx is not performing an external memory access, it responds to the active $\overline{BR}$ input in the next cycle by:

- Three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- Asserting the bus grant ($\overline{BG}$) signal,
- and halting program execution.

If the Go mode is set, however, the ADSP-21xx will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-21xx is performing an external memory access when the external device asserts the $\overline{BR}$ signal, it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the cycle after the access completes (up to eight cycles later depending on the number of wait states). The instruction does not need to be completed when the bus is granted; the ADSP-21xx will grant the bus in between two memory accesses if an instruction requires more than one external memory access.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, re-enables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active. If this feature is not used, the $\overline{BR}$ input should be tied high (to V_{DD}).

Low Power IDLE Instruction

The IDLE instruction places the ADSP-21xx processor in low power state in which it waits for an interrupt. When an interrupt occurs, it is serviced and execution continues with instruction following IDLE. Typically this next instruction will be a JUMP back to the IDLE instruction. This implements a low-power standby loop.

The *IDLE n* instruction is a special version of IDLE that slows the processor's internal clock signal to further reduce power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor, *n*, given in the IDLE instruction. The syntax of the instruction is:

IDLE n;

where *n* = 16, 32, 64, or 128.

The instruction leaves the chip in an idle state, operating at the slower rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and the timer clock, are reduced by the same ratio. Upon receipt of an enabled interrupt, the processor will stay in the IDLE state for up to a maximum of *n* CLKIN cycles, where *n* is the divisor specified in the instruction, before resuming normal operation.

When the *IDLE n* instruction is used, it slows the processor's internal clock and thus its response time to incoming interrupts–the 1-cycle response time of the standard IDLE state is increased by *n*, the clock divisor. When an enabled interrupt is received, the ADSP-21xx will remain in the IDLE state for up to a maximum of *n* CLKIN cycles (where *n* = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE n* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the IDLE state (a maximum of *n* CLKIN cycles).

ADSP-216x Prototyping

You can prototype your ADSP-216x system with either the ADSP-2101 or ADSP-2103 RAM-based processors. When code is fully developed and debugged, it can be submitted to Analog Devices for conversion into a ADSP-216x ROM product.

The ADSP-2101 EZ-ICE emulator can be used for development of ADSP-216x systems. For the 3.3 V ADSP-2162 and ADSP-2164, a voltage converter interface board provides 3.3 V emulation.

Additional overlay memory is used for emulation of ADSP-2161/62 systems. It should be noted that due to the use of off-chip overlay memory to emulate the ADSP-2161/62, a performance loss may be experienced when both executing instructions and fetching program memory data from the off-chip overlay memory in the same cycle. This can be overcome by locating program memory data in on-chip memory.

2

Ordering Procedure for ADSP-216x ROM Processors

To place an order for a custom ROM-coded ADSP-2161, ADSP-2162, ADSP-2163, or ADSP-2164 processor, you must:

1. Complete the following forms contained in the *ADSP ROM Ordering Package*, available from your Analog Devices sales representative:

   ADSP-216x ROM Specification Form
   ROM Release Agreement
   ROM NRE Agreement & Minimum Quantity Order (MQO) Acceptance Agreement for Pre-Production ROM Products

2. Return the forms to Analog Devices along with two copies of the Memory Image File (.EXE file) of your ROM code. The files must be supplied on two 3.5" or 5.25" floppy disks for the IBM PC (DOS 2.01 or higher).

3. Place a purchase order with Analog Devices for non-recurring engineering changes (NRE) associated with ROM product development.

After this information is received, it is entered into Analog Devices' ROM Manager System which assigns a custom ROM model number to the product. This model number will be branded on all prototype and production units manufactured to these specifications.

To minimize the risk of code being altered during this process, Analog Devices verifies that the .EXE files on both floppy disks are identical, and recalculates the checksums for the .EXE file entered into the ROM Manager System. The checksum data, in the form of a ROM Memory Map, a hard copy of the .EXE file, and a ROM Data Verification form are returned to you for inspection.

A signed ROM Verification Form and a purchase order for production units are required prior to any product being manufactured. Prototype units may be applied toward the minimum order quantity.

Upon completion of prototype manufacture, Analog Devices will ship prototype units and a delivery schedule update for production units. An invoice against your purchase order for the NRE charges is issued at this time.

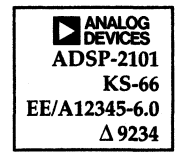
There is a charge for each ROM mask generated and a minimum order quantity. Consult your sales representative for details. A separate order must be placed for parts of a specific package type, temperature range, and speed grade.

Wafer Products
Some ADSP-21xx processors are also available in wafer form. Wafers allow the integration of DSP processors into hybrids, multichip modules, chip-on-board products, etc. For information about wafer product ordering, contact your Analog Devices sales representative.

Functional Differences for Older Revision Devices
Older revisions of the ADSP-21xx processors have slight differences in functionality. The two differences are as follows:

- Bus Grant ($\overline{BG}$) is asserted in the same cycle that Bus Request ($\overline{BR}$) is recognized (i.e. when setup and hold time requirements are met for the $\overline{BR}$ input). Bus Request input is a synchronous input rather than asynchronous. (In newer revision devices, $\overline{BG}$ is asserted in the cycle *after* $\overline{BR}$ is recognized.)
- Only the standard IDLE instruction is available, not the clock-reducing *IDLE n* instruction.

To determine the revision of a particular ADSP-21xx device, inspect the marking on the device. For example, an ADSP-2101 of revision 6.0 will have the following marking:



← *Package & Speed*
← *Lot # & Revision Code*
← *Date Code*

The revision codes for the older versions of each ADSP-21xx device are as follows:

Processor	Old Functionality	New Functionality
ADSP-2101	Revision Code ≤ 5.0	Revision Code ≥ 6.0
ADSP-2105	*No Revision Code*	Revision Code ≥ 1.0
ADSP-2115	Revision Code < 1.0	Revision Code ≥ 1.0
ADSP-2111	RevisionCode < 2.0	Revision Code ≥ 2.0
ADSP-2103	Revision code ≤ 5.0	Revision code ≥ 6.0

Instruction Set

The ADSP-21xx assembly language uses an algebraic syntax for ease of coding and readability. The sources and destinations of computations and data movements are written explicitly in each assembly statement, eliminating cryptic assembler mnemonics.

Every instruction assembles into a single 24-bit word and executes in a single cycle. The instructions encompass a wide variety of instruction types along with a high degree of operational parallelism. There are five basic categories of instructions: data move instructions, computational instructions, multifunction instructions, program flow control instructions and miscellaneous instructions. Multifunction instructions perform one or two data moves and a computation.

The instruction set is summarized below. The *ADSP-2100 Family Users Manual* contains a complete reference to the instruction set.

ALU Instructions

[IF cond]	AR|AF	=	xop + yop [+ C] ;	*Add/Add with Carry*
		=	xop – yop [+ C– 1] ;	*Subtract X – Y/Subtract X – Y with Borrow*
		=	yop – xop [+ C– 1] ;	*Subtract Y – X/Subtract Y – X with Borrow*
		=	xop AND yop ;	*AND*
		=	xop OR yop ;	*OR*
		=	xop XOR yop ;	*XOR*
		=	PASS xop ;	*Pass, Clear*
		=	– xop ;	*Negate*
		=	NOT xop ;	*NOT*
		=	ABS xop ;	*Absolute Value*
		=	yop + 1 ;	*Increment*
		=	yop – 1 ;	*Decrement*
		=	DIVS yop, xop ;	*Divide*
		=	DIVQ xop ;	

MAC Instructions

[IF cond]	MR|MF	=	xop * yop ;	*Multiply*
		=	MR + xop * yop ;	*Multiply/Accumulate*
		=	MR – xop * yop ;	*Multiply/Subtract*
		=	MR ;	*Transfer MR*
		=	0 ;	*Clear*
IF MV	SAT MR ;			*Conditional MR Saturation*

Shifter Instructions

[IF cond]	SR = [SR OR] ASHIFT xop ;	*Arithmetic Shift*
[IF cond]	SR = [SR OR] LSHIFT xop ;	*Logical Shift*
	SR = [SR OR] ASHIFT xop BY <exp>;	*Arithmetic Shift Immediate*
	SR = [SR OR] LSHIFT xop BY <exp>;	*Logical Shift Immediate*
[IF cond]	SE = EXP xop ;	*Derive Exponent*
[IF cond]	SB = EXPADJ xop ;	*Block Exponent Adjust*
[IF cond]	SR = [SR OR] NORM xop ;	*Normalize*

Data Move Instructions

reg = reg ;	*Register-to-Register Move*
reg = <data> ;	*Load Register Immediate*
reg = DM (<addr>) ;	*Data Memory Read (Direct Address)*
dreg = DM (Ix , My) ;	*Data Memory Read (Indirect Address)*
dreg = PM (Ix , My) ;	*Program Memory Read (Indirect Address)*
DM (<addr>) = reg ;	*Data Memory Write (Direct Address)*
DM (Ix , My) = dreg ;	*Data Memory Write (Indirect Address)*
PM (Ix , My) = dreg ;	*Program Memory Write (Indirect Address)*

Multifunction Instructions

<ALU>|<MAC>|<SHIFT> , dreg = dreg ;	*Computation with Register-to-Register Move*
<ALU>|<MAC>|<SHIFT> , dreg = DM (Ix , My) ;	*Computation with Memory Read*
<ALU>|<MAC>|<SHIFT> , dreg = PM (Ix , My) ;	*Computation with Memory Read*
DM (Ix , My) = dreg , <ALU>|<MAC>|<SHIFT> ;	*Computation with Memory Write*
PM (Ix , My) = dreg , <ALU>|<MAC>|<SHIFT> ;	*Computation with Memory Write*
dreg = DM (Ix , My) , dreg = PM (Ix , My) ;	*Data & Program Memory Read*
<ALU>|<MAC> , dreg = DM (Ix , My) , dreg = PM (Ix , My) ;	*ALU/MAC with Data & Program Memory Read*

Program Flow Instructions

DO <addr> [UNTIL term] ;	*Do Until Loop*
[IF cond] JUMP (Ix) ;	*Jump*
[IF cond] JUMP <addr>;	
[IF cond] CALL (Ix) ;	*Call Subroutine*
[IF cond] CALL <addr>;	
IF [NOT] FLAG_IN JUMP <addr>;	*Jump/Call on Flag In Pin*
IF [NOT] FLAG_IN CALL <addr>;	
[IF cond] SET|RESET|TOGGLE FLAG_OUT [, ...] ;	*Modify Flag Out Pin*
[IF cond] RTS ;	*Return from Subroutine*
[IF cond] RTI ;	*Return from Interrupt Service Routine*
IDLE [(n)] ;	*Idle*

Miscellaneous Instructions

NOP ;	*No Operation*
MODIFY (Ix , My);	*Modify Address Register*
[PUSH STS] [, POP CNTR] [, POP PC] [, POP LOOP] ;	*Stack Control*
ENA|DIS SEC_REG [, ...] ;	*Mode Control*
BIT_REV	
AV_LATCH	
AR_SAT	
M_MODE	
TIMER	
G_MODE	

Notation Conventions

Ix	Index registers for indirect addressing
My	Modify registers for indirect addressing
<data>	Immediate data value
<addr>	Immediate address value
<exp>	Exponent (shift value) in shift immediate instructions (8-bit signed number)
<ALU>	Any ALU instruction (except divide)
<MAC>	Any multiply-accumulate instruction
<SHIFT>	Any shift instruction (except shift immediate)
cond	Condition code for conditional instruction
term	Termination code for DO UNTIL loop
dreg	Data register (of ALU, MAC, or Shifter)
reg	Any register (including dregs)
;	A semicolon terminates the instruction
,	Commas separate multiple operations of a single instruction
[ ]	Optional part of instruction
[, ...]	Optional, multiple operations of an instruction
option1 | option2	List of options; choose one.

Assembly Code Example

The following example is a code fragment that performs the filter tap update for an adaptive filter based on a least-mean-squared algorithm. Notice that the computations in the instructions are written like algebraic equations.

```
        MF=MX0*MY1(RND), MX0=DM(I2,M1);        {MF=error*beta}
        MR=MX0*MF(RND), AY0=PM(I6,M5);
        DO adapt UNTIL CE;
           AR=MR1+AY0, MX0=DM(I2,M1), AY0=PM(I6,M7);
adapt:     PM(I6,M6)=AR, MR=MX0*MF(RND);

        MODIFY(I2,M3);                         {Point to oldest data}
        MODIFY(I6,M7);                         {Point to start of data}
```

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	–55	+125	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

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Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[8]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[6]		10	µA
C_I	Input Pin Capacitance[1, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 8, 9, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0 (not on ADSP-2105).
[3]Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0 (not on ADSP-2105), SCLK0 (not on ADSP-2105), RFS0 (not on ADSP-2105), TFS0 (not on ADSP-2105).
[5]Input-only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0 (not on ADSP-2105).
[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[7]Although specified for TTL outputs, all ADSP-21xx outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[8]Guaranteed but not tested.
[9]Applies to PGA, PLCC, PQFP package types.
[10]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . –55°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (10 sec) PGA . . . . . +300°C
Lead Temperature (5 sec) PLCC, PQFP, TQFP . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADSP-21xx processors feature proprietary ESD protection circuitry to dissipate high energy electrostatic discharges (Human Body Model), permanent damage may occur to devices subjected to such discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before the devices are removed. Per method 3015 of MIL-STD-883, the ADSP-21xx processors have been classified as Class 1 devices.

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2101/2161/2163)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		58	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		51	mA
		@ V_{DD} = max, t_{CK} = 80 ns[2]		45	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 80 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
For typical supply current (internal power dissipation) figures, see Figure 11.

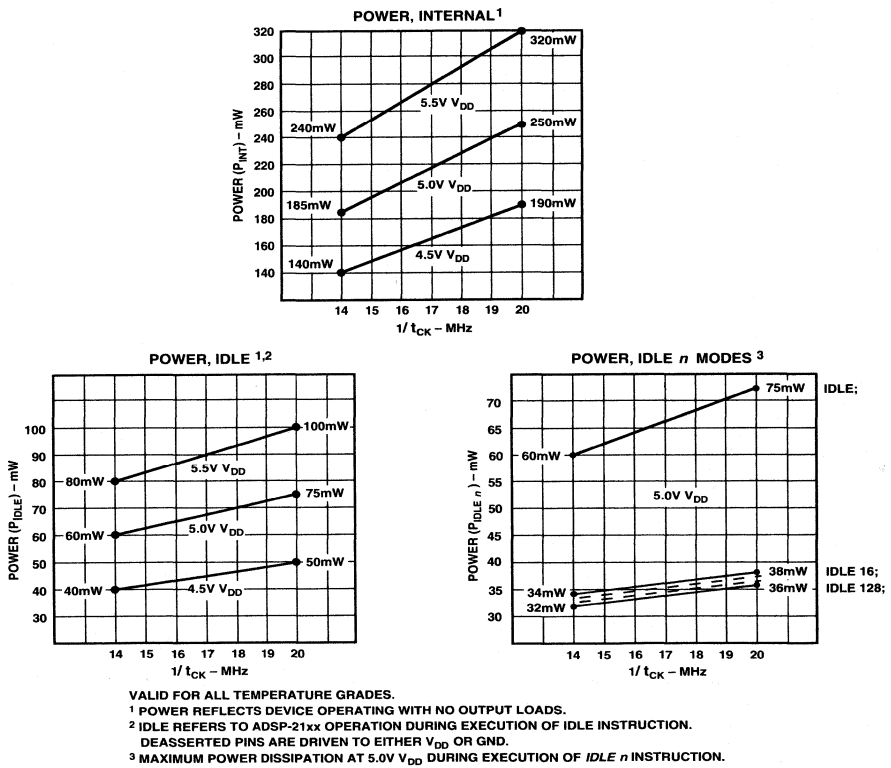


Figure 11. ADSP-2101 Power (Typical) vs. Frequency

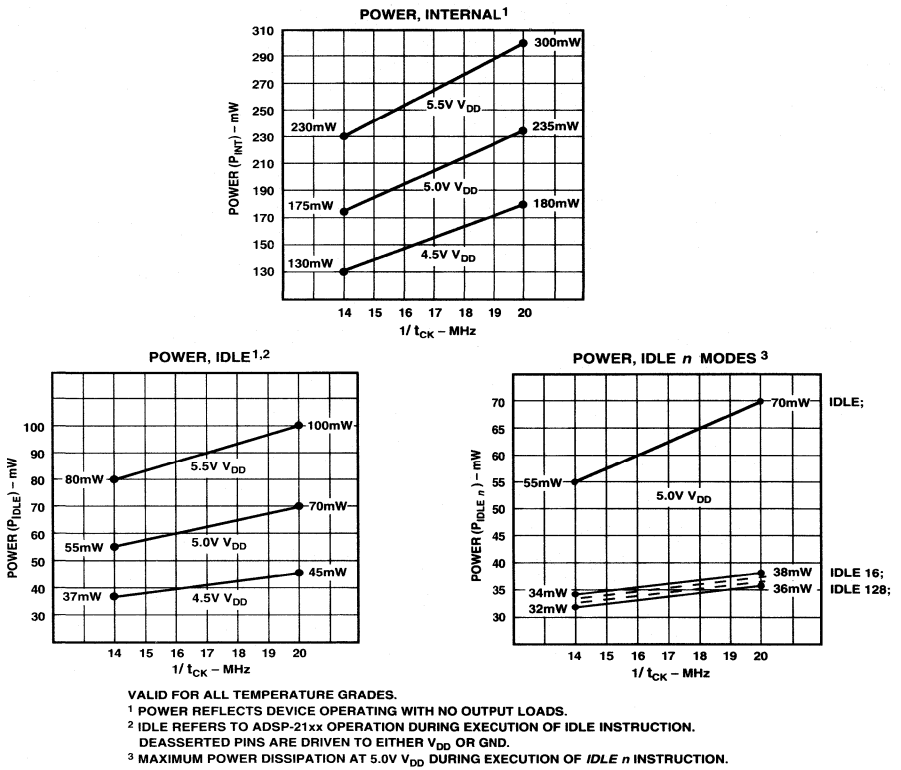
SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2115)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		55	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		48	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns[2]		42	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 72.3 ns		14	mA

2

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
For typical supply current (internal power dissipation) figures, see Figure 12.



VALID FOR ALL TEMPERATURE GRADES.
[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
[3] MAXIMUM POWER DISSIPATION AT 5.0V V_{DD} DURING EXECUTION OF *IDLE n* INSTRUCTION.

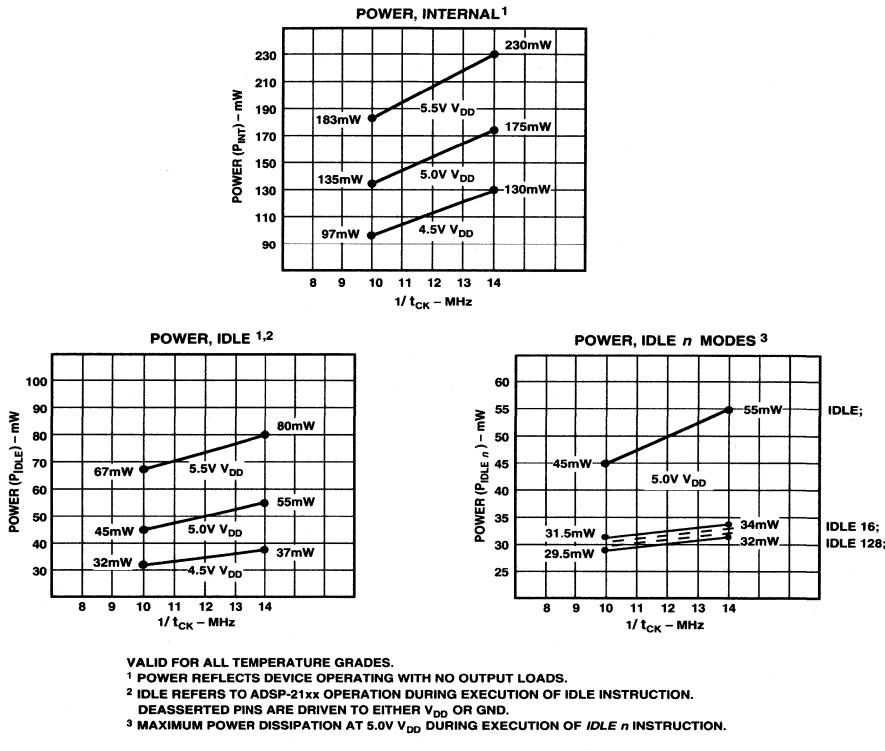
Figure 12. ADSP-2115 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

SUPPLY CURRENT & POWER (ADSP-2105)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 72.3 ns[2]		42	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 72.3 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
For typical supply current (internal power dissipation) figures, see Figure 13.



VALID FOR ALL TEMPERATURE GRADES.
[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] IDLE REFERS TO ADSP-21xx OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
[3] MAXIMUM POWER DISSIPATION AT 5.0V V_{DD} DURING EXECUTION OF *IDLE n* INSTRUCTION.

Figure 13. ADSP-2105 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an ADSP-2101 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

Total Power Dissipation = $P_{INT} + (C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation (from Figure 11).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz	= 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz	= 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz	= 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz	= 5.0 mW
					70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	18°C/W	9°C/W	9°C/W
PLCC	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W
TQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 14 and 15 show capacitive loading characteristics for the ADSP-2101, ADSP-2105, ADSP-2115, and ADSP-2161/2163.

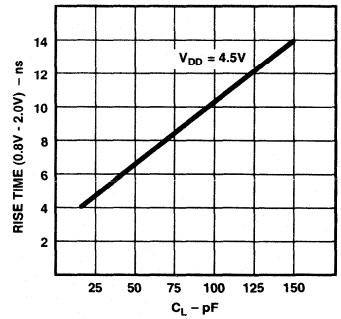


Figure 14. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

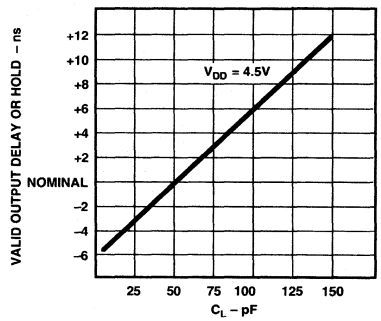


Figure 15. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2101/2105/2115/2161/2163)

TEST CONDITIONS

Figure 16 shows voltage reference levels for ac measurements.

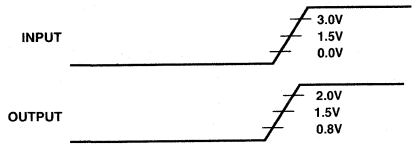


Figure 16. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 17. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 17. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

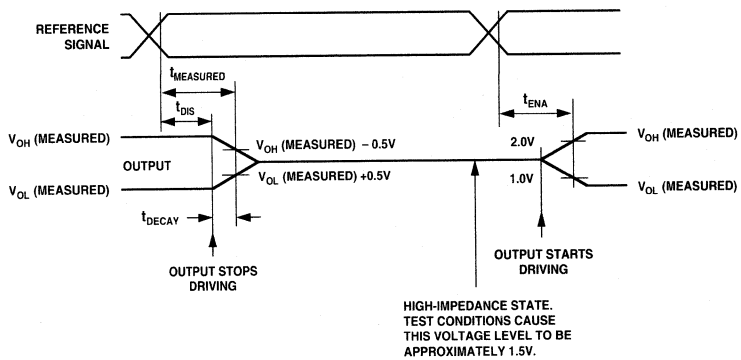


Figure 17. Output Enable/Disable

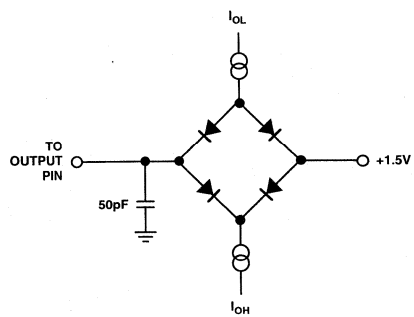


Figure 18. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

ADSP-2111–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	–55	+125	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

2

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[3, 5]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[8]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[2, 3, 7]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0V		10	µA
I_{OZH}	Tristate Leakage Curren[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[6]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0V[6]		10	µA
C_I	Input Pin Capacitance[1, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 8, 9, 10]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES

[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HRW, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1-0.

[2]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0, $\overline{\text{HACK}}$, FL2-0.

[3]Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0, HD0–HD15/HAD0–HAD15.

[4]Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0, HD0–HD15/HAD0–HAD15.

[5]Input-only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HRW, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, HA2/ALE, HA1-0.

[6]0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).

[7]Although specified for TTL outputs, all ADSP-2111 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[8]Guaranteed but not tested.

[9]Applies to ADSP-2111 PGA and PQFP packages.

[10]Output pin capacitance is the capacitive load for any three-stated output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... 0.3 V to +7 V
Input Voltage ..... –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) ...–55°C to +125°C
Storage Temperature Range .....–65°C to +150°C
Lead Temperature (10 sec) PGA ..... +300°C
Lead Temperature (5 sec) PQFP ..... +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (ADSP-2111)

SUPPLY CURRENT & POWER (ADSP-2111)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 50 ns[2]		60	mA
		@ V_{DD} = max, t_{CK} = 60 ns[2]		52	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns[2]		46	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 50 ns		18	mA
		@ V_{DD} = max, t_{CK} = 60 ns		16	mA
		@ V_{DD} = max, t_{CK} = 76.9 ns		14	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.

For typical supply current (internal power dissipation) figures, see Figure 19.

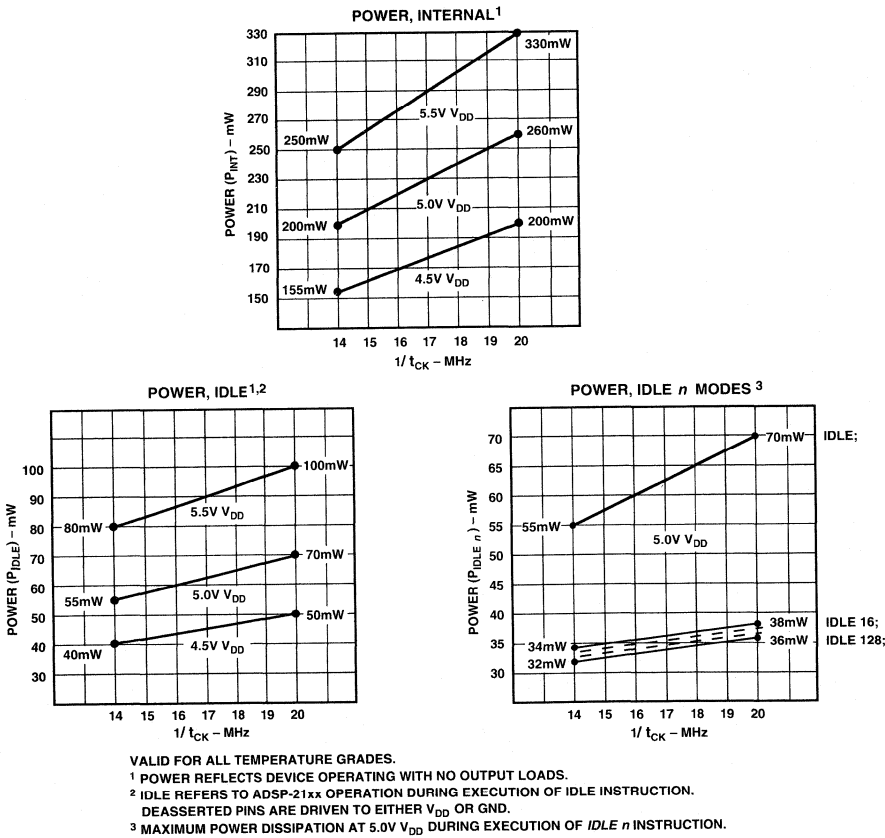


Figure 19. ADSP-2111 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2111)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an ADSP-2111 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 50 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 19).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 20 MHz = 40.0 mW
Data, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 10 MHz = 22.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 10 MHz = 2.5 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 20 MHz = 5.0 mW
				70.0 mW

Total power dissipation for this example = P_{INT} + 70.0 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	35°C/W	18°C/W	17°C/W
PQFP	42°C/W	18°C/W	23°C/W

CAPACITIVE LOADING

Figures 20 and 21 show capacitive loading characteristics for the ADSP-2111.

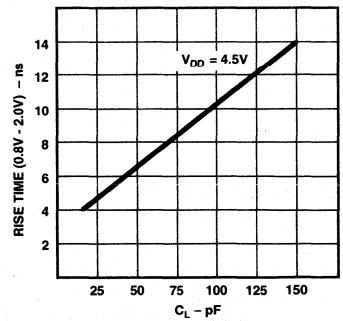


Figure 20. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

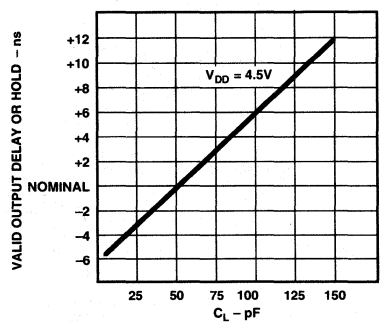


Figure 21. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

SPECIFICATIONS (ADSP-2111)

TEST CONDITIONS

Figure 22 shows voltage reference levels for ac measurements.

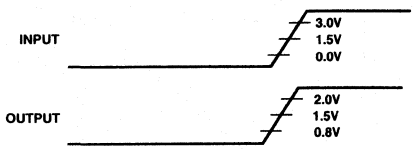


Figure 22. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 23. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 23. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

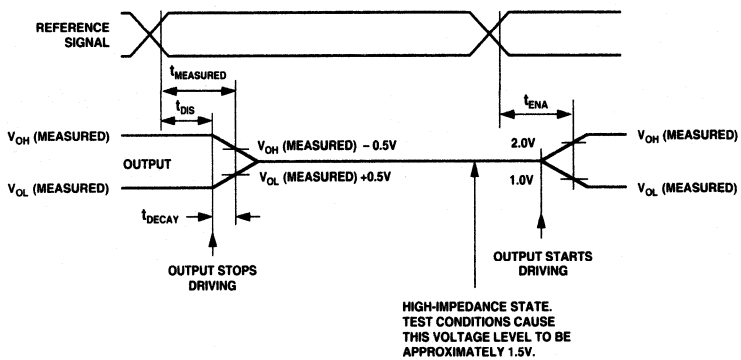


Figure 23. Output Enable/Disable

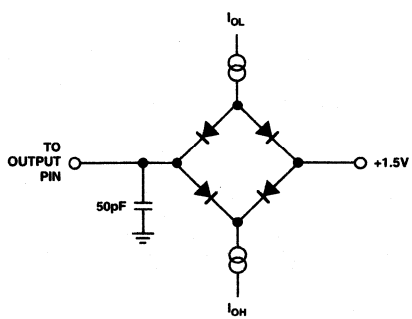


Figure 24. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	3.00	3.60	3.00	3.60	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 3]	@ V_{DD} = max	2.0		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.4	V
V_{OH}	Hi-Level Output Voltage[2, 3, 6]	@ V_{DD} = min, I_{OH} = –0.5 mA[6]	2.4		V
V_{OL}	Lo-Level Output Voltage[2, 3, 6]	@ V_{DD} = min, I_{OL} = 2 mA[6]		0.4	V
I_{IH}	Hi-Level Input Current[1]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[1]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max[5]		10	µA
I_{OZL}	Tristate Leakage Current[4]	@ V_{DD} = max, V_{IN} = 0 V[5]		10	µA
C_I	Input Pin Capacitance[1, 7, 8]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[4, 7, 8, 9]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES
[1]Input-only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR1, DR0.
[2] Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, A0–A13, CLKOUT, DT1, DT0.
[3] Bidirectional pins: D0–D23, SCLK1, RFS1, TFS1, SCLK0, RFS0, TFS0.
[4] Tristatable pins: A0–A13, D0–D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT1, SCLK1, RSF1, TFS1, DT0, SCLK0, RFS0, TFS0.
[5] 0 V on $\overline{\text{BR}}$, CLKIN Active (to force tristate condition).
[6] All ADSP-2103, ADSP-2162, and ADSP-2164 outputs are CMOS and will drive to V_{DD} and GND with no dc loads.
[7] Guaranteed but not tested.
[8] Applies to PLCC and PQFP package types.
[9]Output pin capacitance is the capacitive load for any three-stated output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +4.5 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) PLCC, PQFP . . . . . +280°C

*Stresses greater than those listed above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SPECIFICATIONS (ADSP-2103/2162/2164)

SUPPLY CURRENT & POWER (ADSP-2103/2162/2164)

Parameter		Test Conditions	Min	Max	Unit
I_{DD}	Supply Current (Dynamic)[1]	@ V_{DD} = max, t_{CK} = 97.6 ns[2]		20	mA
I_{DD}	Supply Current (Idle)[1, 3]	@ V_{DD} = max, t_{CK} = 97.6 ns		6	mA

NOTES
[1]Current reflects device operating with no output loads.
[2]V_{IN} = 0.4 V and 2.4 V.
[3]Idle refers to ADSP-21xx state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
For typical supply current (internal power dissipation) figures, see Figure 25.

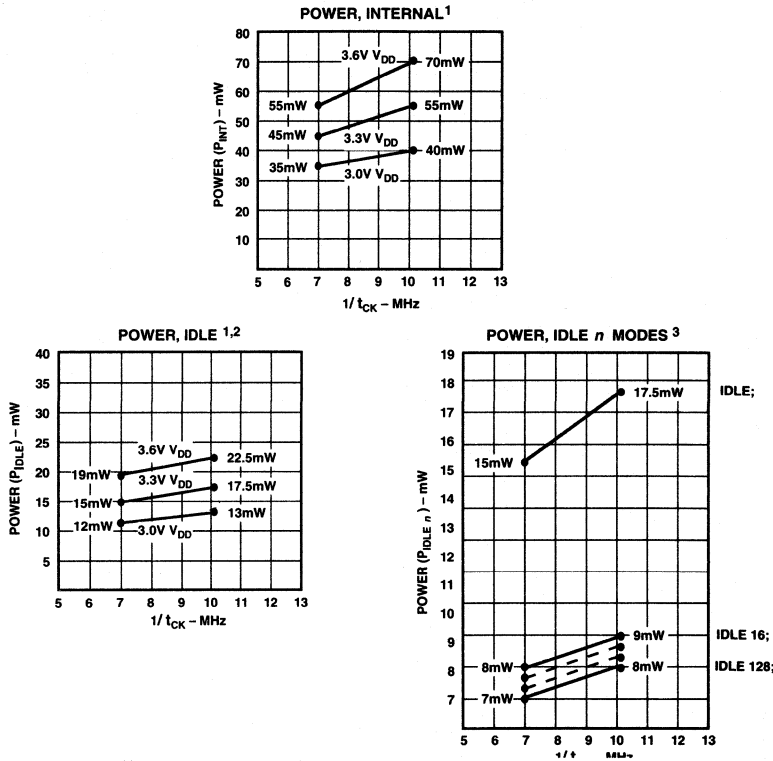


Figure 25. ADSP-2103 Power (Typical) vs. Frequency

SPECIFICATIONS (ADSP-2103/2162/2164)

POWER DISSIPATION EXAMPLE

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an ADSP-2103 application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 3.3 V and t_{CK} = 100 ns.

$$\textit{Total Power Dissipation} = P_{INT} + (C \times V_{DD}^2 \times f)$$

P_{INT} = internal power dissipation (from Figure 25).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

Output	# of Pins	× C	× V_{DD}^2	× f	
Address, $\overline{DMS}$	8	× 10 pF	× 3.3² V	× 10 MHz	= 8.71 mW
Data, $\overline{WR}$	9	× 10 pF	× 3.3² V	× 5 MHz	= 4.90 mW
$\overline{RD}$	1	× 10 pF	× 3.3² V	× 5 MHz	= 0.55 mW
CLKOUT	1	× 10 pF	× 3.3² V	× 10 MHz	= 1.09 mW
					15.25 mW

Total power dissipation for this example = P_{INT} + 15.25 mW.

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
PGA	27°C/W	16°C/W	11°C/W
PQFP	60°C/W	18°C/W	42°C/W

CAPACITIVE LOADING

Figures 26 and 27 show capacitive loading characteristics for the ADSP-2103, ADSP-2162, and ADSP-2164.

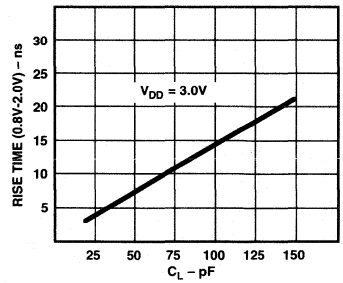


Figure 26. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

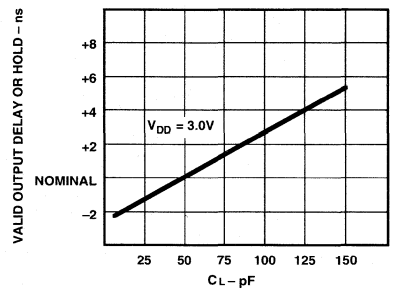


Figure 27. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Figure 28 shows voltage reference levels for ac measurements.

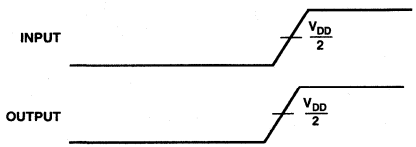


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in Figure 29. The time $t_{MEASURED}$ is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage.

The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \times 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in Figure 29. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

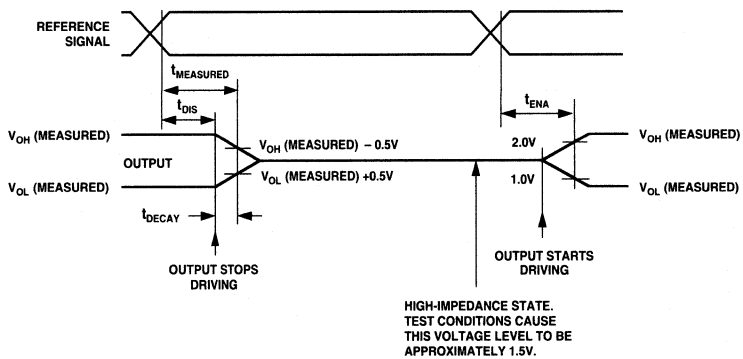


Figure 29. Output Enable/Disable

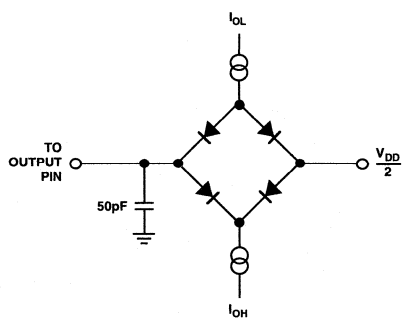


Figure 30. Equivalent Device Loading for AC Measurements (Except Output Enable/Disable)

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Device Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

CLOCK SIGNALS & RESET

Parameter		13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{CK}	CLKIN Period	72.3	150	60	150	50	150			ns
t_{CKL}	CLKIN Width Low	20		20		20				ns
t_{CKH}	CLKIN Width High	20		20		20				ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	361.5		300		250		$5t_{CK}$[1]		ns
Switching Characteristic:										
t_{CPL}	CLKOUT Width Low	26.2		20		15		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	26.2		20		15		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	0	20	0	20			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles, assuming stable CLKIN (not including crystal oscillator startup time).

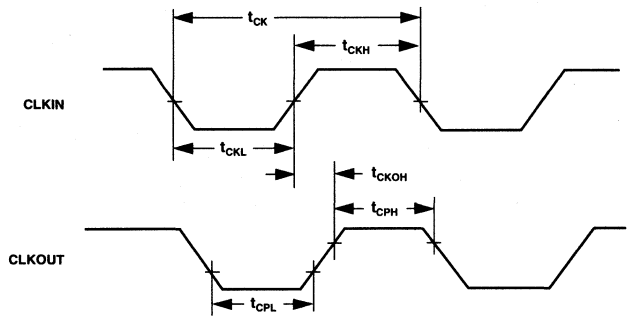


Figure 31. Clock Signals

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

INTERRUPTS & FLAGS

Parameter		13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	33.1		30		27.5		$0.25t_{CK} + 15$[4]		ns
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low (ADSP-2111)[2, 3]	36.1		33		30.5		$0.25t_{CK} + 18$[4]		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	18.1		15		12.5		$0.25t_{CK}$		ns
Switching Characteristic:										
t_{FOH}	FO Hold after CLKOUT High[5]	0		0		0				ns
t_{FOD}	FO Delay from CLKOUT High		15		15		15			ns

NOTES
[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.
[4]t_{IFS} (min) = $0.25t_{CK}$ + 20 ns for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).
[5]t_{FOH} (min) = –5 ns for ADSP-2111TG-52 and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

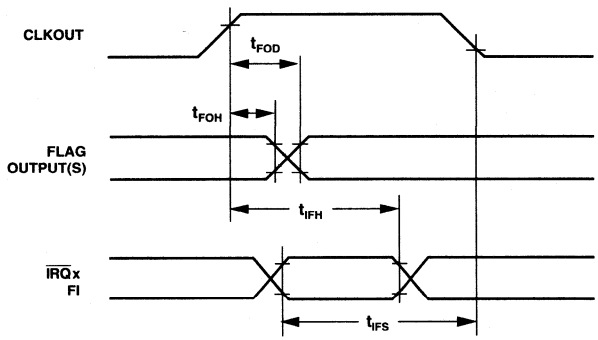


Figure 32. Interrupts & Flags

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

BUS REQUEST/GRANT

Parameter		13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	23.1		20		17.5		$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	38.1		35		32.5		$0.25t_{CK}$ + 20		ns
Switching Characteristic:										
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		38.1		35		32.5		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		0		0				ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		0		0				ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	8.1		5		2.5		$0.25t_{CK}$ – 10		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

Section 10.2.4, "Bus Request/Grant," on page 212 of the *ADSP-2100 Family User's Manual (1st Edition, 1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

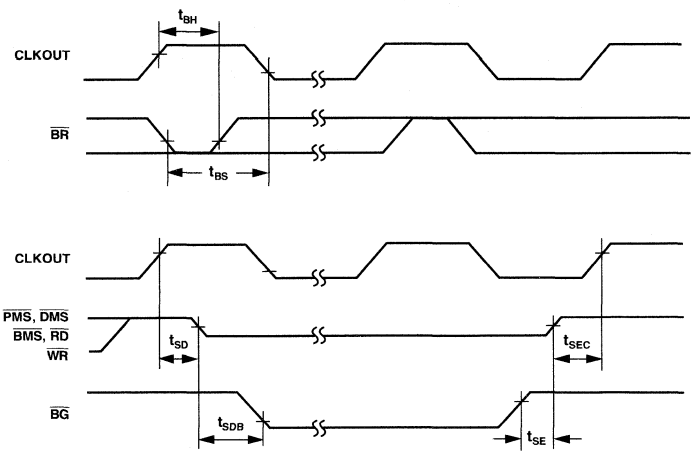


Figure 33. Bus Request/Grant

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY READ

Parameter		13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	Unit
Timing Requirement:								
t_{RDD}	$\overline{RD}$ Low to Data Valid		21.2		15		10	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		34.2		25		17.5	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		0		0		ns
Switching Characteristic:								
t_{RP}	$\overline{RD}$ Pulse Width	31.2		25		20		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	13.1	28.1	10	25	7.5	22.5	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	6.1		3		3.5		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	8.1		5		4.5		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	31.2		25		20		ns

Parameter		Frequency Dependency (CLKIN ≤ 16.67 MHz) Min	Frequency Dependency (CLKIN ≤ 16.67 MHz) Max	Frequency Dependency (16.67 MHz < CLKIN ≤ 20 MHz) Min	Frequency Dependency (16.67 MHz < CLKIN ≤ 20 MHz) Max	Unit
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid	$0.5t_{CK} - 15 + w$		$0.5t_{CK} - 15 + w$		ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid	$0.75t_{CK} - 20 + w$		$0.75t_{CK} - 20 + w$		ns
t_{RDH}	Data Hold from $\overline{RD}$ High					
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$[1]		$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$[2]	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 12$		$0.25t_{CK} - 9$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 10$		$0.25t_{CK} - 8$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		$0.5t_{CK} - 5$		ns

w = wait states × t_{CK}.

NOTES

[1]t_{RP} (min) = $0.5t_{CK} - 8 + w$ for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[2]t_{CRD} (max) = $0.25t_{CK} + 12$ for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

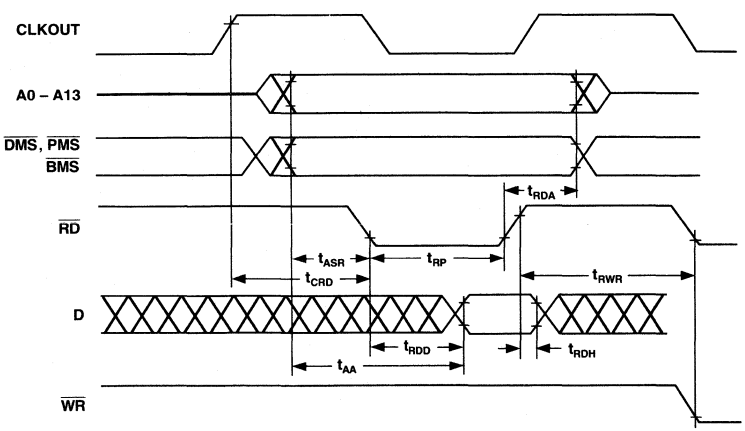


Figure 34. Memory Read

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

MEMORY WRITE

Parameter		13.824 MHz Min	13.824 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	Unit
Switching Characteristic:								
t_{DW}	Data Setup before $\overline{WR}$ High	26.2		20		15		ns
t_{DH}	Data Hold after $\overline{WR}$ High	8.1		5		4.5		ns
t_{WP}	$\overline{WR}$ Pulse Width	31.2		25		20		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		0		0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	6.1		3		3.5		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	8.1		5		2.5		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	13.1	28.1	10	25	7.5	22.5	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	39.2		30		22.5		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	8.1		5		4.5		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	31.2		25		20		ns

Parameter		Frequency Dependency (CLKIN ≤ 16.67 MHz) Min	Frequency Dependency (CLKIN ≤ 16.67 MHz) Max	Frequency Dependency (16.67 MHz < CLKIN ≤ 20 MHz) Min	Frequency Dependency (16.67 MHz < CLKIN ≤ 20 MHz) Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 10 + w$		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 10$		$0.25t_{CK} - 8$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5 + w$[1]		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled					
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 12$		$0.25t_{CK} - 9$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 10$		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$[2]	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 15 + w$		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	$0.25t_{CK} - 10$		$0.25t_{CK} - 8$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		$0.5t_{CK} - 5$		ns

w = wait states × t_{CK}.

NOTES

[1]t_{WP} (min) = $0.5t_{CK} - 8 + w$ for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

[2]t_{CWR} (max) = $0.25t_{CK} + 12$ for ADSP-2101TG-50, ADSP-2101TG/883B-50, ADSP-2111TG-52, and ADSP-2111TG/883B-52 (Extended Temperature Range devices).

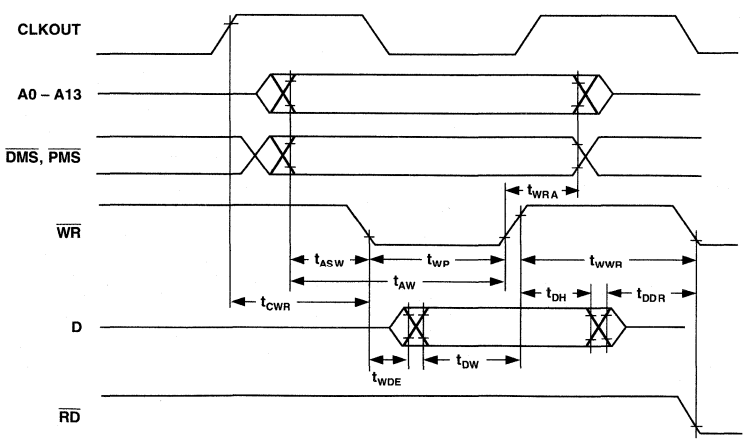


Figure 35. Memory Write

TIMING PARAMETERS (ADSP-2101/2105/2111/2115/2161/2163)

SERIAL PORTS

Parameter		12.5 MHz Min	12.5 MHz Max	13.0 MHz Min	13.0 MHz Max	13.824 MHz* Min	13.824 MHz* Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:										
t_{SCK}	SCLK Period	80		76.9		72.3				ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8		8		8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10		10		10				ns
t_{SCP}	$SCLK_{IN}$ Width	30		28		28				ns
Switching Characteristic:										
t_{CC}	CLKOUT High to $SCLK_{OUT}$	20	35	19.2	34.2	18.1	33.1	$0.25t_{CK}$	$0.25t_{CK}$ + 15ns	
t_{SCDE}	SCLK High to DT Enable	0		0		0				ns
t_{SCDV}	SCLK High to DT Valid		20		20		20			ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		0		0				ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		20		20		20			ns
t_{SCDH}	DT Hold after SCLK High	0		0		0				ns
t_{TDE}	TFS (Alt) to DT Enable	0		0		0				ns
t_{TDV}	TFS (Alt) to DT Valid		18		18		18			ns
t_{SCDD}	SCLK High to DT Disable		25		25		25			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20		20		20			ns

*Maximum serial port operating frequency is 13.824 MHz for all processor speed grades except the 12.5 MHz ADSP-2101and 13.0 MHz ADSP-2111.

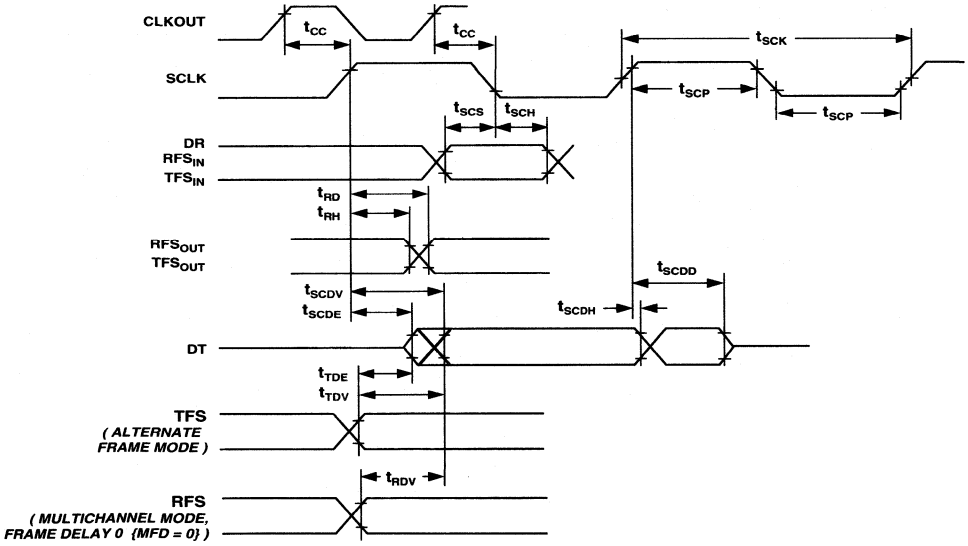


Figure 36. Serial Ports

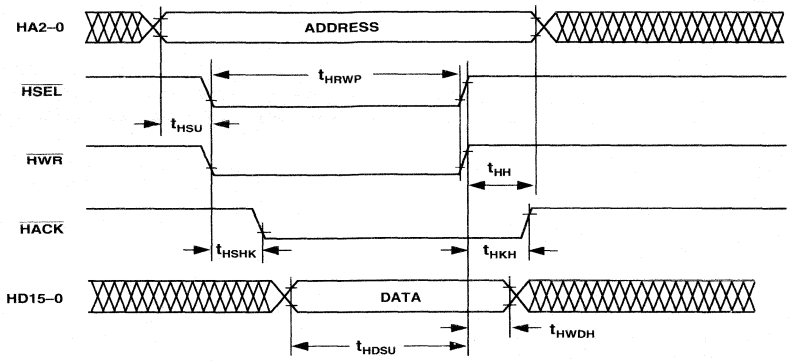
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0 Setup before Start of Write or Read[1, 2]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[3]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[3]	3		3		3			ns
t_{HH} HA2-0 Hold after End of Write or Read[3, 4]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[2]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[2]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[4]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[4]		10		10		10		ns

NOTES
[1]Start of Write = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]Start of Read = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low.
[3]End of Write = $\overline{\text{HWR}}$ High or $\overline{\text{HSEL}}$ High.
[4]End of Read = $\overline{\text{HRD}}$ High or $\overline{\text{HSEL}}$ High.
[5]Read Pulse Width = $\overline{\text{HRD}}$ Low and $\overline{\text{HSEL}}$ Low, Write Pulse Width = $\overline{\text{HWR}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

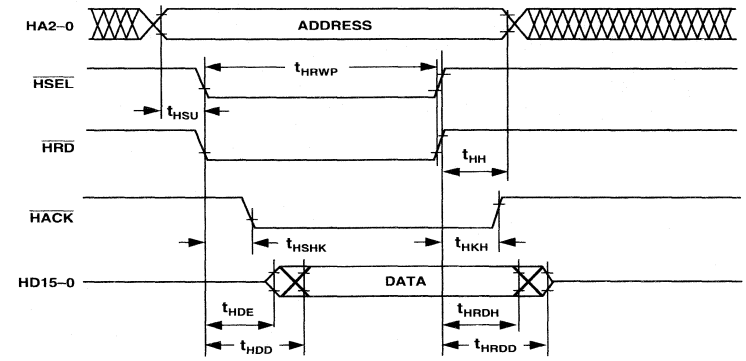


Figure 37. Host Interface Port (HMD1 = 0, HMD0 = 0)

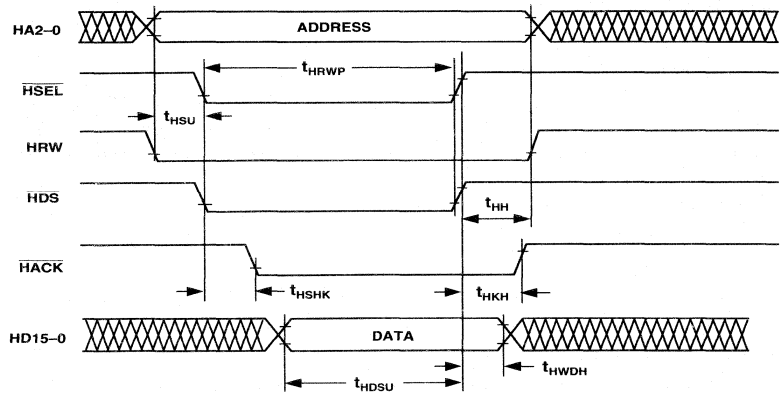
TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Separate Data & Address (HMD1 = 0)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HSU} HA2-0, HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} Data Setup before End of Write[2]	8		8		8			ns
t_{HWDH} Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HA2-0, HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle



Host Read Cycle

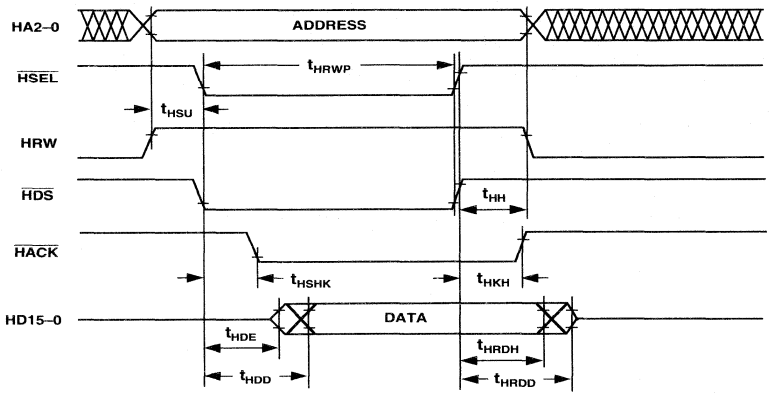


Figure 38. Host Interface Port (HMD1 = 0, HMD0 =1)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read Strobe & Write Strobe (HMD0 = 0)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			
t_{HALS} Start of Write or Read after ALE Low[1, 2]	15		15		15			
t_{HDSU} HAD15-0 Data Setup before End of Write[3]	8		8		8			
t_{HWDH} HAD15-0 Data Hold after End of Write[3]	3		3		3			
t_{HRWP} Read or Write Pulse Width[5]	30		30		30			
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	20	0	20	0	20		
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	20	0	20	0	20		
t_{HDE} HAD15-0 Data Enabled after Start of Read[2]	0		0		0			
t_{HDD} HAD15-0 Data Valid after Start of Read[2]		23		23		23		
t_{HRDH} HAD15-0 Data Hold after End of Read[4]	0		0		0			
t_{HRDD} HAD15-0 Data Disabled after End of Read[4]		10		10		10		

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

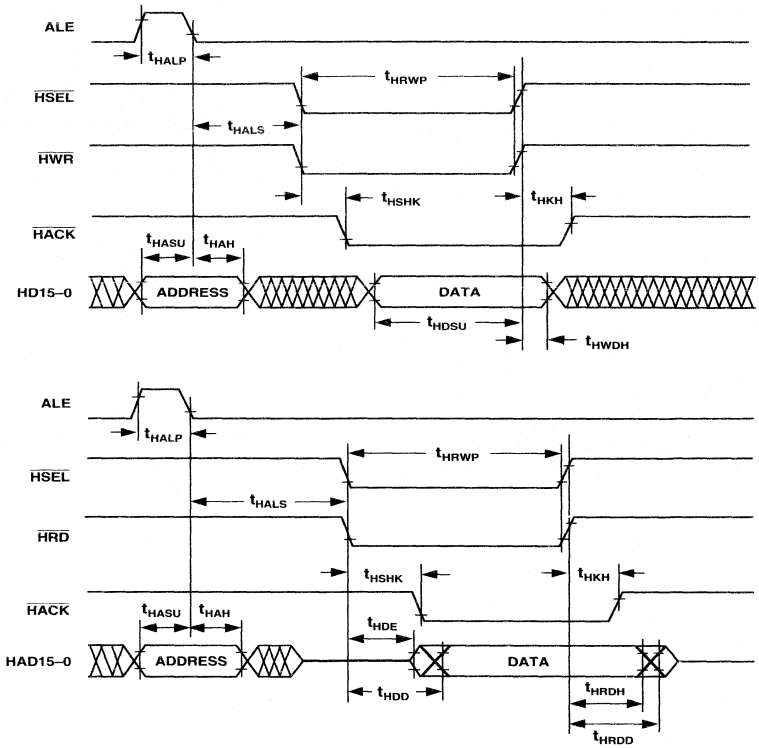


Figure 39. Host Interface Port (HMD1 = 1, HMD0 = 0)

TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1]	15		15		15			ns
t_{HSU} HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[2]	5		5		5			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{\text{HACK}}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{\text{HACK}}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.
[2]End of Write or Read = $\overline{\text{HDS}}$ High or $\overline{\text{HSEL}}$ High.
[3]Read or Write Pulse Width = $\overline{\text{HDS}}$ Low and $\overline{\text{HSEL}}$ Low.

Host Write Cycle

Host Read Cycle

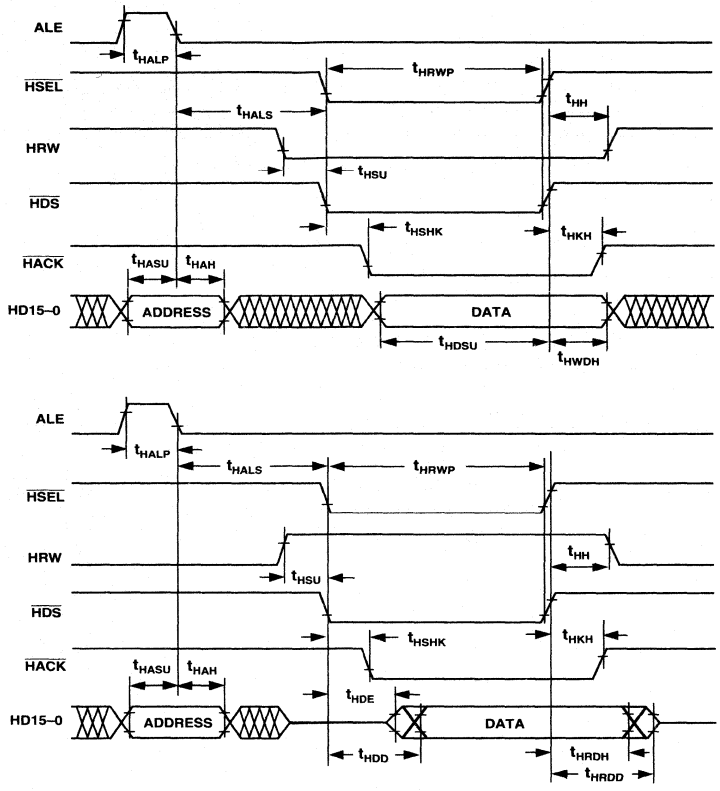


Figure 40. Host Interface Port (HMD1 = 1, HMD0 = 1)

TIMING PARAMETERS (ADSP-2103/2162/2164)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid

TIMING PARAMETERS (ADSP-2103/2162/2164)

CLOCK SIGNALS & RESET

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{CK}	CLKIN Period	97.6	150			ns
t_{CKL}	CLKIN Width Low	20				ns
t_{CKH}	CLKIN Width High	20				ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	488		$5t_{CK}$[1]		ns
Switching Characteristic:						
t_{CPL}	CLKOUT Width Low	38.8		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	38.8		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator startup time).

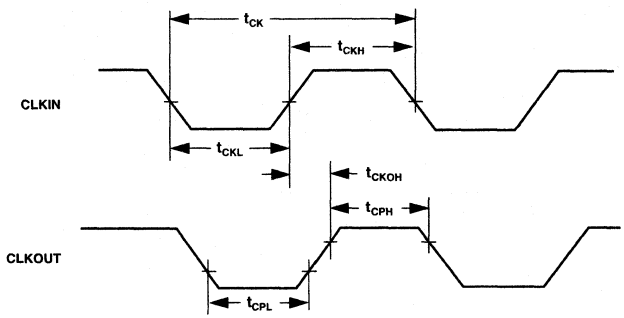


Figure 41. Clock Signals

TIMING PARAMETERS (ADSP-2103/2162/2164)

INTERRUPTS & FLAGS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	44.4		$0.25t_{CK}$ + 20		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	24.4		$0.25t_{CK}$		ns
Switching Characteristic:						
t_{FOH}	FO Hold after CLKOUT High	0				ns
t_{FOD}	FO Delay from CLKOUT High		15			ns

NOTES
[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

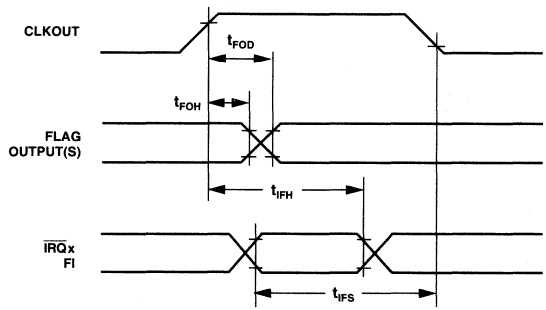


Figure 42. Interrupts & Flags

TIMING PARAMETERS (ADSP-2103/2162/2164)

BUS REQUEST/GRANT

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	29.4		$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	44.4		$0.25t_{CK}$ + 20		ns
Switching Characteristic:						
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		44.4		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0				ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0				ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	14.4		$0.25t_{CK}$ – 10		ns

NOTES
[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

Section 10.2.4, "Bus Request/Grant," of the *ADSP-2100 Family User's Manual (1st Edition, ©1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

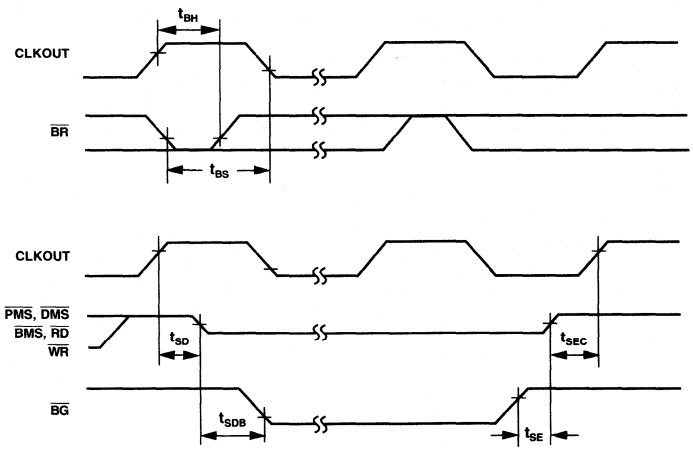


Figure 43. Bus Request/Grant

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY READ

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid		33.8		$0.5t_{CK} - 15 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		49.2		$0.75t_{CK} - 24 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0				ns
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

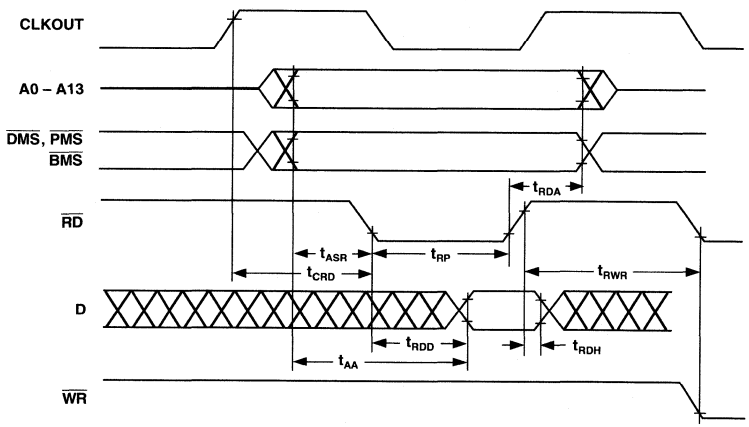


Figure 44. Memory Read

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY WRITE

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	38.8		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	14.4		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0				
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	14.4		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	58.2		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

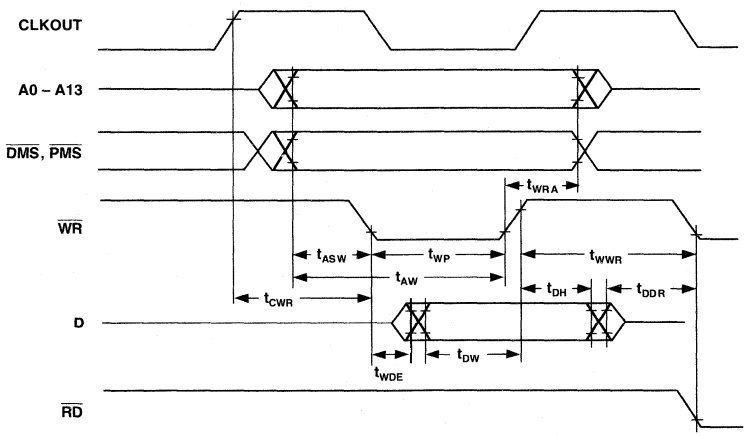


Figure 45. Memory Write

TIMING PARAMETERS (ADSP-2103/2162/2164)

SERIAL PORTS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		t_{CK}		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10				ns
t_{SCP}	$SCLK_{in}$ Width	28				ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	24.4	39.4	$0.25t_{CK}$	$0.25t_{CK} + 15$	ns
t_{SCDE}	SCLK High to DT Enable	0				ns
t_{SCDV}	SCLK High to DT Valid		28			ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0				ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		28			ns
t_{SCDH}	DT Hold after SCLK High	0				ns
t_{TDE}	TFS (alt) to DT Enable	0				ns
t_{TDV}	TFS (alt) to DT Valid		18			ns
t_{SCDD}	SCLK High to DT Disable		30			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20			ns

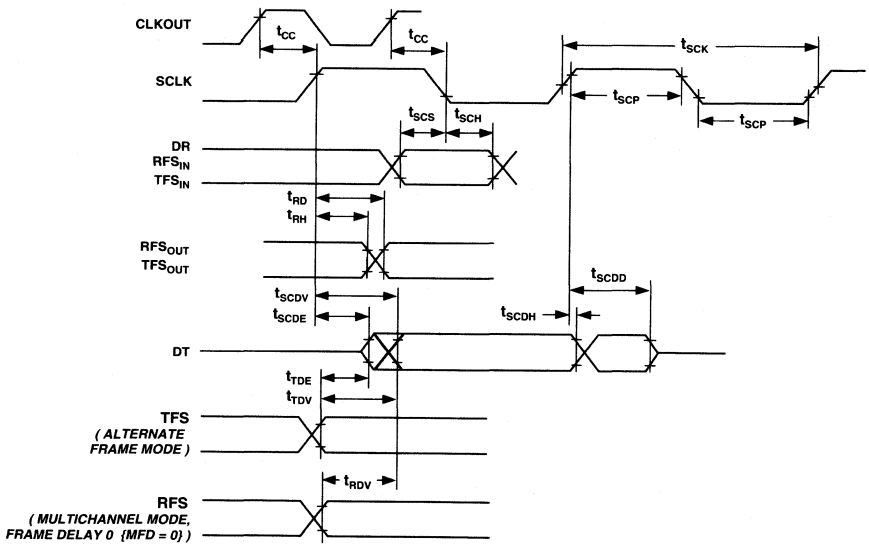
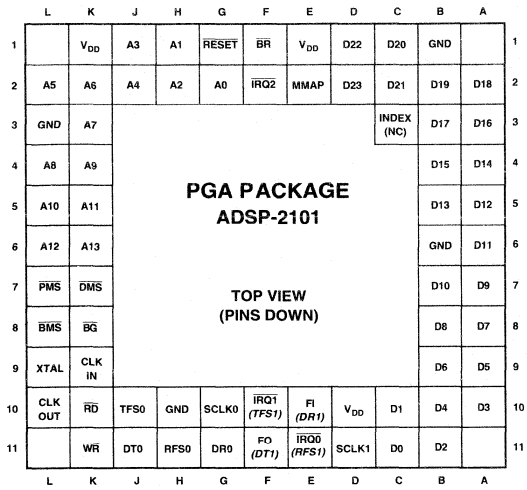
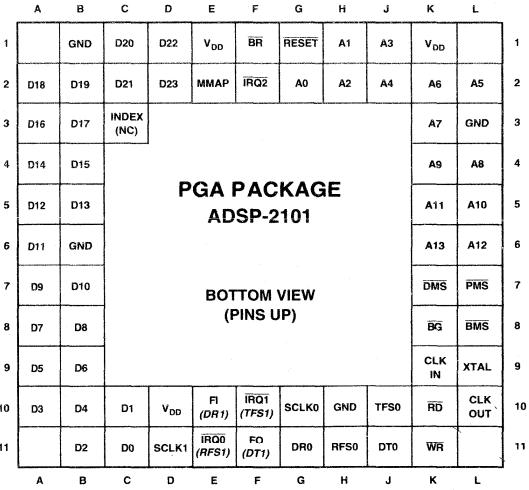


Figure 46. Serial Ports

PIN CONFIGURATIONS

68-Pin PGA





NC = NO CONNECT

PGA Number	Pin Name
K11	$\overline{WR}$
K10	$\overline{RD}$
J11	DT0
J10	TFS0
H11	RFS0
H10	GND
G11	DR0
G10	SCLK0
F11	FO *(DT1)*
F10	$\overline{IRQ1}$ *(TFS1)*
E11	$\overline{IRQ0}$ *(RFS1)*
E10	FI *(DR1)*
D11	SCLK1
D10	V_{DD}
C11	D0
C10	D1
B11	D2

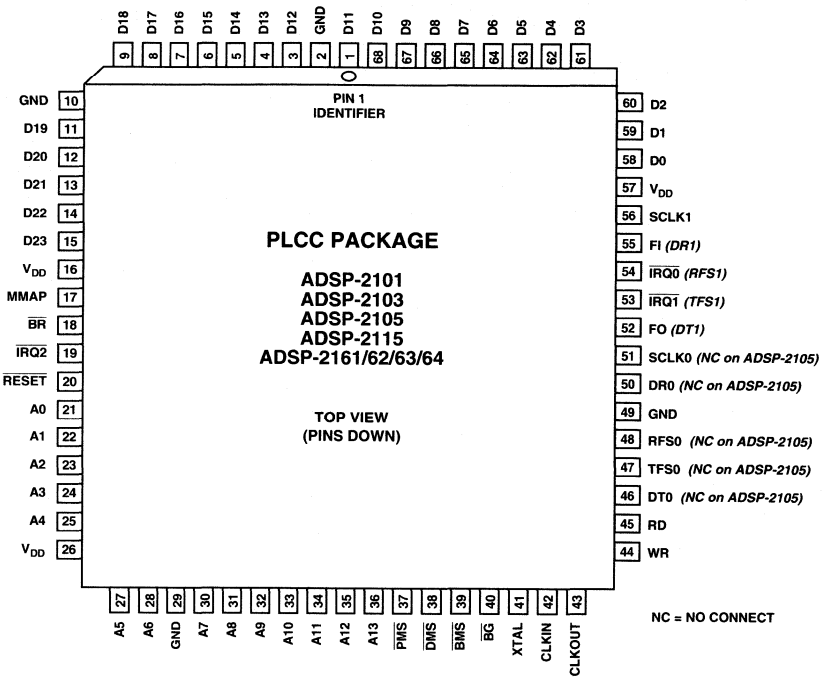
PGA Number	Pin Name
A10	D3
B10	D4
A9	D5
B9	D6
A8	D7
B8	D8
A7	D9
B7	D10
A6	D11
B6	GND
A5	D12
B5	D13
A4	D14
B4	D15
A3	D16
B3	D17
A2	D18

PGA Number	Pin Name
B1	GND
B2	D19
C1	D20
C2	D21
D1	D22
D2	D23
E1	VDD
E2	MMAP
F1	$\overline{BR}$
F2	$\overline{IRQ2}$
G1	$\overline{RESET}$
G2	A0
H1	A1
H2	A2
J1	A3
J2	A4
K1	V_{DD}

PGA Number	Pin Name
L2	A5
K2	A6
L3	GND
K3	A7
L4	A8
K4	A9
L5	A10
K5	A11
L6	A12
K6	A13
L7	$\overline{PMS}$
K7	$\overline{DMS}$
L8	$\overline{BMS}$
K8	$\overline{BG}$
L9	XTAL
K9	CLKIN
L10	CLKOUT
C3	Index (NC)

PIN CONFIGURATIONS

68-Lead PLCC



PLCC Number	Pin Name
1	D11
2	GND
3	D12
4	D13
5	D14
6	D15
7	D16
8	D17
9	D18
10	GND
11	D19
12	D20
13	D21
14	D22
15	D23
16	V_{DD}
17	MMAP

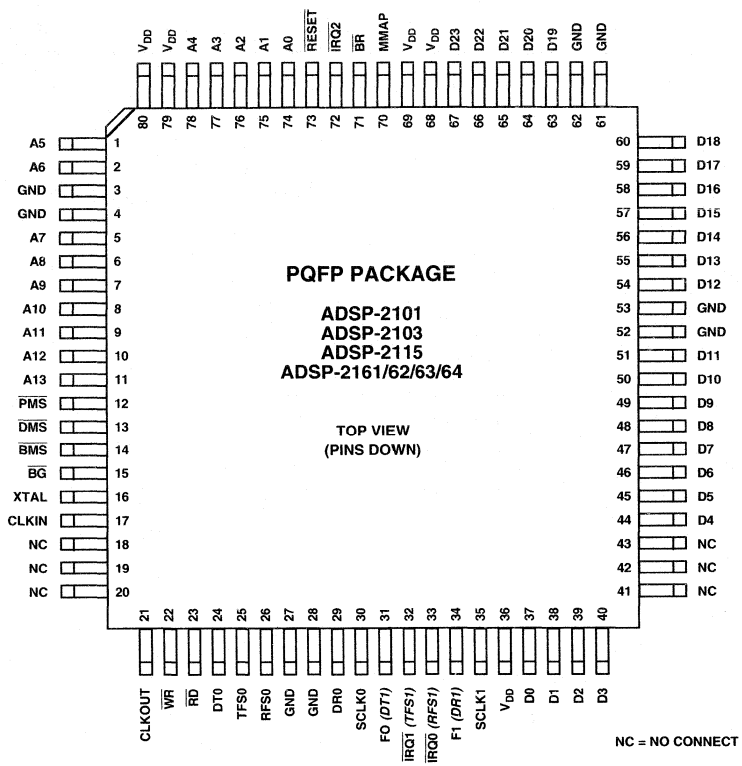
PLCC Number	Pin Name
18	$\overline{BR}$
19	$\overline{IRQ2}$
20	$\overline{RESET}$
21	A0
22	A1
23	A2
24	A3
25	A4
26	V_{DD}
27	A5
28	A6
29	GND
30	A7
31	A8
32	A9
33	A10
34	A11

PLCC Number	Pin Name
35	A12
36	A13
37	$\overline{PMS}$
38	$\overline{DMS}$
39	$\overline{BMS}$
40	$\overline{BG}$
41	XTAL
42	CLKIN
43	CLKOUT
44	$\overline{WR}$
45	$\overline{RD}$
46	DT0 *(NC on ADSP-2105)*
47	TFS0 *(NC on ADSP-2105)*
48	RFS0 *(NC on ADSP-2105)*
49	GND
50	DR0 *(NC on ADSP-2105)*
51	SCLK0 *(NC on ADSP-2105)*

PLCC Number	Pin Name
52	FO *(DT1)*
53	$\overline{IRQ1}$ *(TFS1)*
54	$\overline{IRQ0}$ *(RFS1)*
55	FI *(DR1)*
56	SCLK1
57	V_{DD}
58	D0
59	D1
60	D2
61	D3
62	D4
63	D5
64	D6
65	D7
66	D8
67	D9
68	D10

PIN CONFIGURATIONS

80-Lead PQFP
80-Lead TQFP



PQFP/ TQFP Number	Pin Name
1	A5
2	A6
3	GND
4	GND
5	A7
6	A8
7	A9
8	A10
9	A11
10	A12
11	A13
12	$\overline{PMS}$
13	$\overline{DMS}$
14	$\overline{BMS}$
15	$\overline{BG}$
16	XTAL
17	CLKIN
18	NC
19	NC
20	NC

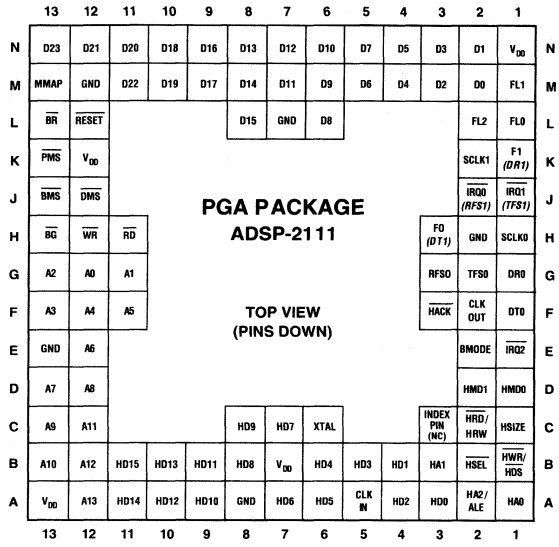
PQFP/ TQFP Number	Pin Name
21	$\overline{CLKOUT}$
22	$\overline{WR}$
23	$\overline{RD}$
24	DT0
25	TFS0
26	RFS0
27	GND
28	GND
29	DR0
30	SCLK0
31	FO *(DT1)*
32	$\overline{IRQ1}$ *(TFS1)*
33	$\overline{IRQ0}$ *(RFS1)*
34	FI *(DR1)*
35	SCLK1
36	V_{DD}
37	D0
38	D1
39	D2
40	D3

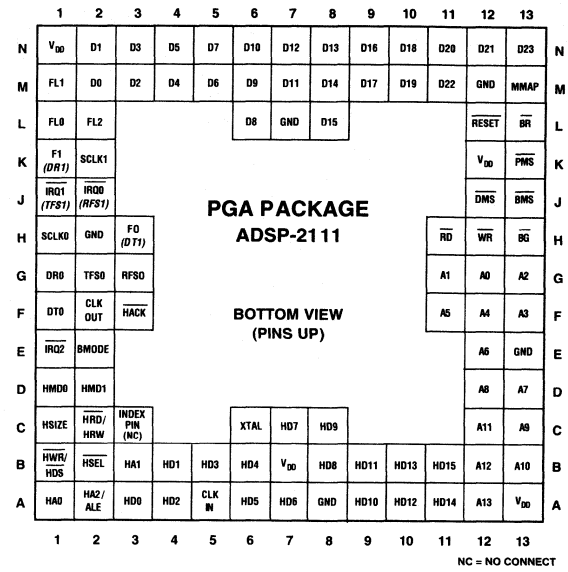
PQFP/ TQFP Number	Pin Name
41	NC
42	NC
43	NC
44	D4
45	D5
46	D6
47	D7
48	D8
49	D9
50	D10
51	D11
52	GND
53	GND
54	D12
55	D13
56	D14
57	D15
58	D16
59	D17
60	D18

PQFP/ TQFP Number	Pin Name
61	GND
62	GND
63	D19
64	D20
65	D21
66	D22
67	D23
68	V_{DD}
69	V_{DD}
70	MMAP
71	$\overline{BR}$
72	$\overline{IRQ2}$
73	$\overline{RESET}$
74	A0
75	A1
76	A2
77	A3
78	A4
79	V_{DD}
80	V_{DD}

PIN CONFIGURATIONS

100-Pin PGA





PGA Number	Pin Name
N13	D23
N12	D21
M13	MMAP
M12	GND
L13	$\overline{BR}$
L12	$\overline{RESET}$
K13	$\overline{PMS}$
K12	V_{DD}
J13	$\overline{BMS}$
J12	$\overline{DMS}$
H13	$\overline{BG}$
H12	$\overline{WR}$
H11	$\overline{RD}$
G13	A2
G12	A0
G11	A1
F13	A3
F12	A4
F11	A5
E13	GND
E12	A6
D13	A7
D12	A8
C13	A9
C12	A11

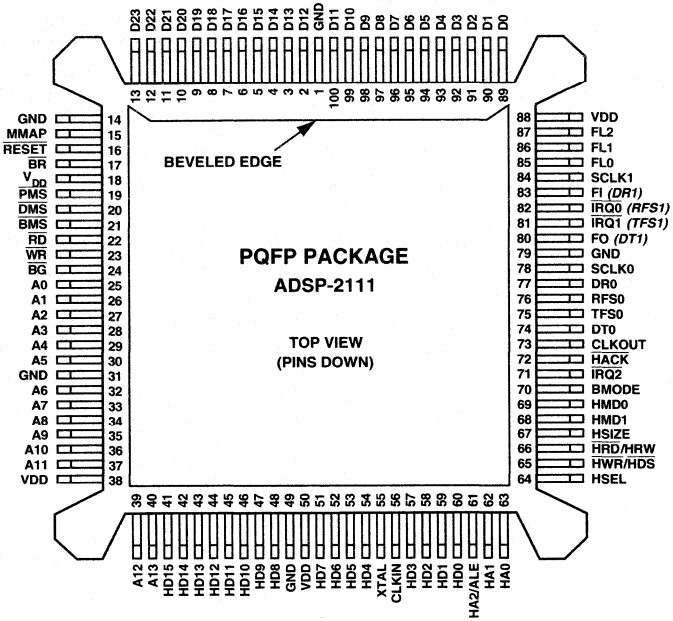
PGA Number	Pin Name
B13	A10
A13	V_{DD}
A12	A13
B12	A12
A11	HD14
B11	HD15
A10	HD12
B10	HD13
A9	HD10
B9	HD11
A8	GND
B8	HD8
C8	HD9
A7	HD6
B7	V_{DD}
C7	HD7
A6	HD5
B6	HD4
C6	XTAL
A5	CLKIN
B5	HD3
A4	HD2
B4	HD1
A3	HD0
B3	HA1

PGA Number	Pin Name
C3	Index (NC)
A2	HA2/ALE
A1	$\overline{HA0}$
B1	$\overline{HWR}$/$\overline{HDS}$
B2	$\overline{HSEL}$
C1	HSIZE
C2	$\overline{HRD}$/HRW
D1	HMD0
D2	HMD1
E1	$\overline{IRQ2}$
E2	BMODE
F1	DT0
F2	$\overline{CLKOUT}$
F3	$\overline{HACK}$
G1	DR0
G2	TFS0
G3	RFS0
H1	SCLK0
H2	GND
H3	FO *(DT1)*
J1	$\overline{IRQ1}$ *(TFS1)*
J2	$\overline{IRQ0}$ *(RFS1)*
K1	FI *(DR1)*
K2	SCLK1
L1	FL0

PGA Number	Pin Name
L2	FL2
M1	FL1
N1	V_{DD}
N2	D1
M2	D0
N3	D3
M3	D2
N4	D5
M4	D4
N5	D7
M5	D6
N6	D10
M6	D9
L6	D8
N7	D12
M7	D11
L7	GND
N8	D13
M8	D14
L8	D15
N9	D16
M9	D17
N10	D18
M10	D19
N11	D20
M11	D22

PIN CONFIGURATIONS

100-Lead Bumpered PQFP



NOTE: PIN 1 IS LOCATED AT THE CENTER OF THE BEVELED-EDGE SIDE OF THE PACKAGE.

PQFP Number	Pin Name
1	GND
2	D12
3	D13
4	D14
5	D15
6	D16
7	D17
8	D18
9	D19
10	D20
11	D21
12	D22
13	D23
14	GND
15	MMAP
16	$\overline{\text{RESET}}$
17	$\overline{\text{BR}}$
18	V_{DD}
19	$\overline{\text{PMS}}$
20	$\overline{\text{DMS}}$
21	$\overline{\text{BMS}}$
22	$\overline{\text{RD}}$
23	$\overline{\text{WR}}$
24	$\overline{\text{BG}}$
25	A0

PQFP Number	Pin Name
26	A1
27	A2
28	A3
29	A4
30	A5
31	GND
32	A6
33	A7
34	A8
35	A9
36	A10
37	A11
38	V_{DD}
39	A12
40	A13
41	HD15
42	HD14
43	HD13
44	HD12
45	HD11
46	HD10
47	HD9
48	HD8
49	GND
50	V_{DD}

PQFP Number	Pin Name
51	HD7
52	HD6
53	HD5
54	HD4
55	XTAL
56	CLKIN
57	HD3
58	HD2
59	HD1
60	HD0
61	HA2/ALE
62	HA1
63	$\overline{\text{HA0}}$
64	$\overline{\text{HSEL}}$
65	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$
66	$\overline{\text{HRD}}$/HRW
67	HSIZE
68	HMD1
69	HMD0
70	BMODE
71	$\overline{\text{IRQ2}}$
72	$\overline{\text{HACK}}$
73	CLKOUT
74	DT0
75	TFS0

PQFP Number	Pin Name
76	RFS0
77	DR0
78	SCLK0
79	GND
80	FO *(DT1)*
81	$\overline{\text{IRQ1}}$ *(TFS1)*
82	$\overline{\text{IRQ0}}$ *(RFS1)*
83	FI *(DR1)*
84	SCLK1
85	FL0
86	FL1
87	FL2
88	V_{DD}
89	D0
90	D1
91	D2
92	D3
93	D4
94	D5
95	D6
96	D7
97	D8
98	D9
99	D10
100	D11

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option[2]
ADSP-2101KG-50	0°C to +70°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2101BG-50	–40°C to +85°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2101KP-50	0°C to +70°C	12.5 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-50	–40°C to +85°C	12.5 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-50	0°C to +70°C	12.5 MHz	80-Lead PQFP	S-80
ADSP-2101BS-50	–40°C to +85°C	12.5 MHz	80-Lead PQFP	S-80
ADSP-2101KG-66	0°C to +70°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101BG-66	–40°C to +85°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101KG-80	0°C to +70°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101BG-80	–40°C to +85°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101TG-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2101TG/883B-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2103KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2103BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2105KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2115KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-55	0°C to +70°C	13.824 MHz	80-Lead PQFP	S-80
ADSP-2115BS-55	–40°C to +85°C	13.824 MHz	80-Lead PQFP	S-80
ADSP-2115KST-55[3]	0°C to +70°C	13.824 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-55[3]	–40°C to +85°C	13.824 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115KST-66[3]	0°C to +70°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-66[3]	–40°C to +85°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115KST-80[3]	0°C to +70°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-80[3]	–40°C to +85°C	20.0 MHz	80-Lead TQFP	ST-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
ST = TQFP (Thin Quad Flatpack)
[2]For outline information see Package Information section.
[3]Minimum order quantities required. Contact factory for further information.

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option[2]
ADSP-2111KG-52	0°C to +70°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-52	–40°C to +85°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-52	0°C to +70°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-52	–40°C to +85°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-66	0°C to +70°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111BG-66	–40°C to +85°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111KS-66	0°C to +70°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-66	–40°C to +85°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-80	0°C to +70°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-80	–40°C to +85°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-80	0°C to +70°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-80	–40°C to +85°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111TG-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111TG/883B-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2161KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2161BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2162KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2162BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2163KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2164KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2164BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
[2]For outline information see Package Information section.

ANALOG DEVICES

DSP Microcomputer

ADSP-2171

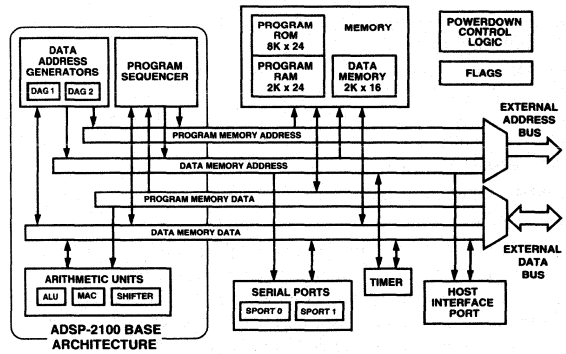
FEATURES

30 ns Instruction Cycle Time (33 MIPS) from 16.67 MHz Crystal at 5.0 V
38 ns Instruction Cycle Time (26 MIPS) from 13 MHz Crystal at 5.0 V
ADSP-2100 Family Code & Function Compatible with New Instruction Set Enhancements for Bit Manipulation Instructions, Multiplication Instructions, Biased Rounding, and Global Interrupt Masking
Bus Grant Hang Logic
2K Words of On-Chip Program Memory RAM
2K Words of On-Chip Data Memory RAM
8K Words of On-Chip Program Memory ROM (Optional)
8- or 16-Bit Parallel Host Interface Port
300 mW Typical Power Dissipation at 5.0 V at 30 ns
245 mW Typical Power Dissipation at 5.0 V at 38 ns
Powerdown Mode Featuring Less than 0.55 mW CMOS Standby Power Dissipation with 100 Cycle Recovery from Powerdown Condition
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, and Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Programmable 16-Bit Interval Timer with Prescaler
Programmable Wait State Generation
Automatic Booting of Internal Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Host Interface Port
Stand-Alone ROM Execution (Optional)
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Three Edge- or Level-Sensitive External Interrupts
Low Power Dissipation in Standby Mode
128-Lead TQFP and 128-Lead PQFP

GENERAL DESCRIPTION

The ADSP-2171 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high-speed numeric processing applications.

FUNCTIONAL BLOCK DIAGRAM



The ADSP-2171 combines the ADSP-2100 base architecture (three computational units, data address generators, and a program sequencer) with two serial ports, a host interface port, a programmable timer, extensive interrupt capabilities, and on-chip program and data memory.

In addition, the ADSP-2171 supports new instructions, which include bit manipulations–bit set, bit clear, bit toggle, bit test–new ALU constants, new multiplication instruction (x squared), biased rounding, and global interrupt masking, for increased flexibility. The ADSP-2171 also has a Bus Grant Hang Logic ($\overline{BGH}$) feature.

The ADSP-2171 provides 8K words (24-bit) of program ROM, 2K words (24-bit) of program RAM, and 2K words (16-bit) of data memory. Power down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2171 is available in 128-pin TQFP and 128-pin PQFP packages.

Fabricated in a high-speed, double metal, low power, CMOS process, the ADSP-2171 operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2171's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2171 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the host interface port
- decrement timer

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2171. The System Builder provides a high-level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-2171 assembly source code. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

EZ-Tools, low cost, easy-to-use hardware tools, also support the ADSP-2171.

The ADSP-2171 EZ-ICE® Emulator aids in the hardware debugging of ADSP-2171 systems. The emulator consists of hardware, host computer resident software, the emulator probe, and the pin adaptor. The emulator performs a full range of emulation functions including stand-alone operation or operation in the target, setting up to 20 breakpoints, single-step or full-speed operation in the target, examining and altering registers and memory values, and PC upload/download functions. If you plan to use the emulator, you should consider the emulator's restrictions (differences between emulator and processor operation).

The EZ-LAB® Evaluation Board is a PC plug-in card, but it can operate in stand-alone mode. The evaluation board/system development board executes EPROM-based or downloaded programs. Modular Analog Front End daughter cards with different codecs will be made available.

EZ-ICE and EZ-LAB are registered trademarks of Analog Devices, Inc.

Additional Information

This data sheet provides a general overview of ADSP-2171 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual.* For more information about the Development System and ADSP-2171 programmer's reference information, refer to the *ADSP-2100 Family Assembler Tools & Simulator Manual.*

ARCHITECTURE OVERVIEW

Figure 1 is an overall block diagram of the ADSP-2171. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus directly connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2171 executes looped code with zero overhead; no explicit jump instructions are required to maintain the loop.

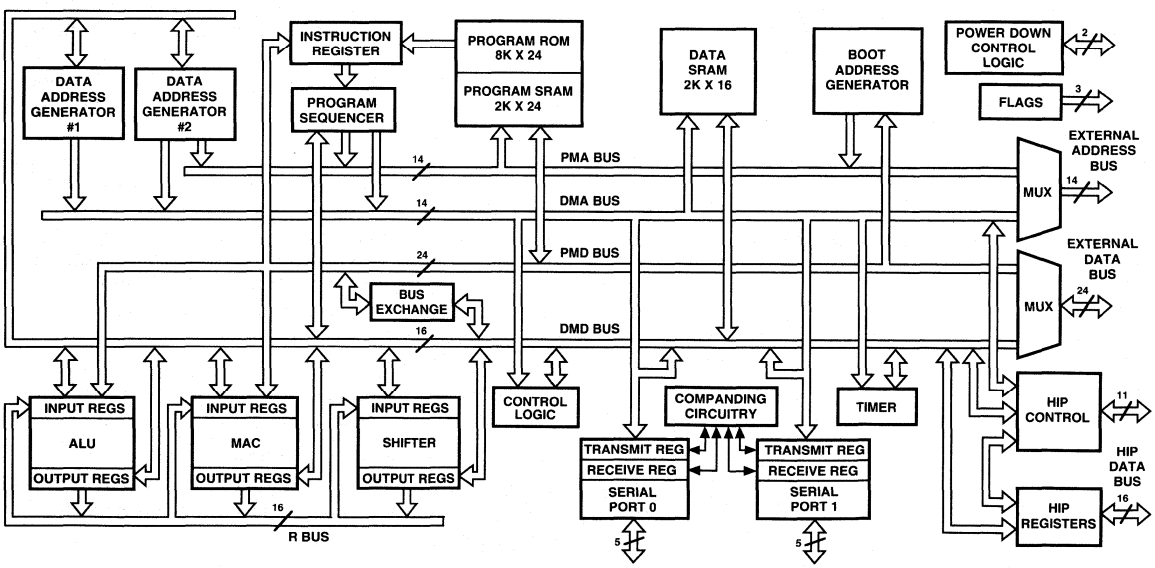


Figure 1. ADSP-2171 Block Diagram

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses.

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus.

Program memory can store both instructions and data, permitting the ADSP-2171 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2171 can fetch an operand from on-chip program memory and the next instruction in the same cycle.

The memory interface supports slow memories and memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2171 to continue running from internal memory. Normal execution mode requires the processor to halt while buses are granted.

In addition to the address and data bus for external memory connection, the ADSP-2171 has a configurable 8- or 16-bit Host Interface Port (HIP) for easy connection to a host processor. The HIP is made up of 16 data/address pins and 11 control pins. The HIP is extremely flexible and provides a simple interface to a variety of host processors. For example, the Motorola 68000 series, the Intel 80C51 series and the Analog Devices' ADSP-2101 can be easily connected to the HIP. The host processor can initialize the ASDP-2171's on-chip memory through the HIP.

The ADSP-2171 can respond to eleven interrupts. There can be up to three external interrupts, configured as edge or level sensitive, and eight internal interrupts generated by the Timer, the Serial Ports ("SPORTs"), the HIP, the powerdown circuitry, and software. There is also a master RESET signal.

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

Boot circuitry provides for loading on-chip program memory automatically from byte-wide external memory. After reset, seven wait states are automatically generated. This allows, for example, a 30 ns ADSP-2171 to use an external 200 ns EPROM as boot memory. Multiple programs can be selected and loaded from the EPROM with no additional hardware. The on-chip program memory can also be initialized through the HIP.

The ADSP-2171 features three general-purpose flag outputs whose states can be simultaneously changed through software. You can use these outputs to signal an event to an external device. In addition, the data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every n processor cycles, where n-l is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

The ADSP-2171 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2171 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Serial Ports

The ADSP-2171 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2171 SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts (IRQ0 and IRQ1) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-2171 is available in 128-lead TQFP and 128-lead PQFP packages. Table I contains the pin descriptions.

Table I. ADSP-2171 Pin List

Pin Group Name	# of Pins	Input/ Output	Function
Address	14	O	Address output for program, data and boot memory spaces
Data	24	I/O	Data I/O pins for program and data memories. Input only for boot memory space, with two MSBs used as boot space addresses.
$\overline{\text{RESET}}$	1	I	Processor reset input
$\overline{\text{IRQ2}}$	1	I	External interrupt request #2
$\overline{\text{BR}}$	1	I	External bus request input
$\overline{\text{BG}}$	1	O	External bus grant output
$\overline{\text{BGH}}$	1	O	External bus grant hang output
$\overline{\text{PMS}}$	1	O	External program memory select
$\overline{\text{DMS}}$	1	O	External data memory select
$\overline{\text{BMS}}$	1	O	Boot memory select
$\overline{\text{RD}}$	1	O	External memory read enable
$\overline{\text{WR}}$	1	O	External memory write enable
MMAP	1	I	Memory map select
CLKIN, XTAL	2	I	External clock or quartz crystal input
CLKOUT	1	O	Processor clock output
$\overline{\text{HSEL}}$	1	I	HIP select input
$\overline{\text{HACK}}$	1	O	HIP acknowledge output
HSIZE	1		8/16 bit host select input 0 = 16-bit; 1 = 8-bit
BMODE	1	I	Boot mode select input 0 = EPROM/data bus; 1 = HIP
HMD0	1	I	Bus strobe select input 0 = RD, WR; 1 = RW, DS
HMD1	1	I	HIP address/data mode select input 0 = separate; 1 = multiplexed
$\overline{\text{HRD}}$/HRW	1	I	HIP read strobe/read/write select input
$\overline{\text{HWR}}$/$\overline{\text{HDS}}$	1	I	HIP write strobe/host data strobe select input
HD15–0/ HAD15-0	16	I/O	HIP data/data and address
HA2/ALE	1	I	Host address 2/Address latch enable input
HA1–0/ Unused	2	I	Host addresses 1 and 0 inputs
SPORT0	5	I/O	Serial port 0 I/O pins (TFS0, RFS0, DT0, DR0, SCLK0)
SPORT1 or $\overline{\text{IRQ1}}$ (TFS1)	5 1	I/O I	Serial port 1 I/O pins External interrupt request #1
$\overline{\text{IRQ0}}$ (RFS1)	1	I	External interrupt request #0
SCLK1	1	O	Programmable clock output
FO (DT1)	1	O	Flag Output pin
FI (DR1)	1	I	Flag Input pin
FL2–0	3	O	General purpose flag output pins
V_{DD}	6		Power supply pins
GND	11		Ground pins
$\overline{\text{PWD}}$	1	I	Powerdown pin
PWDACK	1	O	Powerdown acknowledge pin

Host Interface Port

The ADSP-2171 host interface port is a parallel I/O port that allows for an easy connection to a host processor. Through the HIP, the ADSP-2171 can be used as a memory-mapped peripheral to a host computer. The HIP can be thought of as an area of dual-ported memory, or mailbox registers, that allow communication between the computational core of the ADSP-2171 and the host computer.

The HIP is completely asynchronous. The host processor can write data into the HIP while the ADSP-2171 is operating at full speed.

The HIP can be configured with the following pins:

- HSIZE configures HIP for 8-bit or 16-bit communication with the host processor.
- BMODE (when MMAP = 0) determines whether the ADSP-2171 boots from the host processor (through the HIP) or external EPROM (through the data bus).
- HMD0 configures the bus strobes as separate read and write strobes, or a single read/write select and a host data strobe.
- HMD1 selects separate address (3-bit) and data (16-bit) buses, or a multiplexed, 16-bit address/data bus with address latch enable.

Tying these pins to appropriate values configures the ADSP-2171 for straight-wire interface to a variety of industry-standard microprocessors and microcomputers.

In 8-bit reads, the ADSP-2171 three-states the upper eight bits of the bus. When the host processor writes an 8-bit value to the HIP, the upper eight bits are all zeros. For additional information refer to the *ADSP-2100 Family User's Manual.*

HIP Operation

The HIP contains six data registers (HDR5–0) and two status registers (HSR7–6) with an associated HMASK register for masking interrupts from individual HIP data registers. All HIP data registers are memory-mapped into the internal data memory of the ADSP-2171. HIP transfers can be managed using either interrupts or a polling scheme. These registers are shown in the section "ADSP-2171 Registers."

The HIP allows a software reset to be performed by the host processor. The internal software reset signal is asserted for five ADSP-2171 processor cycles.

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2171 provides up to three external interrupt input pins, $\overline{IRQ0}$, $\overline{IRQ1}$ and $\overline{IRQ2}$. $\overline{IRQ2}$ is always available as a dedicated pin; SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, and the flags. The ADSP-2171 also supports internal interrupts from the timer, the host interface port, the two serial ports, software, and the powerdown control circuit. The interrupt levels are internally prioritized and individually maskable (except powerdown and reset). The input pins can be programmed to be either level- or edge-sensitive. The priorities and vector addresses of all interrupts are shown in Table II, and the interrupt registers are shown in Figure 2.

Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected.The powerdown interrupt is nonmaskable.

The ADSP-2171 masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect autobuffering.

The interrupt control register, ICNTL, allows the external interrupts to be either edge- or level-sensitive. Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially.

The IFC register is a write-only register used to force and clear interrupts generated from software.

Table II. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)	
Reset (or Power-Up with PUCR = 1)	0000	(*Highest Priority*)
Powerdown (Nonmaskable)	002C	
$\overline{IRQ2}$	0004	
HIP Write	0008	
HIP Read	000C	
SPORT0 Transmit	0010	
SPORT0 Receive	0014	
Software Interrupt 1	0018	
Software Interrupt 0	001C	
SPORT1 Transmit or $\overline{IRQ1}$	0020	
SPORT1 Receive or $\overline{IRQ0}$	0024	
Timer	0028	(*Lowest Priority*)

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling.

The stacks are twelve levels deep to allow interrupt nesting.

The following instructions allow global enable or disable servicing of the interrupts (including powerdown), regardless of the state of IMASK. Disabling the interrupts does not affect autobuffering.

ENA INTS;
DIS INTS;

When you reset the processor, the interrupt servicing is enabled.

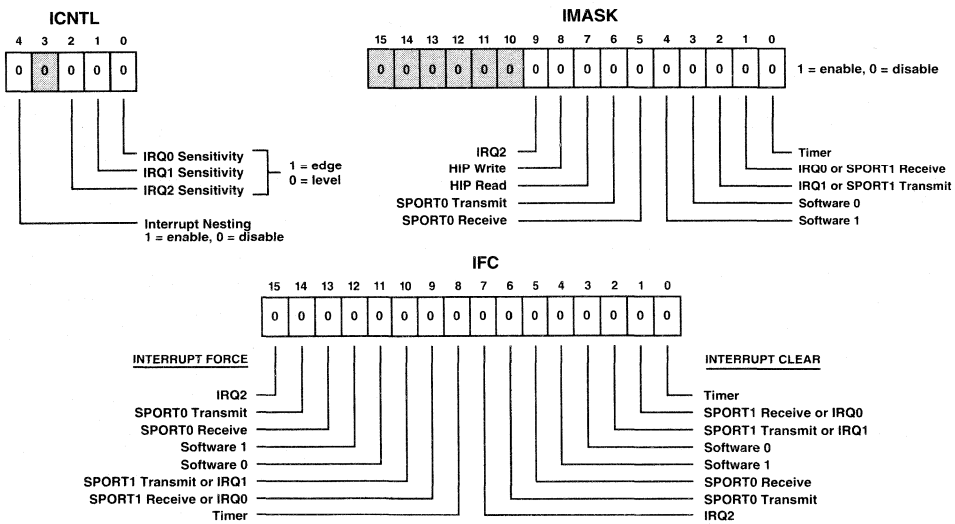


Figure 2. Interrupt Registers

LOW POWER OPERATION

The ADSP-2171 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Powerdown
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation. The CLKOUT pin is controlled by Bit 14 of SPORT0 Autobuffer Control Register, DM[0x3FF3].

Powerdown

The ADSP-2171 processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of powerdown features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9 "System Interface" for detailed information about the powerdown feature.

- Powerdown mode holds the processor in CMOS standby with a maximum current of less than 100 µA in some modes.
- Quick recovery from powerdown. The processor begins executing instructions in as few as 100 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during powerdown without affecting the lowest power rating and 100 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 CLKIN cycle startup.
- Powerdown is initiated by either the powerdown pin ($\overline{\text{PWD}}$) or the software powerdown force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The powerdown interrupt also can be used as a non-maskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the powerdown state.
- The $\overline{\text{RESET}}$ pin also can be used to terminate powerdown, and the host software reset feature can be used to terminate powerdown under certain conditions.
- Powerdown acknowledge pin indicates when the processor has entered powerdown.

Idle

When the ADSP-2171 is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction.

Slow Idle

The *IDLE* instruction is enhanced on the ADSP-2171 to let the processor's internal clock signal be slowed during *IDLE*, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts—the 1-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2171 will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 3 shows a basic system configuration with the ADSP-2171, two serial devices, a host processor, a boot EPROM, and optional external program and data memories. Up to 14K words of data memory and 16K words of program memory can be supported. Programmable wait state generation allows the processor to interface easily to slow memories. The ADSP-2171 also provides one external interrupt and two serial ports or three external interrupts and one serial port.

Clock Signals

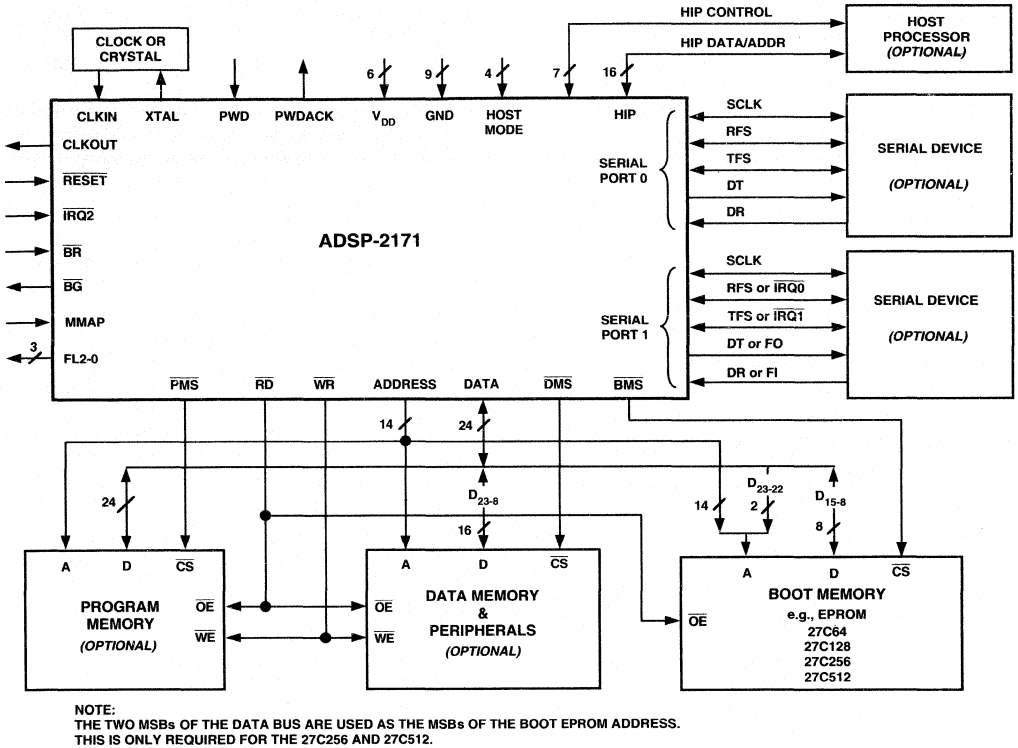
The ADSP-2171 can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the Powerdown State. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual* for detailed information on this powerdown feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-2171 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2171 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 4. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.



NOTE:
THE TWO MSBs OF THE DATA BUS ARE USED AS THE MSBs OF THE BOOT EPROM ADDRESS.
THIS IS ONLY REQUIRED FOR THE 27C256 AND 27C512.

Figure 3. ADSP-2171 Basic System Configuration

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register, DM[0x3FF3].

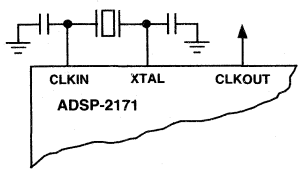


Figure 4. External Crystal Connections

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2171. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power-up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. Then the first instruction is fetched from internal program memory location 0x0000.

Program Memory Interface

The on-chip program memory address bus (PMA) and the on-chip program memory data bus (PMD) are multiplexed with on-chip DMA and DMD buses, creating a single external data bus and a single external address bus. The 14-bit address bus directly addresses up to 16K words. 10K words of memory for ADSP-2171 with optional 8K ROM and 2K words of memory for the non-ROM version are on-chip. The data bus is bidirectional and 24 bits wide to external program memory. Program memory may contain code and data.

The program memory data lines are bidirectional. The program memory select ($\overline{PMS}$) signal indicates access to the program memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and is used as a write strobe.

The read ($\overline{RD}$) signal indicates a read operation and is used as a read strobe or output enable signal.

The ADSP-2171 writes data from its 16-bit registers to the 24-bit program memory using the PX register to provide the lower eight bits. When it reads data (not instructions) from 24-bit program memory to a 16-bit data register, the lower eight bits are placed in the PX register.

Program Memory Maps

ADSP-2171

Program memory can be mapped in two ways, depending on the state of the MMAP pin. Figure 5 shows the different configurations. When MMAP = 0, internal RAM occupies 2K words beginning at address 0x0000. In this configuration, the boot loading sequence (described in "Boot Memory Interface") is automatically initiated when $\overline{RESET}$ is released.

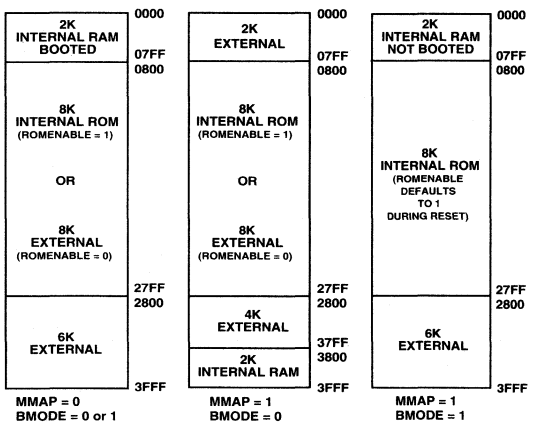


Figure 5. ADSP-2171 Memory Maps

When MMAP = 1, words of external program memory begin at address 0x0000 and internal RAM is located in the upper 2K words, beginning at address 0x3800. In this configuration, program memory is not loaded although it can be written to and read from under program control.

The optional ROM always resides at locations PM[0x0800] through PM[0x27FF] regardless of the state of the MMAP pin. The ROM is enabled by setting the ROMENABLE bit in the Data Memory Wait State control register, DM[0x3FFE]. When the ROMENABLE bit is set to 1, addressing program memory in this range will access the on-chip ROM. When set to zero, addressing program memory in this range will access external program memory. The ROMENABLE bit is set to 0 on chip reset unless MMAP *and* BMODE = 1.

The program memory interface can generate 0 to 7 wait states for external memory devices; default is to 7 wait states after $\overline{RESET}$.

Boot Memory Interface

The ADSP-2171 can load on-chip memory from external boot memory space. The boot memory space consists of 64K by 8-bit space, divided into eight separate 8K by 8-bit pages. Three bits in the system control register select which page is loaded by the boot memory interface. Another bit in the system control register allows the user to force a boot loading sequence under software control. Boot loading from page 0 after $\overline{RESET}$ is initiated automatically if MMAP = 0.

The boot memory interface can generate 0 to 7 wait states; it defaults to 7 wait states after $\overline{RESET}$. This allows the ADSP-2171 to boot from a single low cost EPROM such as a 27C256. Program memory is booted one byte at a time and converted to 24-bit program memory words.

The $\overline{BMS}$ and $\overline{RD}$ signals are used to select and to strobe the boot memory interface. Only 8-bit data is read over the data bus, on pins D8–D15. To accommodate addressing up to eight pages of boot memory, the two MSBs of the data bus are used in the boot memory interface as the two MSBs of the boot space address.

The ADSP-2100 Family Assembler and Linker support the creation of programs and data structures requiring multiple boot pages during execution.

$\overline{RD}$ and $\overline{WR}$ must always be qualified by $\overline{PMS}$, $\overline{DMS}$, or $\overline{BMS}$ to ensure the correct program, data, or boot memory accessing.

HIP Booting

The ADSP-2171 can also boot programs through its Host Interface Port. If BMODE = 1 and MMAP = 0, the ADSP-2171 boots from the HIP. If BMODE = 0, the ADSP-2171 boots through the data bus (in the same way as the ADSP-2101), as described above in "Boot Memory Interface." For additional information about HIP booting, refer to the *ADSP-2100 Family User's Manual*, Chapter 7, "Host Interface Port."

The ADSP-2100 Family Development Software includes a utility program called the HIP Splitter. This utility allows the creation of programs that can be booted via the ADSP-2171's HIP, in a similar fashion as EPROM-bootable programs generated by the PROM Splitter utility.

Stand-Alone ROM Execution
When the MMAP and BMODE pins both are set to 1, the ROM is automatically enabled and execution commences from program memory location 0x0800 at the start of ROM. This feature lets an embedded design operate without external memory components. To operate in this mode, the ROM coded program must copy an interrupt vector table to the appropriate locations in program memory RAM. In this mode, the ROM enable bit defaults to 1 during reset.

Table III. Boot Summary Table

	BMODE = 0	BMODE = 1
MMAP = 0	Boot from EPROM, then execution starts at internal RAM location 0x0000	Boot from HIP, then execution starts at internal RAM location 0x0000
MMAP = 1	No booting, execution starts at external memory location 0x0000	Stand-Alone Mode, execution starts at internal ROM location 0x0800

Data Memory Interface
The data memory address (DMA) bus is 14 bits wide. The bidirectional external data bus is 24 bits wide, with the upper 16 bits (D8–D23) used for data memory data (DMD) transfers.

The data memory select ($\overline{DMS}$) signal indicates access to the data memory and can be used as a chip select signal. The write ($\overline{WR}$) signal indicates a write operation and can be used as a write strobe. The read ($\overline{RD}$) signal indicates a read operation and can be used as a read strobe or output enable signal.

The ADSP-2171 supports memory-mapped I/O, with the peripherals memory mapped into the data or program memory address spaces and accessed by the processor in the same manner.

Data Memory Map
The on-chip data memory RAM resides in the 2K words of data memory beginning at address 0x3000, as shown in Figure 6. In addition, data memory locations from 0x3800 to the end of data memory at 0x3FFF are reserved. Control registers for the system, timer, wait state configuration, host interface port, and serial port operations are located in this region of memory.

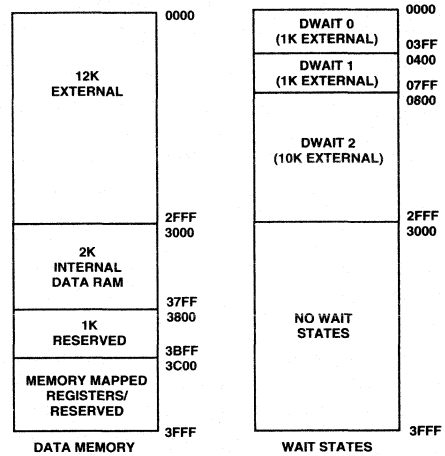


Figure 6. ADSP-2171 Data Memory Map

The remaining 12K of data memory is external. External data memory is divided into three zones, each associated with its own wait state generator. By mapping peripherals into different zones, you can accommodate peripherals with different wait state requirements. All zones default to 7 wait states after $\overline{RESET}$. For compatibility with other ADSP-2100 Family processors, bit definitions for DWAIT 3 and DWAIT4 are shown in the Data Memory Wait State Control Register, but they are not used by the ADSP-2171.

Bus Request & Bus Grant
The ADSP-2171 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2171 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If the Go Mode is enabled, the ADSP-2171 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2171 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes, which can be up

to eight cycles later depending on the number of wait states. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The new Bus Grant Hang logic and associated $\overline{BGH}$ pin allow the user to operate in a multiprocessor environment with a minimal number of "wasted" processor cycles. The bus grant hang pin is asserted when the ADSP-2171 desires a cycle, but cannot execute it because the bus is granted to some other processor. With the new $\overline{BGH}$ pad, the other processor(s) in the system can be alerted that the ADSP-2171 is hung and release the bus by deasserting bus request. Once the bus is released the ADSP-2171 executes the external access and deasserts bus grant hang. This is a signal to the other processors that external memory is now available.

ADSP-2171 REGISTERS

Figure 7 summarizes all the registers in the ADSP-2171. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

A secondary set of registers in all computational units allows a single-cycle context switch.

The bit and field definitions for control and status registers are given in the rest of this section, except for IMASK, ICNTL and IFC, which are defined earlier in this data sheet. The system control register, DWAIT register, timer registers, HIP control registers, HIP data registers, and SPORT control registers are all mapped into data memory; that is, registers are accessed by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

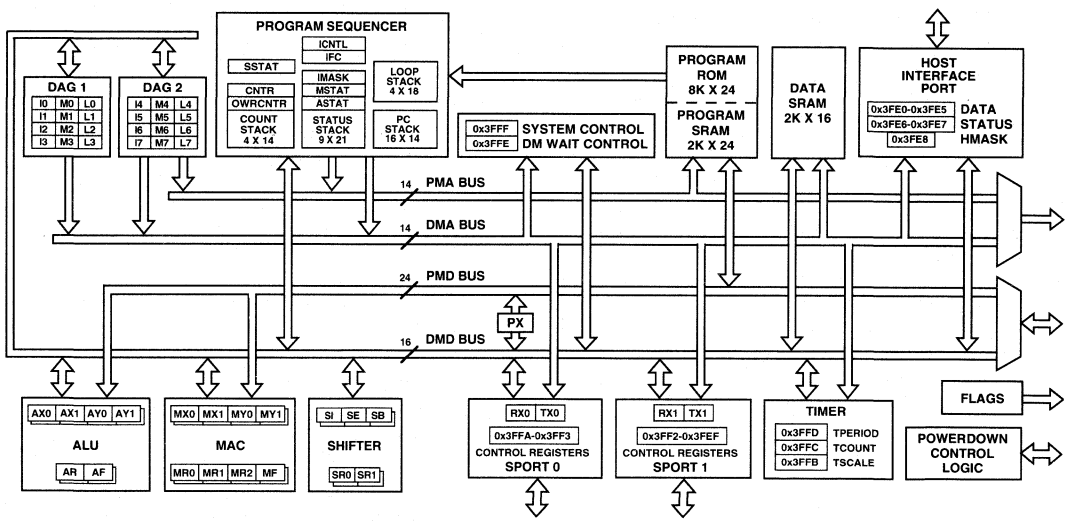
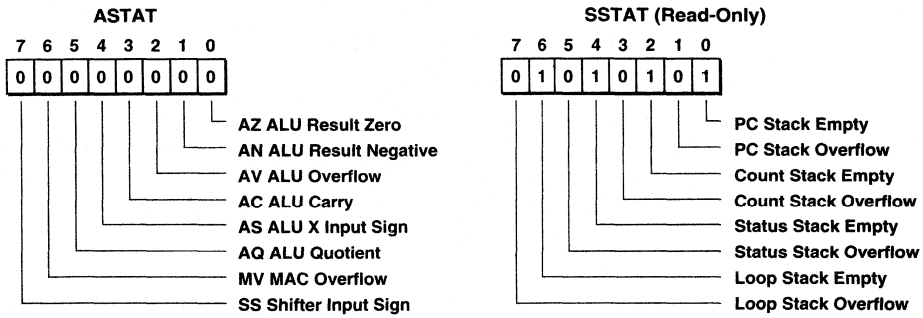
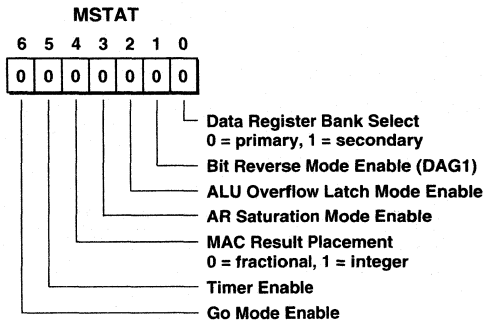
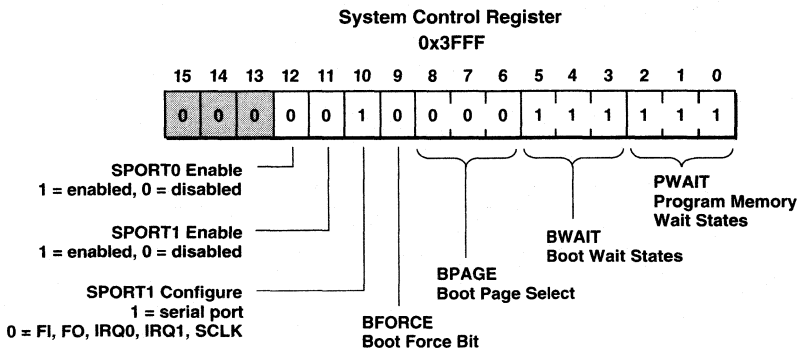
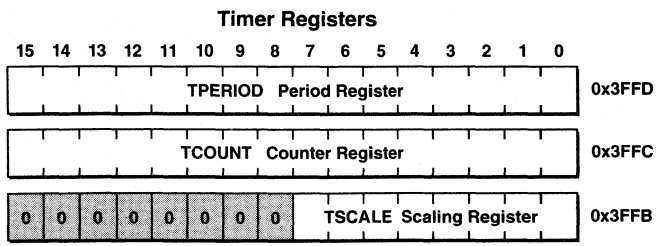


Figure 7. ADSP-2171 Registers Control Register



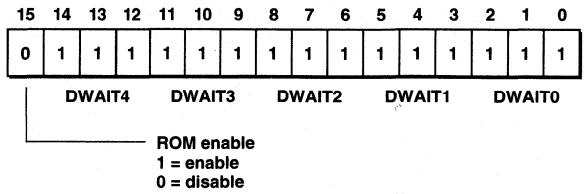






Control Registers

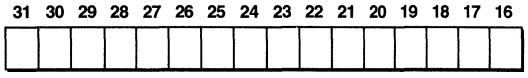
ROM Enable/Data Memory Wait State Control Register
0x3FFE



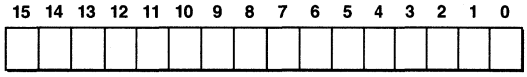
SPORT0 Multichannel Receive Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

0x3FFA



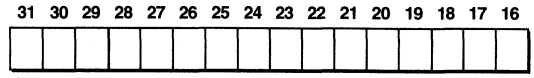
0x3FF9



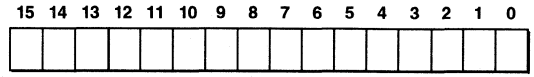
SPORT0 Multichannel Transmit Word Enable Registers

1 = Channel Enabled
0 = Channel Ignored

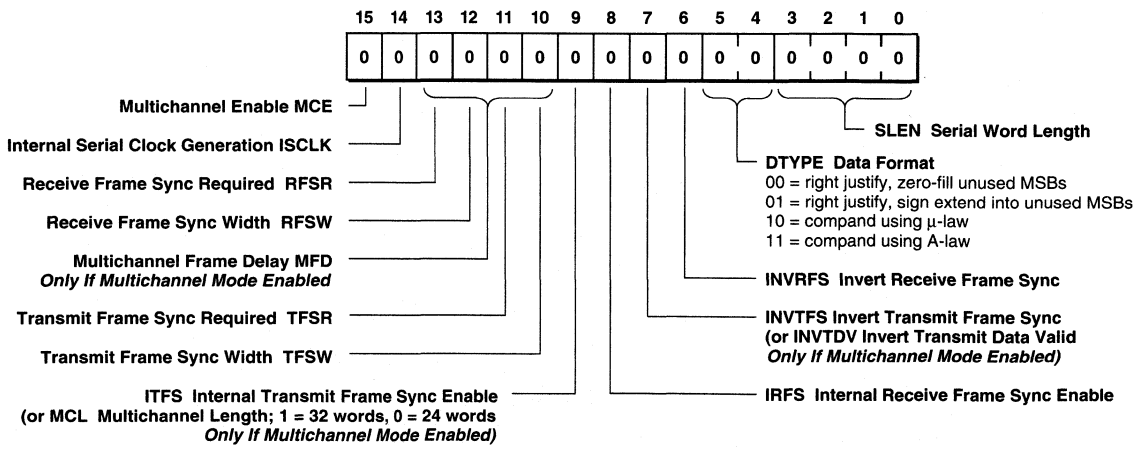
0x3FF8



0x3FF7

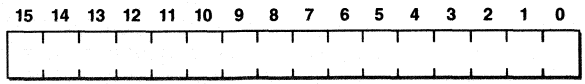


SPORT0 Control Register
0x3FF6

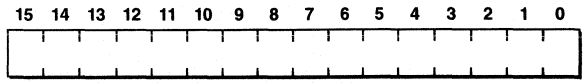


Control Registers

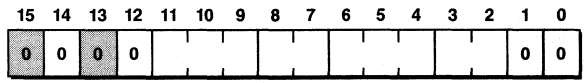
SPORT0 SCLKDIV
Serial Clock Divide Modulus
0x3FF5



SPORT0 RFSDIV
Receive Frame Sync Divide Modulus
0x3FF4



SPORT0 Autobuffer Control Register
0x3FF3



CLKODIS
CLKOUT Disable Control Bit

BIASRND
MAC Biased Rounding Control Bit

TIREG
Transmit Autobuffer I Register

TMREG
Transmit Autobuffer M Register

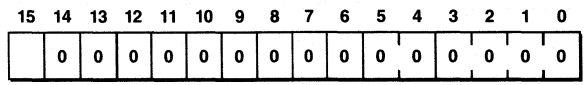
RBUF
Receive Autobuffering Enable

TBUF
Transmit Autobuffering Enable

RMREG
Receive Autobuffer M Register

RIREG
Receive Autobuffer I Register

SPORT1 Control Register
0x3FF2



Flag Out (Read Only)

Internal Serial Clock Generation ISCLK

Receive Frame Sync Required RFSR

Receive Frame Sync Width RFSW

Transmit Frame Sync Required TFSR

Transmit Frame Sync Width TFSW

ITFS Internal Transmit Frame Sync Enable

SLEN Serial Word Length

DTYPE Data Format
00 = right justify, zero-fill unused MSBs
01 = right justify, sign extend into unused MSBs
10 = compand using μ-law
11 = compand using A-law

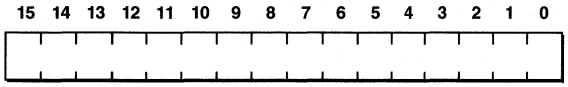
INVRFS Invert Receive Frame Sync

INVTFS Invert Transmit Frame Sync

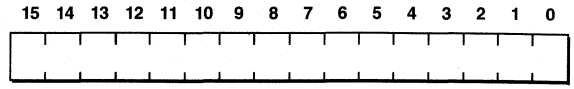
IRFS Internal Receive Frame Sync Enable

Control Registers

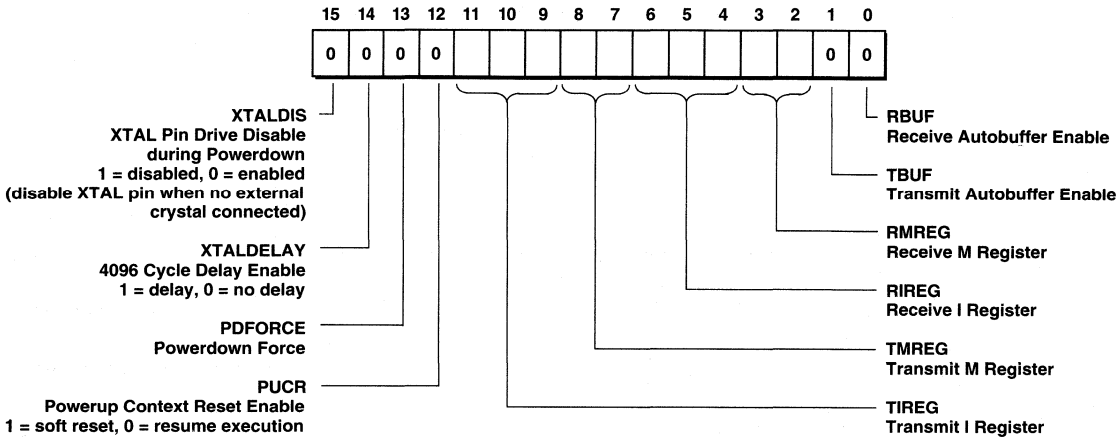
SPORT1 SCLKDIV
Serial Clock Divide Modulus
0x3FF1



SPORT1 RFSDIV
Receive Frame Sync Divide Modulus
0x3FF0

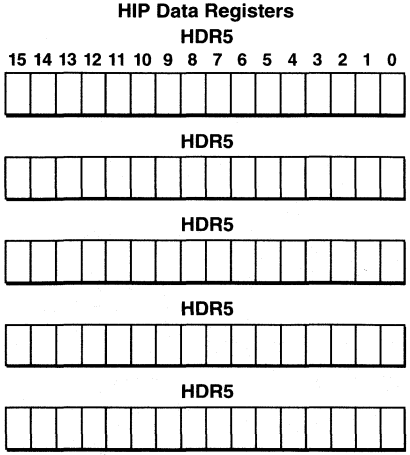


SPORT1 Autobuffer Control Register
0x3FEF

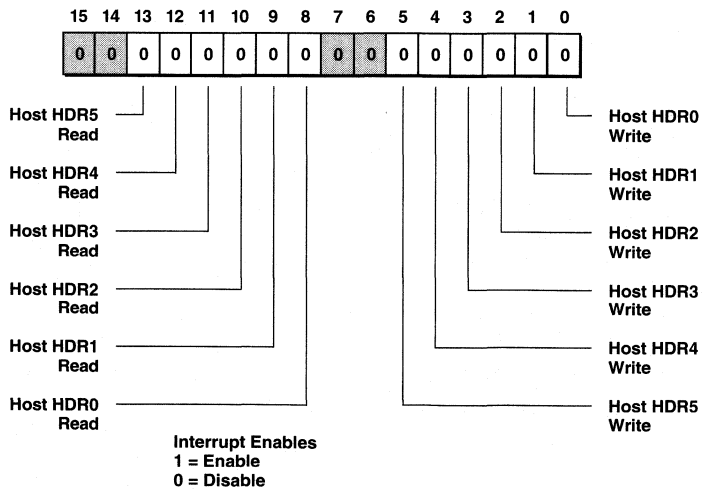


HIP Data Registers

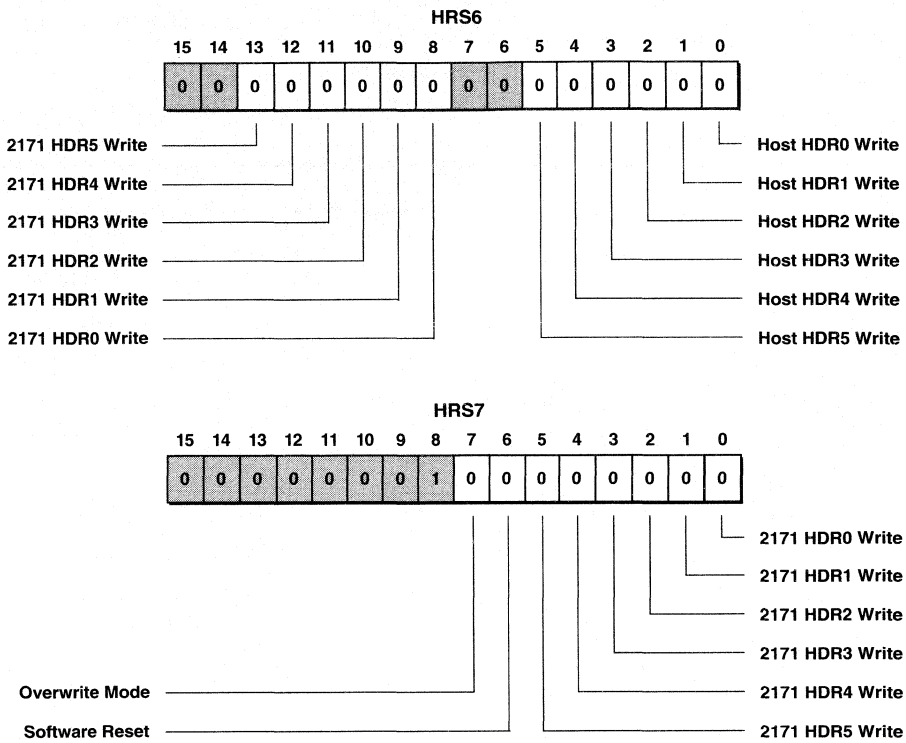
HDR5
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0



HMASK Register



Control Registers



Control Registers

INSTRUCTION SET DESCRIPTION

The ADSP-2171 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize internal memory and conform to the ADSP-2171's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

The ADSP-2171 supports the ADSP-2100 Family instruction set. This section only includes detailed descriptions of the instructions that are unique to the ADSP-2171. Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

New Instructions & Operations

This section discusses the new instructions and operations available on the ADSP-2171. Syntax, examples and detailed descriptions of each instruction follow.

Slow IDLE

The IDLE instruction on the ADSP-2171 supports a "slow idle" feature. Slow IDLE allows slowing the clock down by a factor of 16, 32, 64, or 128 during IDLE. The instruction source code is specified as follows:

Syntax: IDLE (n);

Permissible n Values
16, 32, 64, 128

Examples: IDLE;
IDLE (16);

Description: The IDLE instruction causes the processor to wait indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. The optional value provides a "slow idle" feature; slowing the clock down by the factor set with the value.

ALU xop Operations

ALU operations support constants in addition to *yop*s. These constants are available for all nonmultifunction ALU operations using both X and Y operands except *DIVS*. The instruction source code is specified as follows:

Syntax: [IF condition] | AR / AF | = xop function | yop / value |

Permissible xops

AX0, AX1, AR, MR0, MR1, MR2, SR0, SR1

Permissible functions

ADD/ADD with CARRY, SUBTRACT X–Y/SUBTRACT X–Y with BORROW, SUBTRACT Y–X/SUBTRACT Y–X with BORROW, AND, OR, XOR

Permissible yops and values

AY0, AY1, AF, 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32767, -2, -3, -5, -9, -17, -33, -65, -129, -257, -513, -1025, -2049, -4097, -8193, -16385, -32768

Permissible Conditions

EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Examples:
```
AR=AR+1;
AR=MR1 - 33;
IF GT AF=AX1 OR 16;
```

Description: Test the optional condition and, if true, perform the specified function. If false then perform a no-operation. Omitting the condition performs the function unconditionally. The operands are contained in the data registers specified in the instruction or optionally a value may be used.

ALU Bit Operations

The new ALU *xop* operations instructions allow you to code bit test, set, clear, and toggle operations through careful choice of the constant and ALU function. For streamlined programming, the source code for these operations can also be specified as:

Syntax: [IF condition] | AR / AF | = | TSTBIT n of xop; / SETBIT n of xop; / CLRBIT n of xop; / TGLBIT n of xop; |

Permissible xops

AX0, AX1, AR, MR0, MR1, MR2, SR0, SR1

Permissible Conditions

EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Permissible n Values (0 = LSB)

0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15

Examples:
```
AF=TSTBIT 5 of AR;
IF NE JUMP SET;
/* JUMP TO SET IF BIT IS SET */
```

Definitions of Operations

TSTBIT is an AND operation with a 1 in the selected bit
SETBIT is an OR operation with a 1 in the selected bit
CLRBIT is an AND operation with a 0 in the selected bit
TGLBIT is an XOR operation with a 1 in the selected bit

ALU PASS Operations

The ALU PASS operation on the ADSP-2171 supports a new list of constants in addition to yops. The instruction source code is specified as follows:

Syntax: [IF condition] | AR / AF | = pass | yop / value |

Permissible yops and values

AY0, AY1, AF, 0, 1, 2, 3, 4, 5, 7, 8, 9, 15, 16, 17, 31, 32, 33, 63, 64, 65, 127, 128, 129, 255, 256, 257, 511, 512, 513, 1023, 1024, 1025, 2047, 2048, 2049, 4095, 4096, 4097, 8191, 8192, 8193, 16383, 16384, 16385, 32766, 32767, –1, –2, –3, –4, –5, –6, –8, –9, –10, –16, –17, –18, –32, –33, –34, –64, –65, –66, –128, –129, –130, –256, –257, –258, –512, –513, –514, –1024, –1025, –1026, –2048, –2049, –2050, –4096, –4097, –4098, –8192, –8193, –8194, –16384, –16385, –16386, –32767, –32768

Permissible Conditions

EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Example:
```
IF GE AR = PASS AY0;
IF EQ AF = PASS -1025;
```

Description: Test the optional condition and, if true, pass the source operand unmodified through the ALU block and store in the destination location. If the condition is not true, perform a no-operation. Omitting the condition performs the *pass* unconditionally. The source operand is contained in the data registers specified in the instruction or optional value.

The PASS instruction performs the transfer to the AR register and affects the status flag; this instruction is different from a register move operation which does not affect any status flags. PASS 0 is one method of clearing AR. PASS 0 can also be combined in a multifunction instruction in conjunction with memory reads and writes to clear AR.

Note: The ALU status flags (in the ASTAT register) are not defined for the execution of this instruction when using the constant values other than 0, 1, and –1.

MAC Operations

The ADSP-2171 has a modified MAC which allows additional "type 9" instructions. The conditional ALU/MAC instruction has been modified to allow the X operand to be used as the Y operand as well. This allows a single cycle X^2, and also ΣX^2 operations.

The new MAC instructions allow the use of any *xop* as both the X and Y operands. The instructions source code is specified as follows:

Syntax: [IF condition] | MR / MF | = | [MR +] / [MR –] | xop * yop | (UU); / (SS); / (RND); |

Permissible xops

AR, MR0, MR1, MR2, MX0, MX1, SR0, SR1

Permissible Conditions
EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Example: IF LT MR=MR+ SR0*SR0 (SS);

Note: Both X operators must be the same register.

Biased Rounding
A new mode has been added to allow biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding odd MR1 values up. For example:

MR value before RND	biased RND result	unbiased RND result
00-0000-8000	00-0001-8000	00-0000-8000
00-0001-8000	00-0002-8000	00-0002-8000
00-0000-8001	00-0001-8001	00-0001-8001
00-0001-8001	00-0002-8001	00-0002-8001
00-0000-7FFF	00-0000-7FFF	00-0000-7FFF
00-0001-7FFF	00-0001-7FFF	00-0001-7FFF

This mode only has an effect when the MR0 register contains 0x8000, all other rounding operation work normally. This mode was added to allow more efficient implementation of bit specified algorithms which specify biased rounding such as the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
  MF=MX0*MY1 (RND), MX0=DM (I2,M1);   /* MF=error*beta */
  MR=MX0*MF (RND), AY0=PM (I6,MS);
DO adapt UNTIL CE;
  AR=MR1 + AY0, MX0=DM (I2,M1), AY0=PM (I6,M7);
adapt:  PM(I6,M6) =AR, MR=MX0*MF (RND);
        MODIFY (I2, M3);            /* Point to oldest data */
        MODIFY (I6, M7);            /* Point to start of data */
```

Interrupt Enable
The ADSP-2171 supports an interrupt enable instruction. Interrupts are enabled by default at reset. The instruction source code is specified as follows:

Syntax: ENA INTS;

Description: Executing the ENA INTS instruction allows all unmasked interrupts to be serviced again.

Interrupt Disable
The ADSP-2171 supports an interrupt disable instruction.The instruction source code is specified as follows:

Syntax: DIS INTS;

Description: Reset enables interrupt servicing. Executing the DIS INTS instruction causes all interrupts to be masked without changing the contents of the IMASK register. Disabling interrupts does not affect the autobuffer circuitry, which will operate normally whether or not interrupts are enabled. The disable interrupt instruction masks all user interrupts including the powerdown interrupt.

ADSP-2171–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.5	5.5	4.5	5.5	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IH}	Hi-Level RESET Voltage	@ V_{DD} = max	2.0		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min I_{OH} = –100 mA[6]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max[8]		10	µA
I_{OZL}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V[8]		10	µA
I_{DD}	Supply Current (Idle)[9, 10]	@ V_{DD} = max		17 (33 MIPS) 15 (26 MIPS)	mA mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DD} = max t_{CK} = 30 ns[11]		75 (33 MIPS) 62 (26 MIPS)	mA mA
I_{DD}	Supply Current (Powerdown)[10]	Lowest Power Mode[12]		100	µA
C_I	Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF
C_O	Output Pin Capacitance[6, 7, 13, 14]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = 25°C		8	pF

NOTES

[1]Bidirectional pins: D0-D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, HD0-HD15/HAD0-HAD15.

[2]Input only pins: $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[3]Input only pins: CLKIN, $\overline{\text{RESET}}$, $\overline{\text{IRQ2}}$, $\overline{\text{BR}}$, MMAP, DR0, DR1, $\overline{\text{HSEL}}$, HSIZE, BMODE, HMD0, HMD1, $\overline{\text{HRD}}$/HWR, $\overline{\text{HWR}}$/$\overline{\text{HDS}}$, $\overline{\text{PWD}}$, HA2/ALE, HA1-0.

[4]Output pins: $\overline{\text{BG}}$, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, PWDACK, A0-A13, DT0, DT1, CLKOUT, $\overline{\text{HACK}}$, FL2-0, $\overline{\text{BGH}}$.

[5]Although specified for TTL outputs, all ADSP-2171 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.

[6]Guaranteed but not tested.

[7]Three-statable pins: A0-A13, D0-D23, $\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RSF1, HD0-HD15/HAD0-HAD15.

[8]0 V on $\overline{\text{BR}}$, CLKIN Active (to force three-state condition).

[9]Idle refers to ADSP-2171 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND. Current reflects device operation with CLKOUT disabled.

[10]Current reflects device operating with no output loads.

[11]V_{IN} = 0.4 V and 2.4 V. For typical figures for supply currents, refer to "Power Dissipation" section.

[12]See Chapter 9, of the *ADSP-2100 Family User's Manual* for details.

[13]Applies to TQFP and PQFP package types.

[14]Output pin capacitance is the capacitve load for any three-state output pin.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage ..... –0.3 V to +7 V
Input Voltage ..... –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing ..... –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) .... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (5 sec) TQFP ..... +280°C
Lead Temperature (5 sec) PQFP ..... +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The ADSP-2171 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2171 features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-2171 has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2171 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	Address Setup to WriteStart
t_{AW}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ before $\overline{WR}$ Deasserted	Setup Address Setup to Write End
t_{WRA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0-A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid	Address Access Time

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2171 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock (which is equivalent to 60 ns) yields a 30 ns processor cycle (equivalent to 33 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value. Example: $t_{CKH} = 0.5t_{CK} - 7$ ns = 0.5 (30 ns) – 7 ns = 8 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	60 (33 MIPS) 76.92 (26 MIPS)	150	ns ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

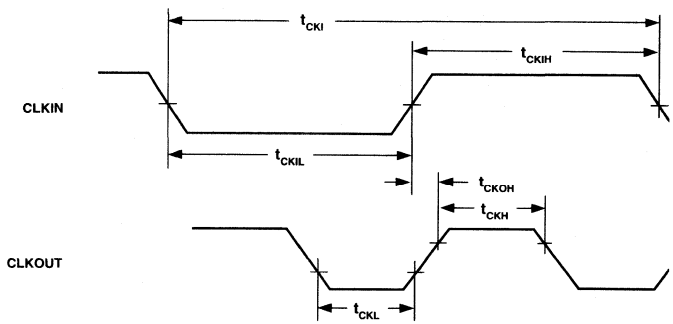


Figure 8. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flags				
Timing Requirement:				
t_{IFS}	$\overline{IRQx}$ or FI Setup before CLKOUT Low[1, 2, 3]	$0.25t_{CK} + 15$		ns
t_{IFH}	$\overline{IRQx}$ or FI Hold after CLKOUT High[1, 2, 3]	$0.25t_{CK}$		ns
Switching Characteristic:				
t_{FOH}	Flag Output Hold after CLKOUT Low[4]	$0.5t_{CK} - 7$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[4]		$0.5t_{CK} + 5$	ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[4]Flag Output = FL0, FL1, FL2, and FO.

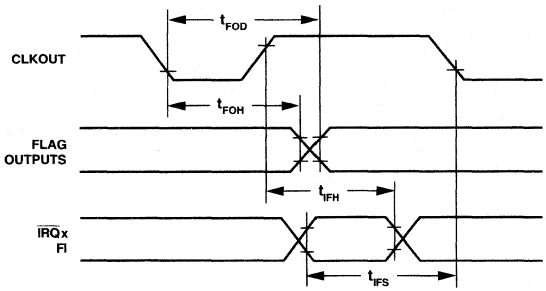


Figure 9. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK}$ +2		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK}$ + 17		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK}$ + 10	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK}$ – 7		ns
t_{SDBH}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

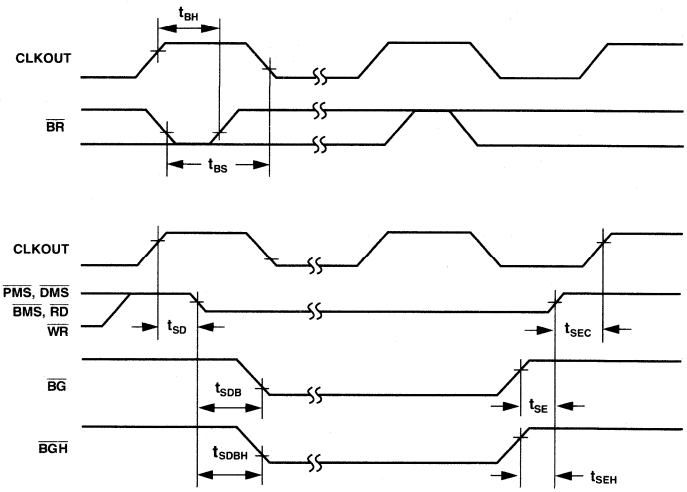


Figure 10. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 9 + w$ (33 MIPS)	ns
			$0.5t_{CK} - 11 + w$ (26 MIPS)	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		$0.75t_{CK} - 10.5 + w$ (33 MIPS)	ns
			$0.75t_{CK} - 12 + w$ (26 MIPS)	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}.

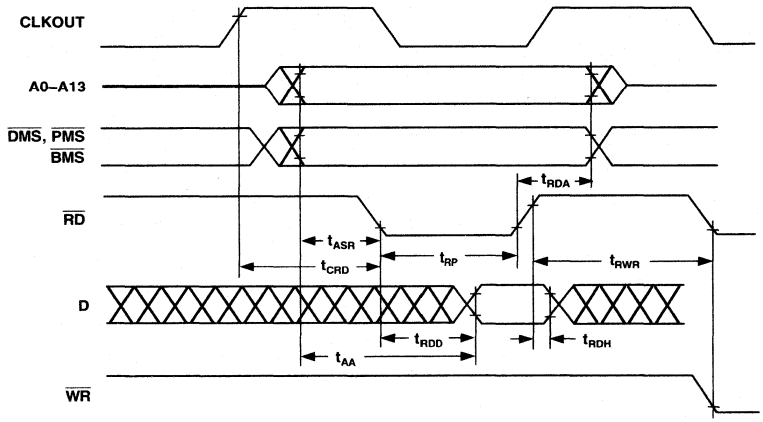


Figure 11. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	0.5 t_{CK} – 7 + w		ns
t_{DH}	Data Hold after $\overline{WR}$ High	0.25t_{CK} – 2		ns
t_{WP}	$\overline{WR}$ Pulse Width	0.5t_{CK} – 5 + w		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	0.25t_{CK} – 6		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	0.25t_{CK} – 6		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	0.25t_{CK} – 5	0.25 t_{CK} + 7	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	0.75t_{CK} – 9 + w		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted	0.25t_{CK} – 3		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	0.5t_{CK} – 5		ns

w = wait states x t_{CK}.

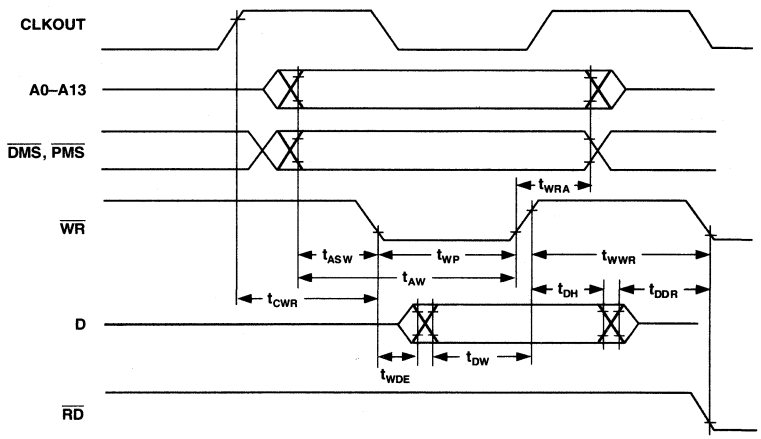


Figure 12. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	50		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	20		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS(Alt) to DT Enable	0		ns
t_{TDV}	TFS(Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

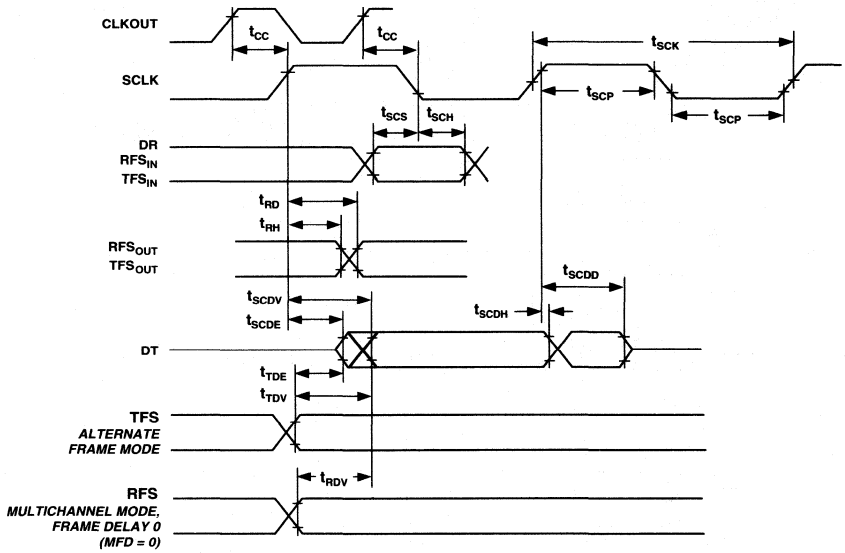
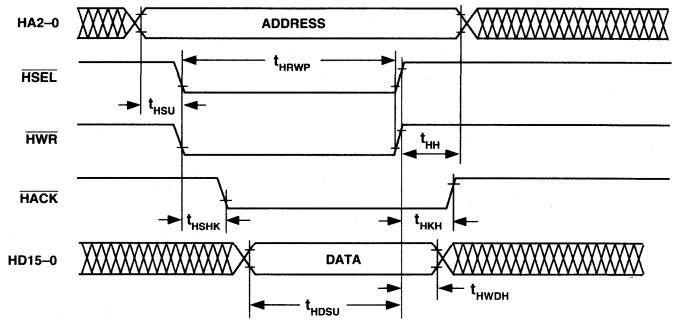


Figure 13. Serial Ports

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMDI = 0)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HSU}	HA2–0 Setup before Start of Write or Read[1, 2]	5		ns
t_{HDSU}	Data Setup before End of Write[3]	5		ns
t_{HWDH}	Data Hold after End of Write[3]	3		ns
t_{HH}	HA2–0 Hold after End of Write or Read[3, 4]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	15	ns
t_{HDE}	Data Enabled after Start of Read[2]	0		ns
t_{HDD}	Data Valid after Start of Read[2]		18	ns
t_{HRDH}	Data Hold after End of Read[4]	0		ns
t_{HRDD}	Data Disabled after End of Read[4]		7	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

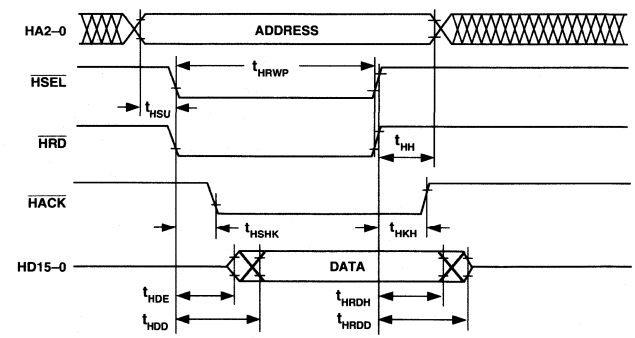
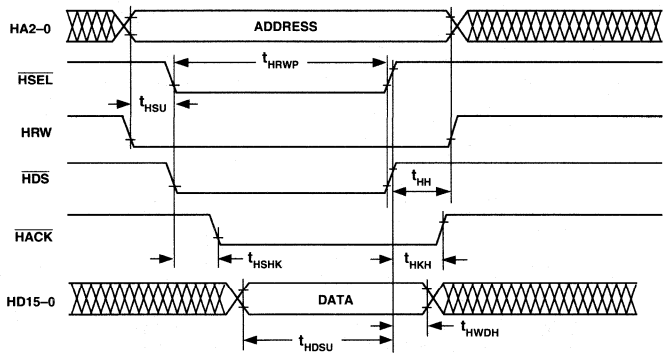


Figure 14. Host Interface Port (HMD1 = 0, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Separate Data and Address (HMD1 = 0)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HSU}	HA2–0, HRW Setup before Start of Write or Read[1]	5		ns
t_{HDSU}	Data Setup before End of Write[2]	5		ns
t_{HWDH}	Data Hold after End of Write[2]	3		ns
t_{HH}	HA2–0, HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	15	ns
t_{HDE}	Data Enabled after Start of Read[1]	0		ns
t_{HDD}	Data Valid after Start of Read[1]		18	ns
t_{HRDH}	Data Hold after End of Read[2]	0		ns
t_{HRDD}	Data Disabled after End of Read[2]		7	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

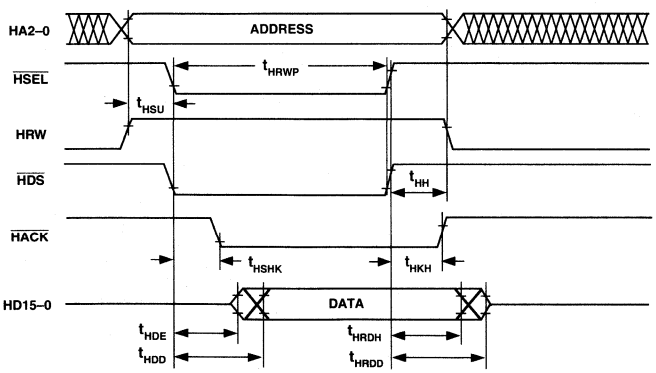
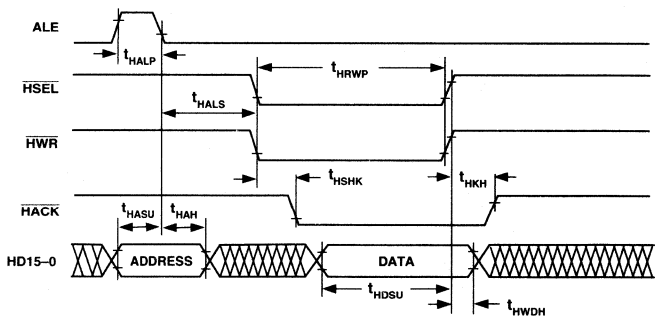


Figure 15. Host Interface Port HMD1 = 0, HMD0 = 1)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 0)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	10		ns
t_{HASU}	HAD15–0 Address Setup, before ALE Low	5		ns
t_{HAH}	HAD 15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1, 2]	10		ns
t_{HDSU}	HAD 15–0 Data Setup before End of Write[3]	5		ns
t_{HWDH}	HAD 15–0 Data Hold after End of Write[3]	3		ns
t_{HRWP}	Read or Write Pulse Width[5]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1, 2]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[3, 4]	0	15	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[2]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[2]		18	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[4]		7	ns

NOTES
[1]Start of Write = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.
[2]Start of Read = $\overline{HRD}$ Low and $\overline{HSEL}$ Low.
[3]End of Write = $\overline{HWR}$ High or $\overline{HSEL}$ High.
[4]End of Read = $\overline{HRD}$ High or $\overline{HSEL}$ High.
[5]Read Pulse Width = $\overline{HRD}$ Low and $\overline{HSEL}$ Low, Write Pulse Width = $\overline{HWR}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

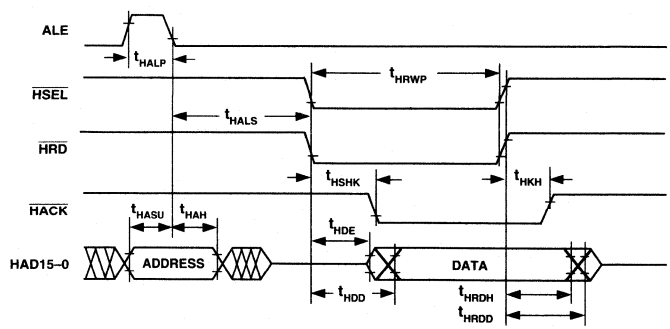
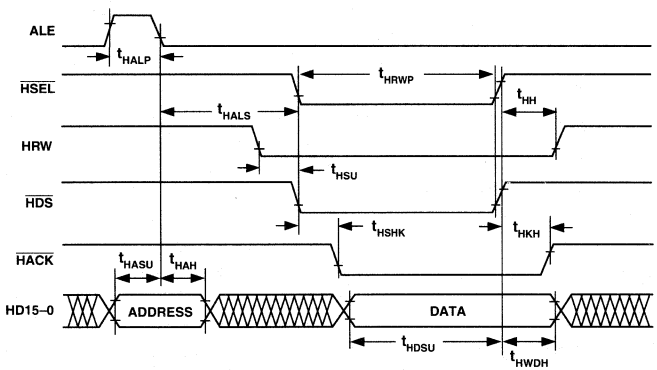


Figure 16. Host Interface Port (H MD1 = 1, HMD0 = 0)

Parameter		Min	Max	Unit
Host Interface Port				
Multiplexed Data and Address (HMD1 = 1)				
Read Strobe and Write Strobe (HMD0 = 1)				
Timing Requirement:				
t_{HALP}	ALE Pulse Width	10		ns
t_{HASU}	HAD15–0 Address Setup before ALE Low	5		ns
t_{HAH}	HAD15–0 Address Hold after ALE Low	2		ns
t_{HALS}	Start of Write or Read after ALE Low[1]	10		ns
t_{HSU}	HRW Setup before Start of Write or Read[1]	5		ns
t_{HDSU}	HAD15–0 Data Setup before End of Write[2]	5		ns
t_{HWDH}	HAD15–0 Data Hold after End of Write[2]	3		ns
t_{HH}	HRW Hold after End of Write or Read[2]	3		ns
t_{HRWP}	Read or Write Pulse Width[3]	20		ns
Switching Characteristic:				
t_{HSHK}	$\overline{HACK}$ Low after Start of Write or Read[1]	0	15	ns
t_{HKH}	$\overline{HACK}$ Hold after End of Write or Read[2]	0	15	ns
t_{HDE}	HAD15–0 Data Enabled after Start of Read[1]	0		ns
t_{HDD}	HAD15–0 Data Valid after Start of Read[1]		18	ns
t_{HRDH}	HAD15–0 Data Hold after End of Read[2]	0		ns
t_{HRDD}	HAD15–0 Data Disabled after End of Read[2]		7	ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High and $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle



Host Read Cycle

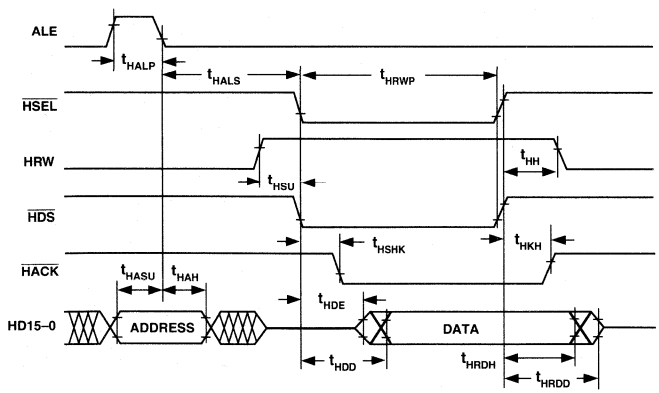


Figure 17. Host Interface Port (HMD1 = 1, HMD0 = 1)

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	50°C/W	2°C/W	48°C/W
PQFP	41°C/W	10°C/W	31°C/W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 30 ns.

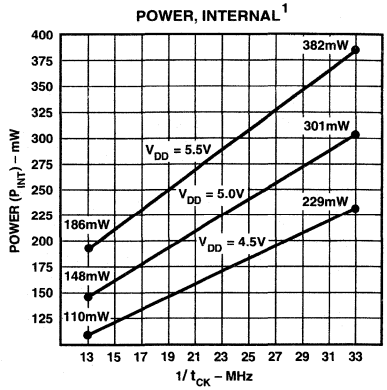
Total Power Dissipation = $P_{INT} + (C \times V_{DD}^2 \times f)$

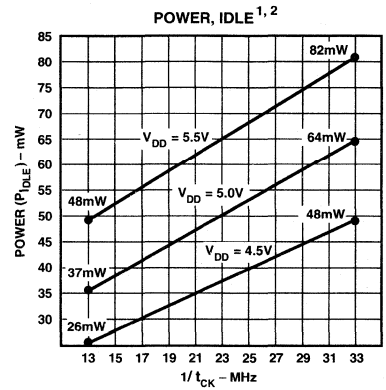
P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 18).

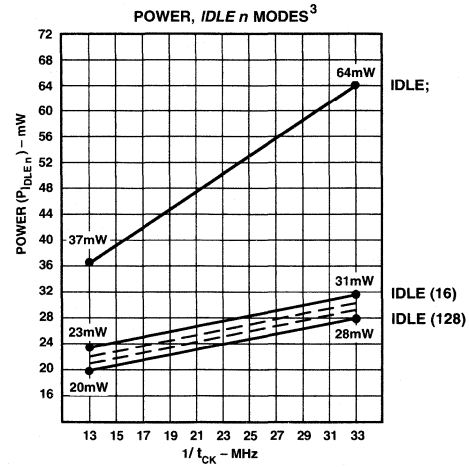
$(C \times V_{DD}^2 \times f)$ is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 33.3 MHz	=	66.6 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 16.67 MHz	=	37.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 16.67 MHz	=	4.2 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 33.3 MHz	=	8.3 mW
						116.6 mW

Total power dissipation for this example is P_{INT} + 116.6 mW.







VALID FOR ALL TEMPERATURE GRADES.

[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.

[2] IDLE REFERS TO ADSP-2171 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND. POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.

[3] TYPICAL POWER DISSIPATION AT 5.0V V_{DD} DURING EXECUTION OF *IDLE N* INSTRUCTION (CLOCK FREQUENCY REDUCTION). POWER REFLECTS DEVICE OPERATING WITH CLKOUT DISABLED.

Figure 18. Power vs. Frequency

CAPACITIVE LOADING

Figures 19 and 20 show the capacitive loading characteristics of the ADSP-2171.

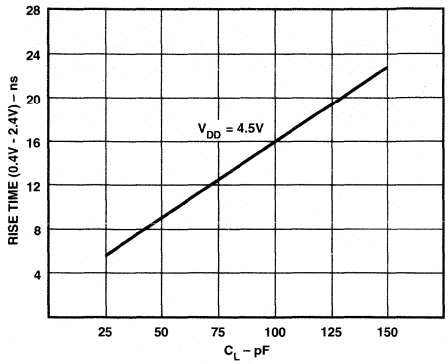


Figure 19. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

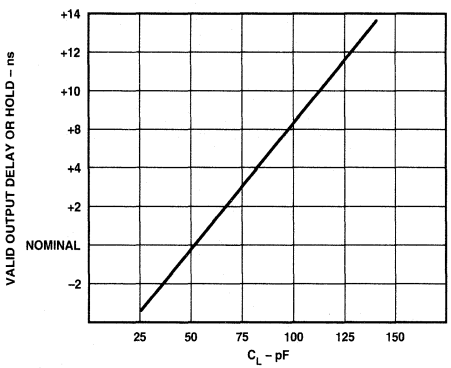


Figure 20. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitative load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5\,V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

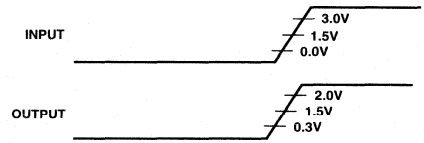


Figure 21. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when that have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

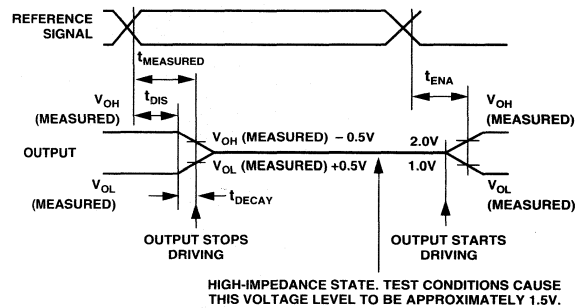


Figure 22. Output Enable/Disable

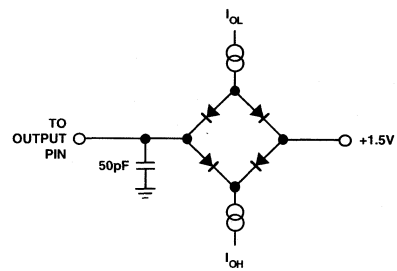
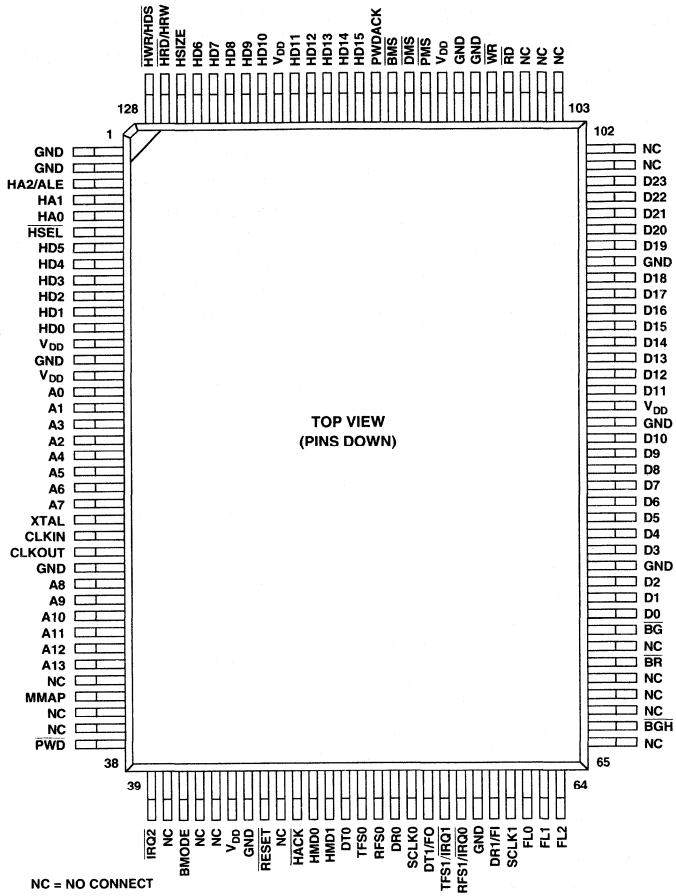


Figure 23. Equivalent Device Loading for AC Measurements (Including All Fixtures)

128-Lead TQFP Package Pinout



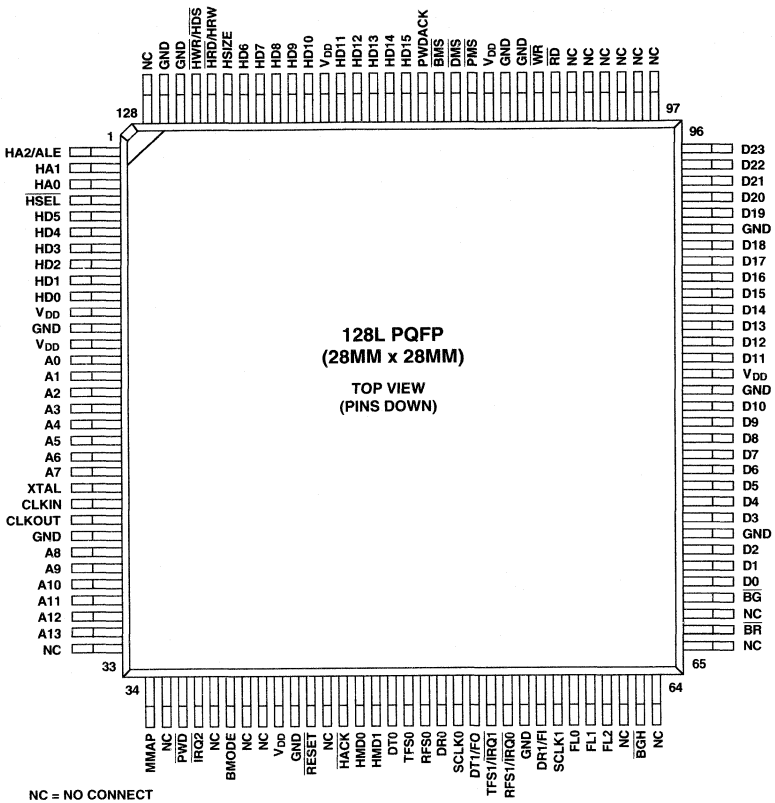
NC = NO CONNECT

TQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	GND	33	A13	65	NC	97	D20
2	GND	34	NC	66	$\overline{BGH}$	98	D21
3	HA2/ALE	35	MMAP	67	NC	99	D22
4	HA1	36	NC	68	NC	100	D23
5	HA0	37	NC	69	NC	101	NC
6	$\overline{HSEL}$	38	$\overline{PWD}$	70	$\overline{BR}$	102	NC
7	HD5	39	$\overline{IRQ2}$	71	NC	103	NC
8	HD4	40	NC	72	$\overline{BG}$	104	NC
9	HD3	41	BMODE	73	D0	105	NC
10	HD2	42	NC	74	D1	106	$\overline{RD}$
11	HD1	43	NC	75	D2	107	$\overline{WR}$
12	HD0	44	V_{DD}	76	GND	108	GND
13	V_{DD}	45	GND	77	D3	109	GND
14	GND	46	$\overline{RESET}$	78	D4	110	V_{DD}
15	V_{DD}	47	NC	79	D5	111	$\overline{PMS}$
16	A0	48	$\overline{HACK}$	80	D6	112	$\overline{DMS}$
17	A1	49	HMD0	81	D7	113	$\overline{BMS}$
18	A2	50	HMD1	82	D8	114	PWDACK
19	A3	51	DT0	83	D9	115	HD15
20	A4	52	TFS0	84	D10	116	HD14
21	A5	53	RFS0	85	GND	117	HD13
22	A6	54	DR0	86	V_{DD}	118	HD12
23	A7	55	SCLK0	87	D11	119	HD11
24	XTAL	56	DT1/FO	88	D12	120	V_{DD}
25	CLKIN	57	TFS1/$\overline{IRQ1}$	89	D13	121	HD10
26	CLKOUT	58	RFS1/$\overline{IRQ0}$	90	D14	122	HD9
27	GND	59	GND	91	D15	123	HD8
28	A8	60	DR1/F1	92	D16	124	HD7
29	A9	61	SCLK1	93	D17	125	HD6
30	A10	62	FL0	94	D18	126	HSIZE
31	A11	63	FL1	95	GND	127	$\overline{HRD}$/HRW
32	A12	64	FL2	96	D19	128	$\overline{HWR}$/$\overline{HDS}$

NC = These pins MUST remain unconnected.

128-Lead PQFP Package Pinout



PQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	HA2/ALE	33	MMAP	65	NC	97	NC
2	HA1	34	NC	66	BR	98	NC
3	HA0	35	PWD	67	NC	99	NC
4	HSEL	36	IRQ2	68	BG	100	NC
5	HD5	37	NC	69	D0	101	NC
6	HD4	38	BMODE	70	D1	102	NC
7	HD3	39	NC	71	D2	103	RD
8	HD2	40	NC	72	GND	104	WR
9	HD1	41	V_{DD}	73	D3	105	GND
10	HD0	42	GND	74	D4	106	GND
11	V_{DD}	43	RESET	75	D5	107	V_{DD}
12	GND	44	NC	76	D6	108	PMS
13	V_{DD}	45	HACK	77	D7	109	DMS
14	A0	46	HMD0	78	D8	110	BMS
15	A1	47	HMD1	79	D9	111	PWDACK
16	A2	48	DT0	80	D10	112	HD15
17	A3	49	TFS0	81	GND	113	HD14
18	A4	50	RFS0	82	V_{DD}	114	HD13
19	A5	51	DR0	83	D11	115	HD12
20	A6	52	SCLK0	84	D12	116	HD11
21	A7	53	DT1/FO	85	D13	117	V_{DD}
22	XTAL	54	TFS1/IRQ1	86	D14	118	HD10
23	CLKIN	55	RFS1/IRQ0	87	D15	119	HD9
24	CLKOUT	56	GND	88	D16	120	HD8
25	GND	57	DR1/F1	89	D17	121	HD7
26	A8	58	SCLK1	90	D18	122	HD6
27	A9	59	FL0	91	GND	123	HSIZE
28	A10	60	FL1	92	D19	124	HRD/HRW
29	A11	61	FL2	93	D20	125	HWR/HDS
30	A12	62	NC	94	D21	126	GND
31	A13	63	BGH	95	D22	127	GND
32	NC	64	NC	96	D23	128	NC

NC = These pins MUST remain unconnected.

ORDERING GUIDE

Part Number*	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option**
ADSP-2171KST-133	0°C to +70°C	33.33	128-Lead TQFP	ST-128
ADSP-2171BST-133	–40°C to +85°C	33.33	128-Lead TQFP	ST-128
ADSP-2171KS-133	0°C to +70°C	33.33	128-Lead PQFP	S-128
ADSP-2171BS-133	–40°C to +85°C	33.33	128-Lead PQFP	S-128
ADSP-2171KST-104	0°C to +70°C	26	128-Lead TQFP	ST-128
ADSP-2171BST-104	–40°C to +85°C	26	128-Lead TQFP	ST-128
ADSP-2171KS-104	0°C to +70°C	26	128-Lead PQFP	S-128
ADSP-2171BS-104	–40°C to +85°C	26	128-Lead PQFP	S-128

*S = Plastic Quad Flatpack, ST = Plastic Thin Quad Flatpack.
**For outline information see Package Information section.

ANALOG DEVICES

DSP Microcomputer

ADSP-2181

FEATURES

PERFORMANCE

30 ns Instruction Cycle Time from 16.67 MHz Crystal @ 5.0 Volts
33 MIPS Sustained Performance
Single-Cycle Instruction Execution
Single-Cycle Context Switch
Multifunction Instructions
Power-Down Mode Featuring Low CMOS Standby Power Dissipation with 100 Cycle Recovery from Power-Down Condition
Low Power Dissipation in Idle Mode

INTEGRATION

ADSP-2100 Family Code Compatible, with Extensions
80K Bytes of On-Chip RAM, Configured as 16K Words On-Chip Program Memory RAM 16K Words On-Chip Data Memory RAM
Dual Purpose Program Memory for Both Instruction and Data Storage
Independent ALU, Multiplier/Accumulator, & Barrel Shifter Computational Units
Two Independent Data Address Generators
Powerful Program Sequencer Provides Zero Overhead Looping Conditional Instruction Execution
Programmable 16-Bit Interval Timer with Prescaler
128-Lead TQFP/128-Lead PQFP

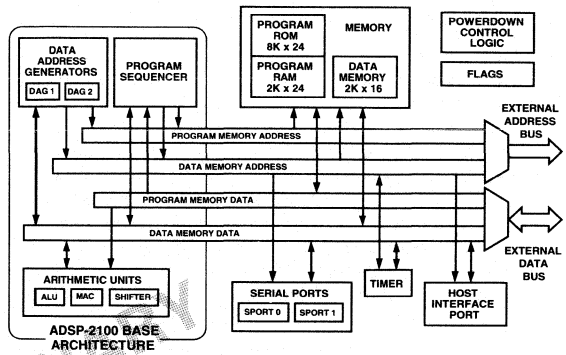
SYSTEM INTERFACE

16-Bit Internal DMA Port for High Speed Access to On-Chip Memory
8-Bit DMA Port to Byte Memory for Transparent Program and Data Memory Transfers
Byte Memory Interface for Storage of Data Tables & Program Overlays
Programmable Memory Strobe & Separate I/O Memory Space Permits "Glueless" System Design
Programmable Wait State Generation
Two Double-Buffered Serial Ports with Companding Hardware and Automatic Data Buffering
Automatic Booting of On-Chip Program Memory from Byte-Wide External Memory, e.g., EPROM, or Through Internal DMA Port
Six External Interrupts
13 Programmable Flag Pins Provide Flexible System Signaling
EZ-Port™ Emulator Interface Supports Debugging in End-User Systems

EZ-Port is a trademark of Analog Devices, Inc.

This is a preliminary data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADSP-2181 is a single-chip microcomputer optimized for digital signal processing (DSP) and other high speed numeric processing applications.

The ADSP-2181 combines the ADSP-2100 family base architecture (three computational units, data address generators and a program sequencer) with two serial ports, a 16-bit internal DMA port, a byte DMA port, a programmable timer, Flag I/O, extensive interrupt capabilities, and on-chip program and data memory.

The ADSP-2181 integrates 80K bytes of on-chip memory configured as 16K words (24-bit) of program RAM, and 16K words (16-bit) of data RAM. Power down circuitry is also provided to meet the low power needs of battery operated portable equipment. The ADSP-2181 is available in 128-pin TQFP and 128-pin PQFP packages.

In addition, the ADSP-2181 supports new instructions, which include bit manipulations—bit set, bit clear, bit toggle, bit test—new ALU constants, new multiplication instruction (x squared), biased rounding, result free ALU operations, I/O memory transfers, and global interrupt masking, for increased flexibility.

Fabricated in a high speed, double metal, low power, 0.6 μm CMOS process, the ADSP-2181 operates with a 30 ns instruction cycle time. Every instruction can execute in a single processor cycle.

The ADSP-2181's flexible architecture and comprehensive instruction set allow the processor to perform multiple operations in parallel. In one processor cycle the ADSP-2181 can:

- generate the next program address
- fetch the next instruction
- perform one or two data moves
- update one or two data address pointers
- perform a computational operation

This takes place while the processor continues to:

- receive and transmit data through the two serial ports
- receive and/or transmit data through the internal DMA port
- receive and/or transmit data through the byte DMA port
- decrement timer

Development System

The ADSP-2100 Family Development Software, a complete set of tools for software and hardware system development, supports the ADSP-2181. The System Builder provides a high level method for defining the architecture of systems under development. The Assembler has an algebraic syntax that is easy to program and debug. The Linker combines object files into an executable file. The Simulator provides an interactive instruction-level simulation with a reconfigurable user interface to display different portions of the hardware environment. A PROM Splitter generates PROM programmer compatible files. The C Compiler, based on the Free Software Foundation's GNU C Compiler, generates ADSP-2181 assembly source code. The source code debugger allows programs to be corrected in the C environment. The Runtime Library includes over 100 ANSI-standard mathematical and DSP-specific functions.

EZ-Tools, low cost, easy-to-use hardware tools, are available to support ADSP-2181 system development.

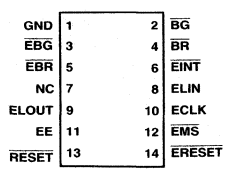
The ADSP-2181 EZ-ICE® Emulator aids in the hardware debugging of ADSP-2181 systems. The emulator consists of hardware, host computer resident software, and the target board connector. The ADSP-2181 integrates on-chip emulation support with a 14 pin EZ-Port. The EZ-Port allows in-circuit emulation without replacing the ADSP-2181. The emulator performs a full range of functions, including:

- stand-alone operation or operation in the target
- up to 20 breakpoints
- single-step or full-speed operation in the target
- registers and memory values can be examined and altered
- PC upload and download functions

If you plan to use the emulator, you should consider the emulator's restrictions (differences between emulator and processor operation).

An emulator header on the target board is used to connect the EZ-ICE to the target ADSP-2181's EZ-Port. The pins on the header *must* connect directly to the ADSP-2181 pins specified. The emulator header is a standard 14-pin, 2-row pin strip header with Pin 7 removed (key pin). The pins are 0.025 inch square and at least 0.20 inch in length. The pins are spaced at the standard 0.1 × 0.1 inches. Pin strip headers are available from vendors such as Samtec, 3M, McKenzie, and others.

The emulator header pinout is shown below.



Pin	Name	Description
1	GND	Ground
2	$\overline{BG}$	Bus Grant
3	$\overline{EBG}$	Emulator†
4	$\overline{BR}$	Bus Request
5	$\overline{EBR}$	Emulator†
6	$\overline{EINT}$	Emulator†
7	NC	Key Pin (NO Pin)
8	ELIN	Emulator†
9	ELOUT	Emulator†
10	ECLK	Emulator†
11	EE	Emulator†
12	$\overline{EMS}$	Emulator†
13	$\overline{RESET}$	Processor Reset Input
14	$\overline{ERESET}$	Emulator†

Pins marked by † must only be used for emulation by connection to the EZ-Port connector. Other pins may be safely used in other parts of your design. The designer should place the Emulator header such that signals that *only* connect between the DSP and the header are no longer than three inches.

Additional Information

This data sheet provides a general overview of ADSP-2181 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-2100 Family User's Manual.* For more information about the Development System and ADSP-2181 programmer's reference information, refer to the *ADSP-2100 Family Assembler Tools & Simulator Manual.*

ARCHITECTURE OVERVIEW

The ADSP-2181 instruction set provides flexible data moves and multifunction (one or two data moves with a computation) instructions. Every instruction can be executed in a single processor cycle. The ADSP-2181 assembly language uses an algebraic syntax for ease of coding and readability. A comprehensive set of development tools supports program development.

Figure 1 is an overall block diagram of the ADSP-2181. The processor contains three independent computational units: the ALU, the multiplier/accumulator (MAC) and the shifter. The computational units process 16-bit data directly and have provisions to support multiprecision computations. The ALU performs a standard set of arithmetic and logic operations; division primitives are also supported. The MAC performs single-cycle multiply, multiply/add and multiply/subtract operations with 40 bits of accumulation. The shifter performs logical and arithmetic shifts, normalization, denormalization, and derive exponent operations. The shifter can be used to efficiently implement numeric format control including multiword and block floating-point representations.

The internal result (R) bus connects the computational units so that the output of any unit may be the input of any unit on the next cycle.

EZ-ICE is a registered trademark of Analog Devices, Inc.

A powerful program sequencer and two dedicated data address generators ensure efficient delivery of operands to these computational units. The sequencer supports conditional jumps, subroutine calls and returns in a single cycle. With internal loop counters and loop stacks, the ADSP-2181 executes looped code with zero overhead; no explicit jump instructions are required to maintain loops.

Two data address generators (DAGs) provide addresses for simultaneous dual operand fetches (from data memory and program memory). Each DAG maintains and updates four address pointers. Whenever the pointer is used to access data (indirect addressing), it is post-modified by the value of one of four possible modify registers. A length value may be associated with each pointer to implement automatic modulo addressing for circular buffers.

Efficient data transfer is achieved with the use of five internal buses:

- Program Memory Address (PMA) Bus
- Program Memory Data (PMD) Bus
- Data Memory Address (DMA) Bus
- Data Memory Data (DMD) Bus
- Result (R) Bus

The two address buses (PMA and DMA) share a single external address bus, allowing memory to be expanded off-chip, and the two data buses (PMD and DMD) share a single external data bus. Byte memory space and I/O memory space also share the external buses.

Program memory can store both instructions and data, permitting the ADSP-2181 to fetch two operands in a single cycle, one from program memory and one from data memory. The ADSP-2181 can fetch an operand from program memory and the next instruction in the same cycle.

In addition to the address and data bus for external memory connection, the ADSP-2181 has a 16-bit Internal DMA port (IDMA port) for connection to external systems. The IDMA port is made up of 16 data/address pins and five control pins. The IDMA port provides transparent, direct access to the DSPs on-chip program and data RAM.

An interface to low cost byte-wide memory is provided by the Byte DMA port (BDMA port). The BDMA port is bidirectional and can directly address up to four megabytes of external RAM or ROM for off-chip storage of program overlays or data tables.

The byte memory and I/O memory space interface supports slow memories and I/O memory-mapped peripherals with programmable wait state generation. External devices can gain control of external buses with bus request/grant signals ($\overline{BR}$, $\overline{BGH}$, and $\overline{BG}$). One execution mode (Go Mode) allows the ADSP-2181 to continue running from on-chip memory. Normal execution mode requires the processor to halt while buses are granted.

The ADSP-2181 can respond to eleven interrupts. There can be up to six external interrupts (one edge-sensitive, two level-sensitive, and three configurable) and seven internal interrupts generated by the timer, the serial ports (SPORTs), the Byte DMA port, and the power-down circuitry. There is also a master $\overline{RESET}$ signal.

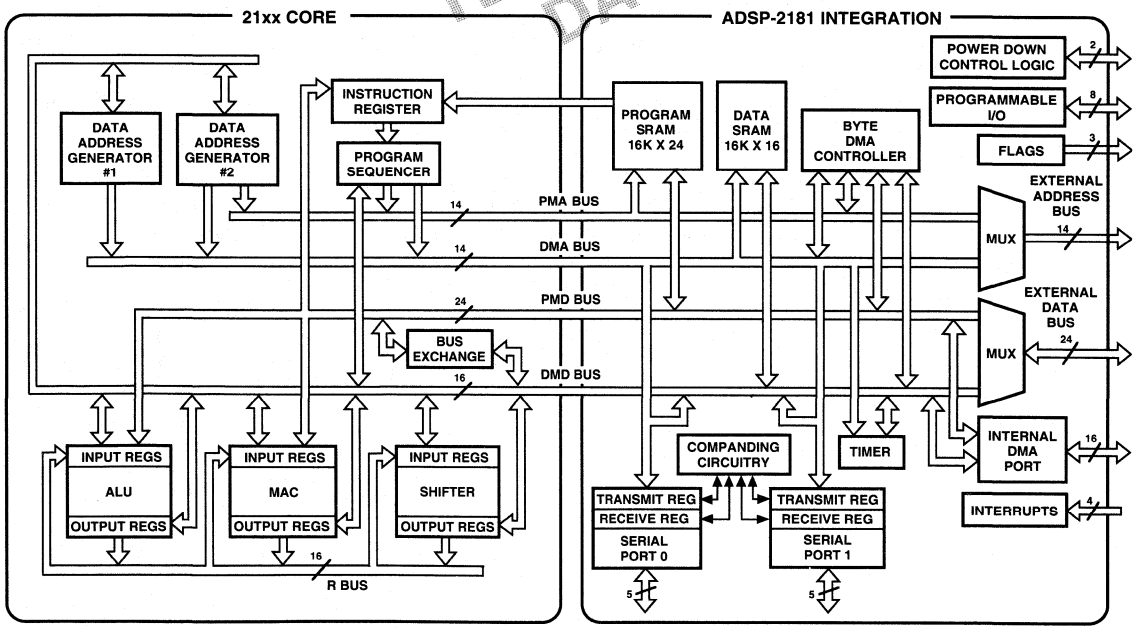


Figure 1. ADSP-2181 Block Diagram

The two serial ports provide a complete synchronous serial interface with optional companding in hardware and a wide variety of framed or frameless data transmit and receive modes of operation. Each port can generate an internal programmable serial clock or accept an external serial clock.

The ADSP-2181 provides up to 13 general-purpose flag pins. The data input and output pins on SPORT1 can be alternatively configured as an input flag and an output flag. In addition, there are eight flags that are programmable as inputs or outputs, and three flags that are always outputs.

A programmable interval timer generates periodic interrupts. A 16-bit count register (TCOUNT) is decremented every *n* processor cycles, where *n* is a scaling value stored in an 8-bit register (TSCALE). When the value of the count register reaches zero, an interrupt is generated and the count register is reloaded from a 16-bit period register (TPERIOD).

Serial Ports

The ADSP-2181 incorporates two complete synchronous serial ports (SPORT0 and SPORT1) for serial communications and multiprocessor communication.

Here is a brief list of the capabilities of the ADSP-2181 SPORTs. Refer to the *ADSP-2100 Family User's Manual* for further details.

- SPORTs are bidirectional and have a separate, double-buffered transmit and receive section.
- SPORTs can use an external serial clock or generate their own serial clock internally.
- SPORTs have independent framing for the receive and transmit sections. Sections run in a frameless mode or with frame synchronization signals internally or externally generated. Frame sync signals are active high or inverted, with either of two pulse widths and timings.
- SPORTs support serial data word lengths from 3 to 16 bits and provide optional A-law and μ-law companding according to CCITT recommendation G.711.
- SPORT receive and transmit sections can generate unique interrupts on completing a data word transfer.
- SPORTs can receive and transmit an entire circular buffer of data with only one overhead cycle per data word. An interrupt is generated after a data buffer transfer.
- SPORT0 has a multichannel interface to selectively receive and transmit a 24 or 32 word, time-division multiplexed, serial bitstream.
- SPORT1 can be configured to have two external interrupts ($\overline{IRQ0}$ and $\overline{IRQ1}$) and the Flag In and Flag Out signals. The internally generated serial clock may still be used in this configuration.

Pin Description

The ADSP-2181 is available in 128-lead TQFP and 128-lead PQFP packages.

PIN DESCRIPTIONS

Pin Group Name	# of Pins	Input/ Output	Function
Address	14	O	Address Output Pins for Program, Data, Byte, & I/O Spaces
Data	24	I/O	Data I/O Pins for the Program, and Data Spaces (Eight MSBs Are Also used as Byte Space Addresses)
$\overline{RESET}$	1	I	Processor Reset Input
$\overline{IRQ2}$	1	I	Edge or Level Sensitive Interrupt Requests
$\overline{IRQL0}$, $\overline{IRQL1}$	2	I	Level Sensitive Interrupt Requests
$\overline{IRQE}$	1	I	Edge Sensitive Interrupt Request
$\overline{BR}$	1	I	Bus Request Input
$\overline{BG}$	1	O	Bus Grant Output
$\overline{BGH}$	1	O	Bus Grant Hung Output
$\overline{PMS}$	1	O	Program Memory Select Output
$\overline{DMS}$	1	O	Data Memory Select Output
$\overline{BMS}$	1	O	Byte Memory Select Output
$\overline{IOMS}$	1	O	I/O Space Memory Select Output
$\overline{CMS}$	1	O	Combined Memory Select Output
$\overline{RD}$	1	O	Memory Read Enable Output
$\overline{WR}$	1	O	Memory Write Enable Output
MMAP	1	I	Memory Map Select Input
BMODE	1	I	Boot Option Control Input
CLKIN, XTAL	2	I	Clock or Quartz Crystal Input
CLKOUT	1	O	Processor Clock Output
SPORT0	5	I/O	Serial Port I/O Pins
SPORT1	5	I/O	Serial Port 1 *or* Two External $\overline{IRQ}$s, Flag In and Flag Out
$\overline{IRD}$, $\overline{IWR}$, $\overline{IS}$, IAL	4	I	IDMA Port Access Control Inputs
IAD	16	I/O	IDMA Port Address/Data Bus
$\overline{IACK}$	1	O	IDMA Port Access Acknowledge
$\overline{PWD}$	1	I	Power-Down Control
PWDACK	1	O	Power-Down Control
FL0, FL1, FL2	3	O	Output Flags
PF7:0	8	I/O	Programmable I/O Pins
GND	11		Ground Pins
V_{DD}	6		Power Supply Pins

Interrupts

The interrupt controller allows the processor to respond to the eleven possible interrupts and reset with minimum overhead. The ADSP-2181 provides four dedicated external interrupt input pins, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, and $\overline{IRQE}$. In addition, SPORT1 may be reconfigured for $\overline{IRQ0}$, $\overline{IRQ1}$, FLAG_IN and FLAG_OUT, for a total of six external interrupts. The ADSP-2181 also supports internal interrupts from the timer, the byte DMA port, the two serial ports, software, and the power-down control circuit. The interrupt levels are internally prioritized and individually maskable (except power down and reset). The $\overline{IRQ2}$, $\overline{IRQ0}$, and $\overline{IRQ1}$ input pins can be programmed to be either level- or edge-sensitive. $\overline{IRQL0}$ and $\overline{IRQL1}$ are level-sensitive and $\overline{IRQE}$ is edge sensitive. The priorities and vector addresses of all interrupts are shown in Table I, and the interrupt registers are shown in Figure 7.

Table I. Interrupt Priority & Interrupt Vector Addresses

Source of Interrupt	Interrupt Vector Address (Hex)	
Reset (or Power-Up with PUCR = 1)	0000	(*Highest Priority*)
Power Down (Nonmaskable)	002C	
$\overline{IRQ2}$	0004	
$\overline{IRQL1}$	0008	
$\overline{IRQL0}$	000C	
SPORT0 Transmit	0010	
SPORT0 Receive	0014	
$\overline{IRQE}$	0018	
BDMA Interrupt	001C	
SPORT1 Transmit or $\overline{IRQ1}$	0020	
SPORT1 Receive or $\overline{IRQ0}$	0024	
Timer	0028	(*Lowest Priority*)

Interrupt routines can either be nested with higher priority interrupts taking precedence or processed sequentially. Interrupts can be masked or unmasked with the IMASK register. Individual interrupt requests are logically ANDed with the bits in IMASK; the highest priority unmasked interrupt is then selected. The power-down interrupt is nonmaskable.

The ADSP-2181 masks all interrupts for one instruction cycle following the execution of an instruction that modifies the IMASK register. This does not affect autobuffering.

The interrupt control register, ICNTL, controls interrupt nesting and defines the $\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$ external interrupts to be either edge- or level-sensitive. The $\overline{IRQE}$ pin is an external edge sensitive interrupt and can be forced and cleared. The $\overline{IRQL0}$ and $\overline{IRQL1}$ pins are external level sensitive interrupts.

The IFC register is a write-only register used to force and clear interrupts.

On-chip stacks preserve the processor status and are automatically maintained during interrupt handling. The stacks are twelve levels deep to allow interrupt, loop, and subroutine nesting.

The following instructions allow global enable or disable servicing of the interrupts (including power down), regardless of the state of IMASK. Disabling the interrupts does not affect serial port autobuffering or DMA.

ENA INTS;
DIS INTS;

When the processor is reset, interrupt servicing is enabled.

LOW POWER OPERATION

The ADSP-2181 has three low power modes that significantly reduce the power dissipation when the device operates under standby conditions. These modes are:

- Power Down
- Idle
- Slow Idle

The CLKOUT pin may also be disabled to reduce external power dissipation.

Power Down

The ADSP-2181 processor has a low power feature that lets the processor enter a very low power dormant state through hardware or software control. Here is a brief list of power-down features. Refer to the *ADSP-2100 Family User's Manual*, Chapter 9 "System Interface" for detailed information about the power-down feature.

- Quick recovery from power down. The processor begins executing instructions in as few as 100 CLKIN cycles.
- Support for an externally generated TTL or CMOS processor clock. The external clock can continue running during power down without affecting the lowest power rating and 100 CLKIN cycle recovery.
- Support for crystal operation includes disabling the oscillator to save power (the processor automatically waits 4096 CLKIN cycles for the crystal oscillator to start and stabilize), and letting the oscillator run to allow 100 CLKIN cycle start up.
- Power down is initiated by either the power-down pin ($\overline{PWD}$) or the software power-down force bit.
- Interrupt support allows an unlimited number of instructions to be executed before optionally powering down. The power-down interrupt also can be used as a nonmaskable, edge sensitive interrupt.
- Context clear/save control allows the processor to continue where it left off or start with a clean context when leaving the power-down state.
- The $\overline{RESET}$ pin also can be used to terminate power down.
- Power-down acknowledge pin indicates when the processor has entered power down.

Idle

When the ADSP-2181 is in the Idle Mode, the processor waits indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the *IDLE* instruction.

Slow Idle

The *IDLE* instruction is enhanced on the ADSP-2181 to let the processor's internal clock signal be slowed, further reducing power consumption. The reduced clock frequency, a programmable fraction of the normal clock rate, is specified by a selectable divisor given in the *IDLE* instruction. The format of the instruction is

IDLE (n);

where n = 16, 32, 64, or 128. This instruction keeps the processor fully functional, but operating at the slower clock rate. While it is in this state, the processor's other internal clock signals, such as SCLK, CLKOUT, and timer clock, are reduced by the same ratio. The default form of the instruction, when no clock divisor is given, is the standard *IDLE* instruction.

When the *IDLE (n)* instruction is used, it effectively slows down the processor's internal clock and thus its response time to incoming interrupts. The one-cycle response time of the standard idle state is increased by n, the clock divisor. When an enabled interrupt is received, the ADSP-2181 will remain in the idle state for up to a maximum of n processor cycles (n = 16, 32, 64, or 128) before resuming normal operation.

When the *IDLE (n)* instruction is used in systems that have an externally generated serial clock (SCLK), the serial clock rate may be faster than the processor's reduced internal clock rate. Under these conditions, interrupts must not be generated at a faster rate than can be serviced, due to the additional time the processor takes to come out of the idle state (a maximum of n processor cycles).

SYSTEM INTERFACE

Figure 2 shows a typical basic system configuration with the ADSP-2181, two serial devices, a byte-wide EPROM, and optional external program and data overlay memories. Programmable wait state generation allows the processor connects easily to slow peripheral devices. The ADSP-2181 also provides four external interrupts and two serial ports or six external interrupts and one serial port.

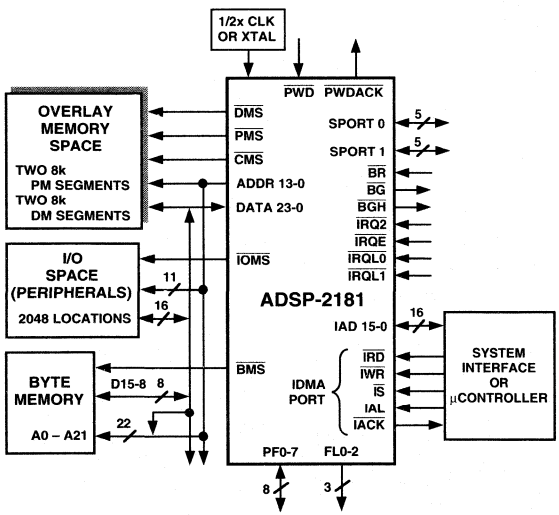


Figure 2. ADSP-2181 Basic System Configuration

Clock Signals

The ADSP-2181 can be clocked by either a crystal or by a TTL-compatible clock signal.

The CLKIN input cannot be halted, changed during operation, or operated below the specified frequency during normal operation. The only exception is while the processor is in the power-down state. For additional information, refer to Chapter 9, *ADSP-2100 Family User's Manual* for detailed information on this power-down feature.

If an external clock is used, it should be a TTL-compatible signal running at half the instruction rate. The signal is connected to the processor's CLKIN input. When an external clock is used, the XTAL input *must* be left unconnected.

The ADSP-2181 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock yields a 30 ns processor cycle (which is equivalent to 33 MHz). Normally, instructions are executed in a single processor cycle. All device timing is relative to the internal instruction clock rate, which is indicated by the CLKOUT signal when enabled.

Because the ADSP-2181 includes an on-chip oscillator circuit, an external crystal may be used. The crystal should be connected across the CLKIN and XTAL pins, with two capacitors connected as shown in Figure 3. Capacitor values are dependent on crystal type and should be specified by the crystal manufacturer. A parallel-resonant, fundamental frequency, microprocessor-grade crystal should be used.

A clock output (CLKOUT) signal is generated by the processor at the processor's cycle rate. This can be enabled and disabled by the CLKODIS bit in the SPORT0 Autobuffer Control Register.

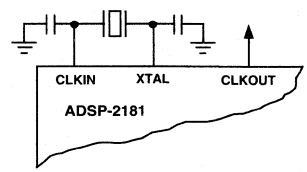


Figure 3. External Crystal Connections

Reset

The $\overline{\text{RESET}}$ signal initiates a master reset of the ADSP-2181. The $\overline{\text{RESET}}$ signal must be asserted during the power-up sequence to assure proper initialization. $\overline{\text{RESET}}$ during initial power-up must be held long enough to allow the internal clock to stabilize. If $\overline{\text{RESET}}$ is activated any time after power up, the clock continues to run and does not require stabilization time.

The power-up sequence is defined as the total time required for the crystal oscillator circuit to stabilize after a valid V_{DD} is applied to the processor, and for the internal phase-locked loop (PLL) to lock onto the specific crystal frequency. A minimum of 2000 CLKIN cycles ensures that the PLL has locked but does not include the crystal oscillator start-up time. During this

power-up sequence the $\overline{\text{RESET}}$ signal should be held low. On any subsequent resets, the $\overline{\text{RESET}}$ signal must meet the minimum pulse width specification, t_{RSP}.

The $\overline{\text{RESET}}$ input contains some hysteresis; however, if you use an RC circuit to generate your $\overline{\text{RESET}}$ signal, the use of an external Schmidt trigger is recommended.

The master reset sets all internal stack pointers to the empty stack condition, masks all interrupts and clears the MSTAT register. When $\overline{\text{RESET}}$ is released, if there is no pending bus request and the chip is configured for booting (MMAP = 0), the boot-loading sequence is performed. The first instruction is fetched from on-chip program memory location 0x0000 once boot loading completes.

Memory Architecture

The ADSP-2181 provides a variety of memory and peripheral interface options. The key functional groups are Program Memory, Data Memory, Byte Memory, and I/O.

Program Memory is a 24-bit-wide space for storing both instruction opcodes and data. The ADSP-2181 has 16K words of Program Memory RAM on chip, and the capability of accessing up to two 8K external memory overlay spaces using the external data bus. Both an instruction opcode and a data value can be read from on-chip program memory in a single cycle.

Data Memory is a 16-bit-wide space used for the storage of data variables and for memory-mapped control registers. The ADSP-2181 has 16K words on Data Memory RAM on chip, consisting of 16,352 user-accessible locations and 32 memory-mapped registers. Support also exists for up to two 8K external memory overlay spaces through the external data bus.

Byte Memory provides access to an 8-bit wide memory space through the Byte DMA (BDMA) port. The Byte Memory interface provides access to 4 MBytes of memory by utilizing eight data lines as additional address lines. This gives the BDMA Port an effective 22-bit address range. On power-up, the DSP can automatically load bootstrap code from byte memory.

I/O Space allows access to 2048 locations of 16-bit-wide data. It is intended to be used to communicate with parallel peripheral devices such as data converters and external registers or latches.

Program Memory

The ADSP-2181 contains a 16K × 24 on-chip program RAM. The on-chip program memory is designed to allow up to two accesses each cycle so that all operations can complete in a single cycle. In addition, the ADSP-2181 allows the use of 8K external memory overlays. Any external accesses in program memory space use the PWAIT register for wait states.

The program memory space organization is controlled by the MMAP pin and the PMOVLAY register. Normally, the ADSP-2181 is configured with MMAP = 0.

The program memory is organized as shown in Figure 4.

There are 16K words of memory accessible internally when the PMOVLAY register is set to 0. When PMOVLAY is set to something other than 0, external accesses occur at addresses 0x2000 through 0x3FFF. The external address is generated as shown in Table II.

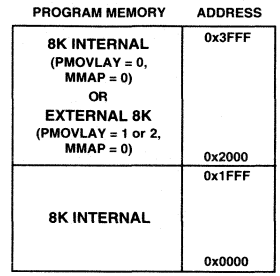


Figure 4. Program Memory (MMAP = 0)

Table II.

PMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x2000 and 0x3FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x2000 and 0x3FFF

This organization provides for two external 8K overlay segments using only the normal 14 address bits. This allows for simple program overlays using one of the two external segments in place of the on-chip memory. Care must be taken in using this overlay space in that the processor core (i.e., the sequencer) does not take into account the PMOVLAY register value. For example, if a loop operation was occurring on one of the external overlays and the program changes to another external overlay or internal memory, an incorrect loop operation could occur. In addition, care must be taken in interrupt service routines as the overlay registers are not automatically saved and restored on the processor mode stack.

For ADSP-2100 Family compatibility, MMAP = 1 is allowed. In this mode, booting is disabled and overlay memory is disabled (*PMOVLAY* must be 0). Figure 5 shows the memory map in this configuration.

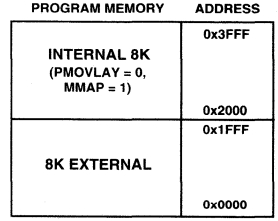


Figure 5. Program Memory (MMAP = 1)

Data Memory

The ADSP-2181 has 16,352 16-bit words of internal data memory. In addition, the ADSP-2181 allows the use of 8K external memory overlays. The following diagram shows the organization of the data memory.

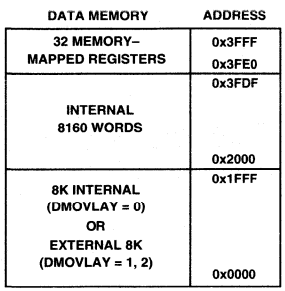


Figure 6. Data Memory

There are 16,352 words of memory accessible internally when the DMOVLAY register is set to 0. When DMOVLAY is set to something other than 0, external accesses occur at addresses 0x0000 through 0x1FFF. The external address is generated as shown in Table III.

Table III.

DMOVLAY	Memory	A13	A12:0
0	Internal	Not Applicable	Not Applicable
1	External Overlay 1	0	13 LSBs of Address Between 0x0000 and 0x1FFF
2	External Overlay 2	1	13 LSBs of Address Between 0x0000 and 0x1FFF

This organization allows for two external 8K overlays using only the normal 14 address bits.

All internal accesses complete in one cycle. Accesses to external memory are timed using the wait states specified by the DWAIT register.

I/O Space

The ADSP-2181 supports an additional external memory space called I/O space. This space is designed to support simple connections to peripherals or to bus interface ASIC data registers. I/O space supports 2048 locations. The lower eleven bits of the external address bus are used; the upper three bits are undefined. Two instructions were added to the core ADSP-2100 Family instruction set to read from and write to I/O memory space. The I/O space also has four dedicated three-bit wait state registers, IOWAIT0-3, which specify up to seven wait states to be automatically generated for each of four regions. The wait states act on address ranges as shown in Table IV.

Composite Memory Select ($\overline{\text{CMS}}$)

The ADSP-2181 has a programmable memory select signal that is useful for generating memory select signals for memories mapped to more than one space. The $\overline{\text{CMS}}$ signal is generated to have the same timing as each of the individual memory select signals ($\overline{\text{PMS}}$, $\overline{\text{DMS}}$, $\overline{\text{BMS}}$, $\overline{\text{IOMS}}$) but can combine their functionality.

Table IV.

Address Range	Wait State Register
0x000–0x1FF	IOWAIT0
0x200–0x3FF	IOWAIT1
0x400–0x5FF	IOWAIT2
0x600–0x7FF	IOWAIT3

Each bit in the CMSSEL register, when set, causes the $\overline{\text{CMS}}$ signal to be asserted when the selected memory select is asserted. For example, to use a 32K word memory to act as both program and data memory, set the $\overline{\text{PMS}}$ and $\overline{\text{DMS}}$ bits in the CMSSEL register and use the $\overline{\text{CMS}}$ pin to drive the chip select of the memory, and use either $\overline{\text{DMS}}$ or $\overline{\text{PMS}}$ as the additional address bit.

The $\overline{\text{CMS}}$ pin functions like the other memory select signals with the same timing and bus request logic. A 1 in the enable bit causes the assertion of the $\overline{\text{CMS}}$ signal at the same time as the selected memory select signal. All four enable bits default to 1 at reset.

Byte Memory

The byte memory space is a bidirectional, 8-bit-wide, external memory space used to store programs and data. Byte memory is accessed using the BDMA feature. The byte memory space consists of 256 pages, each of which is 16K × 8.

The byte memory space on the ADSP-2181 supports read and write operations as well as four different data formats. The byte memory uses data bits 15:8 for data. The byte memory uses data bits 23:16 and address bits 13:0 to create a 22-bit address. This allows up to a 4 meg × 8 (32 megabit) ROM or RAM to be used without glue logic. All byte memory accesses are timed by the BMWAIT register.

Byte Memory DMA (BDMA)

The Byte memory DMA controller allows loading and storing of program instructions and data using the byte memory space. The BDMA circuit is able to access the byte memory space while the processor is operating normally and steals only one DSP cycle per 8-, 16- or 24-bit word transferred.

The BDMA circuit supports four different data formats which are selected by the BTYPE register field. The appropriate number of 8-bit accesses are done from the byte memory space to build the word size selected. Table V shows the data formats supported by the BDMA circuit.

Table V.

BTYPE	Internal Memory Space	Word Size	Alignment
00	Program Memory	24	Full Word
01	Data Memory	16	Full Word
10	Data Memory	8	MSBs
11	Data Memory	8	LSBs

Unused bits in the 8-bit data memory formats are filled with 0s. The BIAD register field is used to specify the starting address for the on-chip memory involved with the transfer. The 14-bit BEAD register specifies the starting address for the external byte

memory space. The 8-bit BMPAGE register specifies the starting page for the external byte memory space. The BDIR register field selects the direction of the transfer. Finally the 14-bit BWCOUNT register specifies the number of DSP words to transfer and initiates the BDMA circuit transfers.

BDMA accesses can cross page boundaries during sequential addressing. A BDMA interrupt is generated on the completion of the number of transfers specified by the BWCOUNT register. The BWCOUNT register is updated after each transfer so it can be used to check the status of the transfers. When it reaches zero, the transfers have finished and a BDMA interrupt is generated. The BMPAGE and BEAD registers must not be accessed by the DSP during BDMA operations.

The source or destination of a BDMA transfer will always be on-chip program or data memory, regardless of the values of MMAP, PMOVLAY or DMOVLAY.

When the BWCOUNT register is written with a nonzero value the BDMA circuit starts executing byte memory accesses with wait states set by BMWAIT. These accesses continue until the count reaches zero. When enough accesses have occurred to create a destination word, it is transferred to or from on-chip memory. The transfer takes one DSP cycle. DSP accesses to external memory have priority over BDMA byte memory accesses.

The BDMA Context Reset bit (BCR) controls whether the processor is held off while the BDMA accesses are occurring. Setting the BCR bit to 0 allows the processor to continue operations. Setting the BCR bit to 1 causes the processor to stop execution while the BDMA accesses are occurring, to clear the context of the processor, and start execution at address 0 when the BDMA accesses have completed.

Internal Memory DMA Port (IDMA Port)

The IDMA Port provides an efficient means of communication between a host system and the ADSP-2181. The port is used to access the on-chip program memory and data memory of the DSP with only one DSP cycle per word overhead.

The IDMA port has a 16-bit multiplexed address and data bus and supports 24-bit program memory. The IDMA port is completely asynchronous and can be written to while the ADSP-2181 is operating at full speed.

The DSP memory address is latched and then is automatically incremented after each IDMA transaction. An external device can therefore access a block of sequentially addressed memory by specifying only the starting address of the block. This increases throughput as the address does not have to be sent for each memory access.

IDMA Port access occurs in two phases. The first is the IDMA Address Latch cycle. When the acknowledge is asserted, a 14-bit address and 1-bit destination type can be driven onto the bus by an external device. The address specifies an on-chip memory location, the destination type specifies whether it is a DM or PM access. The falling edge of the address latch signal latches this value into the IDMAA register.

Once the address is stored, data can then be either read from, or written to, the ADSP-2181's on-chip memory. Asserting the select line ($\overline{IS}$) and the appropriate read or write line ($\overline{IRD}$ and $\overline{IWR}$ respectively) signals the ADSP-2181 that a particular transaction is required. In either case, there is a one-processor-cycle delay for synchronization. The memory access consumes one additional processor cycle.

Once an access has occurred, the latched address is automatically incremented, and another access can occur.

Through the IDMAA register, the DSP can also specify the starting address and data format for DMA operation.

Bootstrap Loading (Booting)

The ADSP-2181 has two mechanisms to allow automatic loading of the on-chip program memory after reset. The method for booting after reset is controlled by the MMAP and BMODE pins as shown in Table VI.

2

BDMA Booting

When the BMODE and MMAP pins specify BDMA booting (MMAP = 0, BMODE = 0), the ADSP-2181 initiates a BDMA boot sequence when reset is released. The BDMA interface is set up during reset to the following defaults when BDMA booting is specified: the BDIR, BMPAGE, BIAD, and BEAD registers are set to 0, the BTYPE register is set to 0 to specify program memory 24 bit words, and the BWCOUNT register is set to 32. This causes 32 words of on-chip program memory to be loaded from byte memory. These 32 words are used to set up the BDMA to load in the remaining program code. The BCR bit is also set to 1, which causes program execution to be held off until all 32 words are loaded into on-chip program memory. Execution then begins at address 0.

Table VI. Boot Summary Table

MMAP	BMODE	Booting Method
0	0	BDMA feature is used in default mode to load the first 32 program memory words from the byte memory space. Program execution is held off until all 32 words have been loaded.
0	1	IDMA feature is used to load any internal memory as desired. Program execution is held off until internal program memory location 0 is written to.
1	X	Bootstrap features disabled. Program execution immediately starts from location 0.

The ADSP-2100 Family development software (Revision 5.02 and later) fully supports the BDMA booting feature and can generate byte memory space compatible boot code.

The IDLE instruction can also be used to allow the processor to hold off execution while booting continues through the BDMA interface.

IDMA Port Booting

The ADSP-2181 can also boot programs through its Internal DMA port. If BMODE = 1 and MMAP = 0, the ADSP-2181 boots from the IDMA port. IDMA feature can load as much on-chip memory as desired. Program execution is held off until on-chip program memory location 0 is written to.

The ADSP-2100 Family development software (Revision 5.02 and later) can generate IDMA compatible boot code.

Bus Request & Bus Grant

The ADSP-2181 can relinquish control of the data and address buses to an external device. When the external device requires access to memory, it asserts the bus request ($\overline{BR}$) signal. If the ADSP-2181 is not performing an external memory access, then it responds to the active $\overline{BR}$ input in the following processor cycle by:

- three-stating the data and address buses and the $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{RD}$, $\overline{WR}$ output drivers,
- asserting the bus grant ($\overline{BG}$) signal, and
- halting program execution.

If Go Mode is enabled, the ADSP-2181 will not halt program execution until it encounters an instruction that requires an external memory access.

If the ADSP-2181 is performing an external memory access when the external device asserts the $\overline{BR}$ signal, then it will not three-state the memory interfaces or assert the $\overline{BG}$ signal until the processor cycle after the access completes. The instruction does not need to be completed when the bus is granted. If a single instruction requires two external memory accesses, the bus will be granted between the two accesses.

When the $\overline{BR}$ signal is released, the processor releases the $\overline{BG}$ signal, reenables the output drivers and continues program execution from the point where it stopped.

The bus request feature operates at all times, including when the processor is booting and when $\overline{RESET}$ is active.

The $\overline{BGH}$ pin is asserted when the ADSP-2181 is ready to execute an instruction but is stopped because the external bus is already granted to another device. The other device can release the bus by deasserting bus request. Once the bus is released, the ADSP-2181 deasserts $\overline{BG}$ and $\overline{BGH}$ and executes the external memory access.

Flag I/O Pins

The ADSP-2181 has eight general purpose programmable input/output flag pins. They are controlled by two memory mapped registers. The PFTYPE register determines the direction, 1 = output and 0 = input. The PFDATA register is used to read and write the values on the pins. Data being read from a pin configured as an input is synchronized to the ADSP-2181's clock. Bits that are programmed as outputs will read the value being output. The PF pins default to input during reset.

In addition to the programmable flags, the ADSP-2181 has five fixed-mode flags, FLAG_IN, FLAG_OUT, FL0, FL1, and FL2. FL0-FL2 are dedicated output flags. FLAG_IN and FLAG_OUT are available as an alternate configuration of SPORT1.

ADSP-2181 REGISTERS

Figure 7 summarizes all the registers in the ADSP-2181. Some registers store values. For example, AX0 stores an ALU operand; I4 stores a DAG2 pointer. Other registers consist of control bits and fields, or status flags. For example, ASTAT contains status flags from arithmetic operations, and fields in DWAIT control the numbers of wait states for different zones of data memory.

A secondary set of data registers in all computational units allows a single-cycle context switch.

The PMOVLAY and DMOVLAY registers control the overlay space for program and data memory. These registers can be used in certain data move instructions. For example:

```
PMOVLAY = 2;
DMOVLAY = AX0;
```

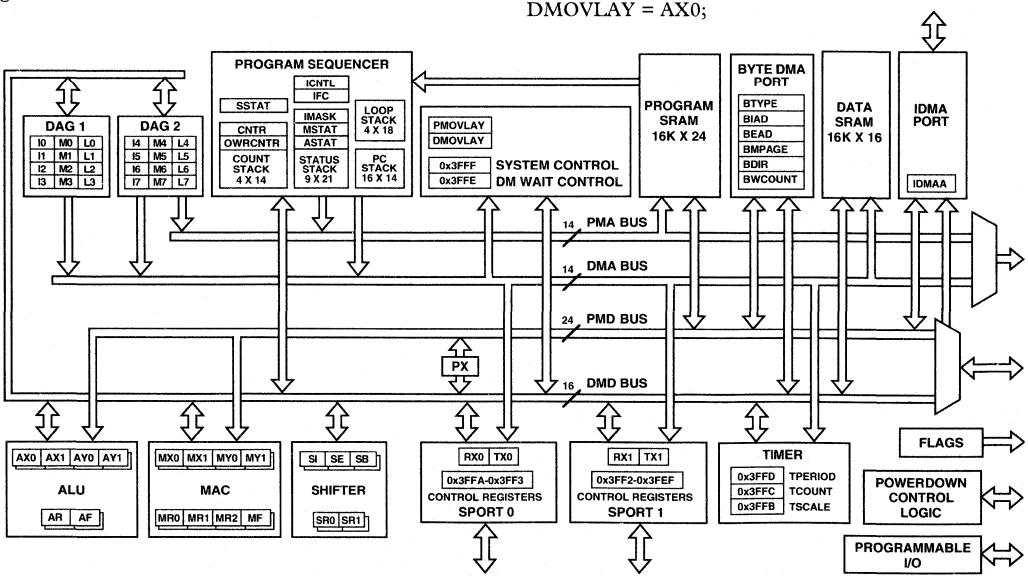
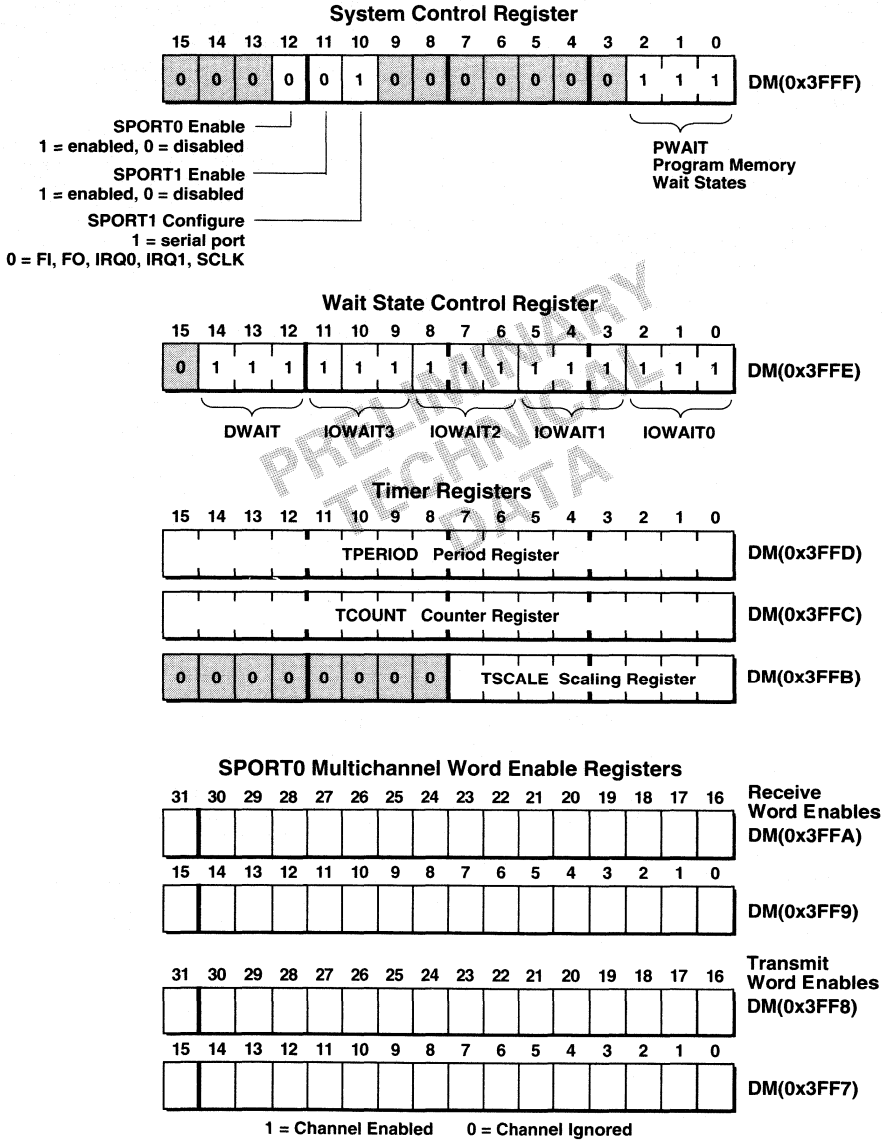



Figure 7. ADSP-2181 Registers

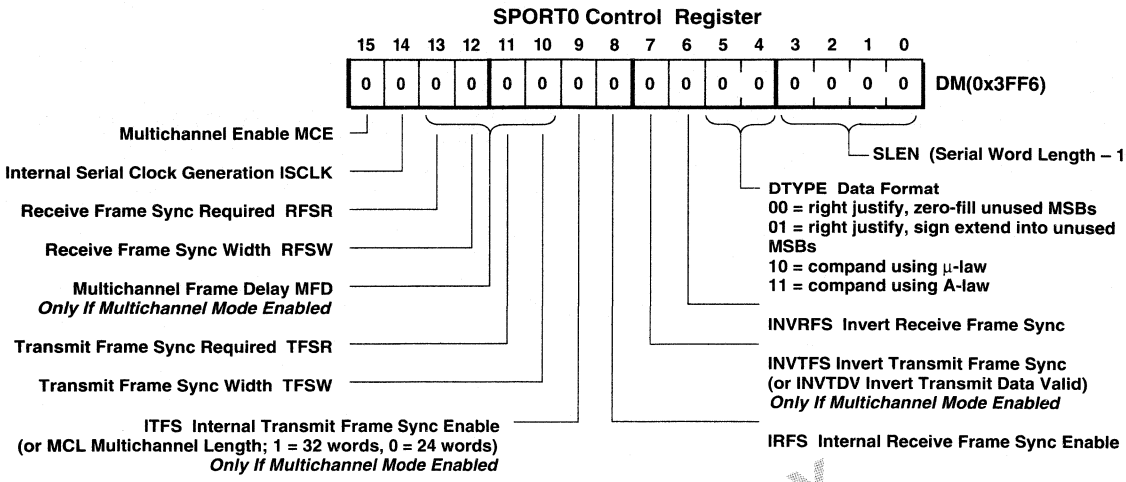
SI = DMOVLAY;
PMOVLAY=DM(0x1234);
DM(0x1234)=DMOVLAY;

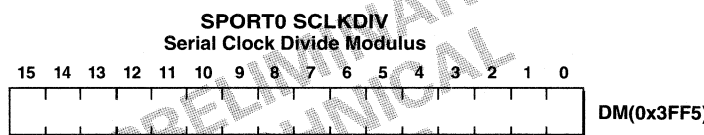
The bit and field definitions for control and status registers are given in the rest of this section. The system control register, DWAIT register, timer registers, IDMA port control registers, IDMA port data registers, and SPORT control registers are all mapped into data memory; that is, registers are accessed by reading and writing data memory locations rather than register names. The particular data memory address is shown with each memory-mapped register.

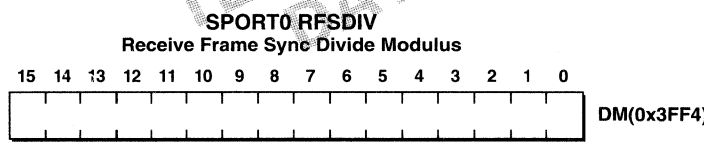
Register bit values shown on the following pages are the default bit values after reset. If no values are shown, the bits are indeterminate at reset. Reserved bits are shown in gray; these bits should always be written with zeros.

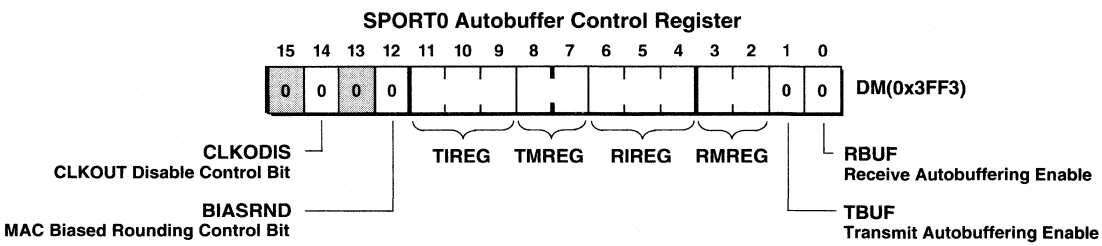


Memory-Mapped Registers



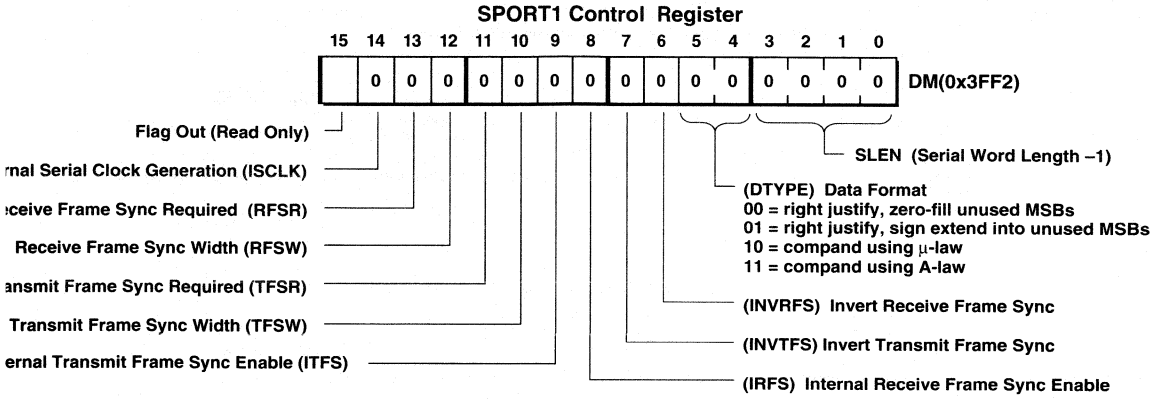


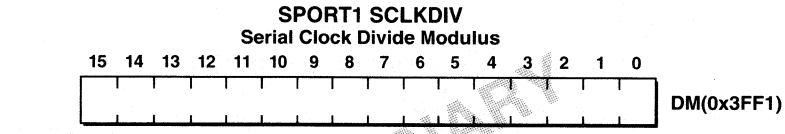


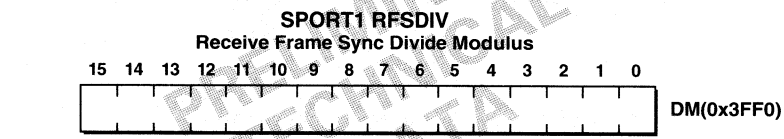


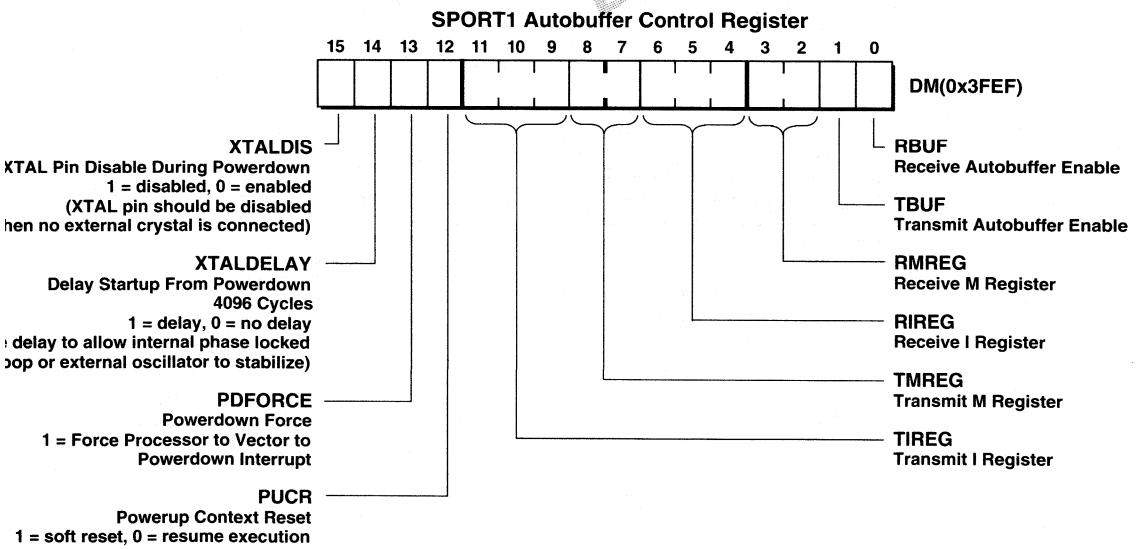
Memory-Mapped Registers

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.









Memory-Mapped Registers

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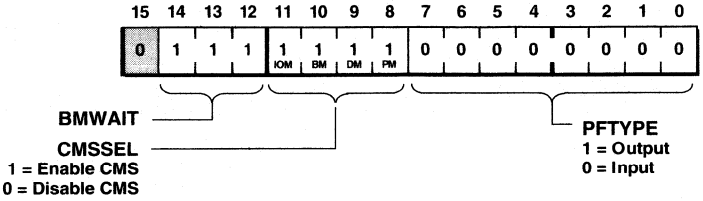
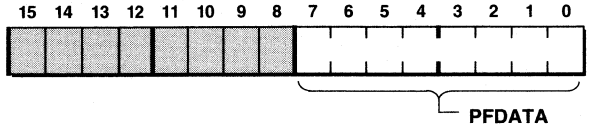
Programmable Flag And Composite Select Control

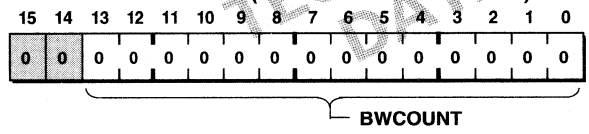


Programmable Flag Data

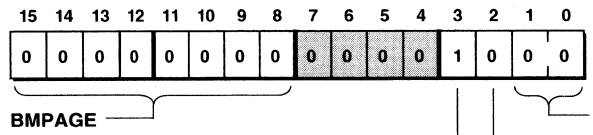


BDMA Word Count (MMAP = 0 AND BMODE = 0)

BDMA Word Count (MMAP = 1 OR BMODE = 1)

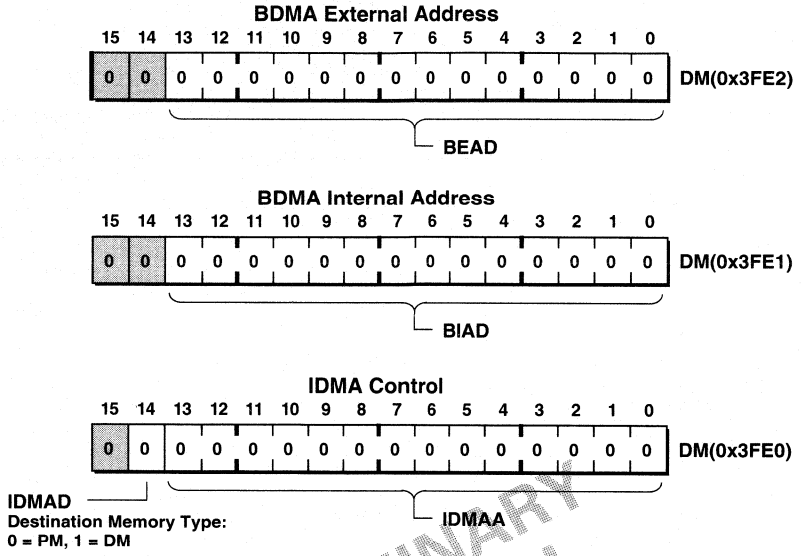


BDMA Control

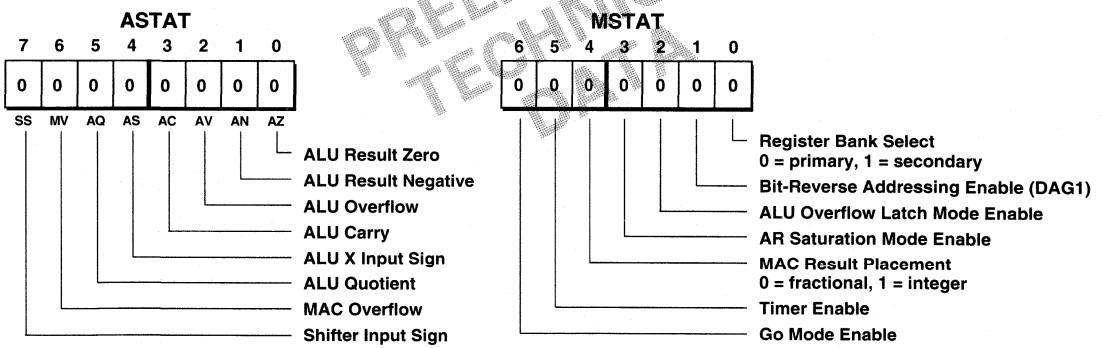


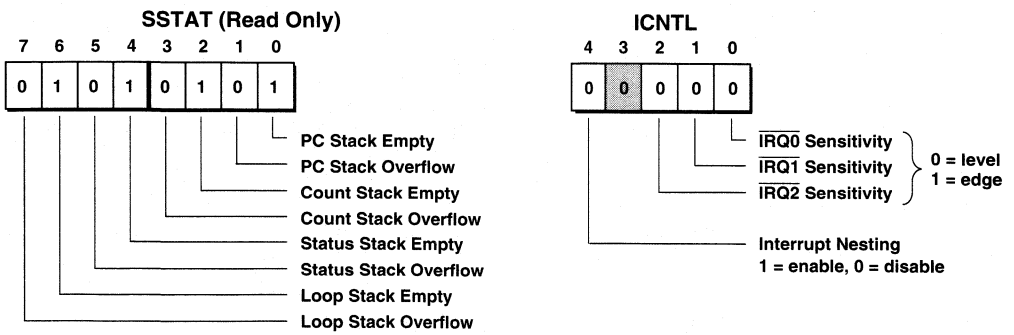
BTYPE	00	01	10	11
Internal Memory Space	PM	DM	DM	DM
Word Size	24	16	8	8
Alignment	Full Word	Full Word	MSB	LSB

Memory-Mapped Registers



Memory-Mapped Registers





Non-Memory-Mapped Registers

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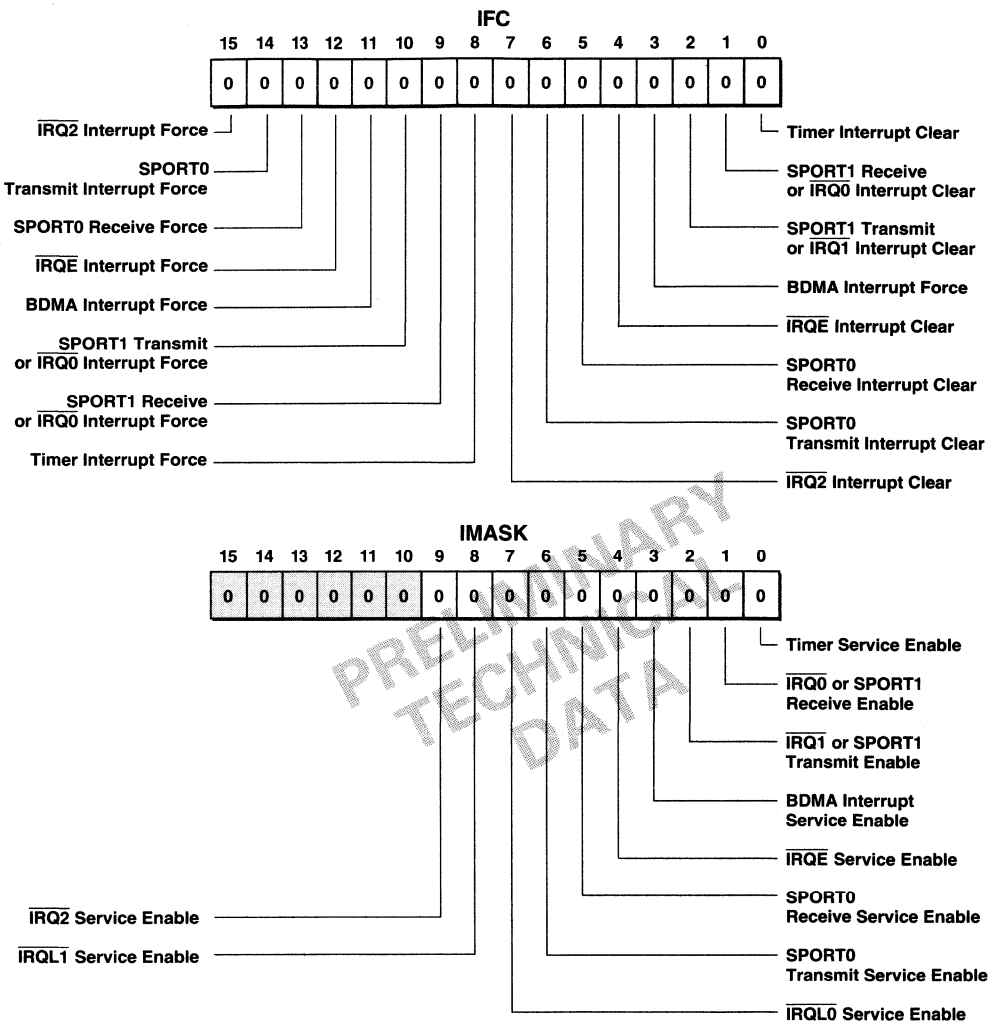


Non-Memory-Mapped Registers

INSTRUCTION SET DESCRIPTION

The ADSP-2181 assembly language instruction set has an algebraic syntax that was designed for ease of coding and readability. The assembly language, which takes full advantage of the processor's unique architecture, offers the following benefits:

- The algebraic syntax eliminates the need to remember cryptic assembler mnemonics. For example, a typical arithmetic add instruction, such as AR = AX0 + AY0, resembles a simple equation.
- Every instruction assembles into a single, 24-bit word that can execute in a single instruction cycle.
- The syntax is a superset ADSP-2100 Family assembly language and is completely source and object code compatible with other family members. Programs may need to be relocated to utilize on-chip memory and conform to the ADSP-2181's interrupt vector and reset vector map.
- Sixteen condition codes are available. For conditional jump, call, return, or arithmetic instructions, the condition can be checked and the operation executed in the same instruction cycle.
- Multifunction instructions allow parallel execution of an arithmetic instruction with up to two fetches or one write to processor memory space during a single instruction cycle.

The ADSP-2181 supports the ADSP-2100 Family instruction set. This section only includes detailed descriptions of the instructions that are unique to the ADSP-2171 and ADSP-2181. Consult the *ADSP-2100 Family User's Manual* for a complete description of the syntax and an instruction set reference.

New Instructions & Operations

This section discusses the new instructions and operations available on the ADSP-2181. Syntax, examples and detailed descriptions of each instruction follow.

New I/O Space Instructions

The instructions used to access I/O space are as shown:

Syntax: IO(*addr*) = *dreg*
dreg = IO(*addr*);

where *addr* is an address value between 0 and 2048 and *dreg* is any of the 16 data registers.

Examples: IO(23) = AR0;
AR1 = IO(17);

Description: The I/O space read and write instructions move data between the data registers and the I/O memory space.

Slow IDLE

The IDLE instruction on the ADSP-2181 supports a "slow idle" feature. Slow IDLE allows slowing the clock down by a factor of 16, 32, 64, or 128 during IDLE. The instruction source code is specified as follows:

Syntax: IDLE (n);

Permissible n Values
16, 32, 64, 128

Examples: IDLE;

IDLE (16);

Description: The IDLE instruction causes the processor to wait indefinitely in a low power state until an interrupt occurs. When an unmasked interrupt occurs, it is serviced; execution then continues with the instruction following the IDLE instruction. The optional value provides a "slow idle" feature; slowing the clock down by the factor set with the value.

ALU xop Operations

ALU operations support constants in addition to *yop*s. These constants are available for all nonmultifunction ALU operations using both X and Y operands except *DIVS*. The instruction source code is specified as follows:

Syntax: [IF condition] | AR / AF | = xop function | yop value |

Permissible xops
AX0, AX1, AR, MR0, MR1, MR2, SR0, SR1

Permissible Functions
ADD/ADD with CARRY, SUBTRACT X–Y/SUBTRACT X–Y with BORROW, SUBTRACT Y–X/SUBTRACT Y–X with BORROW, AND, OR, XOR

Permissible yops and values
AY0, AY1, AF, 0, 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32767, –2, –3, –5, –9, –17, –33, –65, –129, –257, –513, –1025, –2049, –4097, –8193, –16385, –32768

Permissible Conditions
EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Examples: AR = AR +1;
AR = MR1 – 33;
IF GT AF = AX1 OR 16;

Description: Test the optional condition and, if true, perform the specified function. If false then perform a no-operation. Omitting the condition performs the function unconditionally. The operands are contained in the data registers specified in the instruction or optionally a value may be used.

ALU Bit Operations

The new ALU *xop* operations instructions allow you to code bit test, set, clear, and toggle operations through careful choice of the constant and ALU function. For streamlined programming, the source code for these operations can also be specified as:

Syntax: [IF condition] | AR / AF | = | TSTBIT n of xop; / SETBIT n of xop; / CLBIT n of xop; / TGBIT n of xop; |

Permissible xops
AX0, AX1, AR, MR0, MR1, MR2, SR0, SR1

Permissible Conditions
EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Permissible n Values (0 = LSB)
0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15

Examples: AF=TSTBIT 5 of AR;
IF NE JUMP SET;
/* JUMP TO SET IF BIT IS SET */

Definitions of Operations
Testbit is an AND operation with a 1 in the selected bit
Setbit is an OR operation with a 1 in the selected bit
CLRbit is an AND operation with a 0 in the selected bit
TGLbit is an XOR operation with a 1 in the selected bit

ALU PASS Operations

The ALU PASS operation on the ADSP-2181 supports a new list of constants in addition to yops. The instruction source code is specified as follows:

Syntax: [IF condition] | AR / AF | = pass | yop value |

Permissible yops and values
AY0, AY1, AF, 0, 1, 2, 3, 4, 5, 7, 8, 9, 15, 16, 17, 31, 32, 33, 63, 64, 65, 127, 128, 129, 255, 256, 257, 511, 512, 513, 1023, 1024, 1025, 2047, 2048, 2049, 4095, 4096, 4097, 8191, 8192, 8193, 16383, 16384, 16385, 32766, 32767, –1, –2, –3, –4, –5, –6, –8, –9, –10, –16, –17, –18, –32, –33, –34, –64, –65, –66, –128, –129, –130, –256, –257, –258, –512, –513, –514, –1024, –1025, –1026, –2048, –2049, –2050, –4096, –4097, –4098, –8192, –8193, –8194, –16384, –16385, –16386, –32767, –32768

Permissible Conditions

EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Example: IF GE AR = PASS AY0;
IF EQ AF = PASS –1025;

Description: Test the optional condition and, if true, pass the source operand unmodified through the ALU block and store in the destination location. If the condition is not true, perform a no-operation. Omitting the condition performs the *pass* unconditionally. The source operand is contained in the data registers specified in the instruction or optional value.

The PASS instruction performs the transfer to the AR register and affects the status flag; this instruction is different from a register move operation which does not affect any status flags. PASS 0 is one method of clearing AR. PASS 0 can also be combined in a multifunction instruction in conjunction with memory reads and writes to clear AR.

Note: The ALU status flags (in the ASTAT register) are not defined for the execution of this instruction when using the constant values other than 0, 1, and –1.

Result Free ALU Operation

The result free ALU operations on the ADSP-2181 support the generation of condition codes based on an ALU operation but discard the result. The source code for the new instruction is specified as follows:

Syntax: NONE = <ALU>;

where <ALU> is any unconditional ALU operation except DIVS or DIVQ.

Example: NONE = AX0 – AY0;
NONE = PASS SR0;

Description: Perform the designated ALU operation, set the condition codes, then discard the result value. This allows the testing of register values without disturbing the AR or AF register values.

MAC Operations

The ADSP-2181 has a modified MAC which allows additional "type 9" instructions. The conditional ALU/MAC instruction has been modified to allow the X operand to be used as the Y operand as well. This allows a single cycle X^2, and also $\sum X^2$ operations.

The new MAC instructions allow the use of any *xop* as both the X and Y operands. The instructions source code is specified as follows:

Syntax: [IF condition] | MR / MF | = | [MR +] / [MR –] | xop * | yop / xop | | (UU); / (SS); / (RND);

Permissible xops

AR, MR0, MR1, MR2, MX0, MX1, SR0, SR1

Permissible Conditions

EQ, NE, GT, GE, LT, LE, NEG, POS, AV, NOT AV, AC, NOT AC, MV, NOT MV, NOT CE

Example: IF LT MR=MR+ SR0*SR0 (SS);

Note: Both X operators must be the same register.

Biased Rounding

A new mode has been added to allow biased rounding in addition to the normal unbiased rounding. When the BIASRND bit is set to 0, the normal unbiased rounding operations occur. When the BIASRND bit is set to 1, biased rounding occurs instead of the normal unbiased rounding. When operating in biased rounding mode all rounding operations with MR0 set to 0x8000 will round up, rather than only rounding odd MR1 values up. For example:

MR value before RND	biased RND result	unbiased RND result
00-0000-8000	00-0001-8000	00-0000-8000
00-0001-8000	00-0002-8000	00-0002-8000
00-0000-8001	00-0001-8001	00-0001-8001
00-0001-8001	00-0002-8001	00-0002-8001
00-0000-7FFF	00-0000-7FFF	00-0000-7FFF
00-0001-7FFF	00-0001-7FFF	00-0001-7FFF

This mode only has an effect when the MR0 register contains 0x8000, all other rounding operation work normally. This mode was added to allow more efficient implementation of bit specified algorithms which specify biased rounding such as the GSM speech compression routines. Unbiased rounding is preferred for most algorithms.

Note: BIASRND bit is Bit 12 of the SPORT0 Autobuffer Control register.

Interrupt Enable

The ADSP-2181 supports an interrupt enable instruction. Interrupts are enabled by default at reset. The instruction source code is specified as follows:

Syntax: ENA INTS;

Description: Executing the ENA INTS instruction allows all unmasked interrupts to be serviced again.

Interrupt Disable

The ADSP-2181 supports an interrupt disable instruction.The instruction source code is specified as follows:

Syntax: DIS INTS;

Description: Reset enables interrupt servicing. Executing the DIS INTS instruction causes all interrupts to be masked without changing the contents of the IMASK register. Disabling interrupts does not affect the autobuffer circuitry, which will operate normally whether or not interrupts are enabled. The disable interrupt instruction masks all user interrupts including the power-down interrupt.

Example Code

The following example is a code fragment that performs the filter tap update for an adaptive (least-mean-squared algorithm) filter. Notice that the computations in the instructions are written like algebraic equations.

```
  MF=MX0*MY1 (RND), MX0=DM (I2,M1);   /* MF=error*beta */
  MR=MX0*MF (RND), AY0=PM (I6,MS);
DO adapt UNTIL CE;
  AR=MR1 + AY0, MX0=DM (I2,M1), AY0=PM (I6,M7);
adapt:  PM(I6,M6) =AR, MR=MX0*MF (RND);
        MODIFY (I2, M3);            /* Point to oldest data */
        MODIFY (I6, M7);            /* Point to start of data */
```

ADSP-2181–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}	Supply Voltage	4.5	5.5	4.5	5.5	V
T_{AMB}	Ambient Operating Temperature	0	+70	–40	+85	°C

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	K/B Grades Min	K/B Grades Max	Unit
V_{IH}	Hi-Level Input Voltage[1, 2]	@ V_{DD} = max	2.0		V
V_{IH}	Hi-Level CLKIN Voltage	@ V_{DD} = max	2.2		V
V_{IL}	Lo-Level Input Voltage[1, 3]	@ V_{DD} = min		0.8	V
V_{OH}	Hi-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OH} = –0.5 mA	2.4		V
		@ V_{DD} = min, I_{OH} = –100 µA[6]	V_{DD} – 0.3		V
V_{OL}	Lo-Level Output Voltage[1, 4, 5]	@ V_{DD} = min, I_{OL} = 2 mA		0.4	V
I_{IH}	Hi-Level Input Current[3]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Lo-Level Input Current[3]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZH}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max[8]		10	µA
I_{OZL}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = 0 V[8]		10	µA
I_{DD}	Supply Current (Idle)[9, 10]	@ V_{DD} = max		TBD	mA
I_{DD}	Supply Current (Dynamic)[10]	@ V_{DD} = max, t_{CK} = 30 ns[11]		TBD	mA
I_{DD}	Supply Current (Power Down)[10]	Lowest Power Mode[12]		100	µA
C_I	Input Pin Capacitance[3, 6, 13]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C		8	pF
C_O	Output Pin Capacitance[6, 7, 13, 14]	@ V_{IN} = 2.5 V, f_{IN} = 1.0 MHz, T_{AMB} = +25°C		8	pF

NOTES
TBD = To be determined.
[1]Bidirectional pins: D0-D23, RFS0, RFS1, SCLK0, SCLK1, TFS0, TFS1, HD0-HD15/HAD0-HAD15.
[2]Input only pins: RESET, IRQ2, BR, MMAP, DR0, DR1, HSEL, HSIZE, BMODE, HMD0, HMD1, HRD/HWR, HWR/HDS, PWD, HA2/ALE, HA1-0.
[3]Input only pins: CLKIN, RESET, IRQ2, BR, MMAP, DR0, DR1, IS, IAL, IRD, IWR, IRQL0, IRQL1, IRQE, PWD.
[4]Output pins: BG, PMS, DMS, BMS, IOMS, CMS, RD, WR, IACK, PWDACK, A0-A13, DT0, DT1, CLKOUT, FL2-0.
[5]Although specified for TTL outputs, all ADSP-2181 outputs are CMOS-compatible and will drive to V_{DD} and GND, assuming no dc loads.
[6]Guaranteed but not tested.
[7]Three-statable pins: A0-A13, D0-D23, PMS, DMS, BMS, IOMS, CMS, RD, WR, DT0, DT1, SCLK0, SCLK1, TFS0, TFS1, RFS0, RSF1.
[8]0 V on BR, CLKIN Active (to force three-state condition).
[9]Idle refers to ADSP-2181 state of operation during execution of IDLE instruction. Deasserted pins are driven to either V_{DD} or GND.
[10]Current reflects device operating with no output loads.
[11]V_{IN} = 0.4 V and 2.4 V. For typical figures for supply currents, refer to "Power Dissipation" section.
[12]See Chapter 9, of the *ADSP-2100 Family User's Manual* for details.
[13]Applies to TQFP and PQFP package types.
[14]Output pin capacitance is the capacitive load for any three-state output pin.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) TQFP . . . . . +280°C
Lead Temperature (5 sec) PQFP . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-2181 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2181 features proprietary ESD protection circuitry to dissipate high energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-2171 has been classified as a Class 1 device.

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

TIMING PARAMETERS

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add up parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing; it is dependent on the internal design. Timing requirements apply to signals that are controlled outside the processor, such as the data input for a read operation.

Timing requirements guarantee that the processor operates correctly with another device. Switching characteristics tell you what the device will do under a given circumstance. Also, use the switching characteristics to ensure any timing requirement of a device connected to the processor (such as memory) is satisfied.

MEMORY REQUIREMENTS

This chart links common memory device specification names and ADSP-2181 timing parameters for your convenience.

Parameter Name	Function	Common Memory Device Specification Name
t_{ASW}	A0–A13, Setup before $\overline{WR}$ Low	Address Setup to Write Start
t_{AW}	A0–A13, Setup before $\overline{WR}$ Deasserted	Address Setup to Write End
t_{WRA}	A0–A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	Address Hold Time
t_{DW}	Data Setup before $\overline{WR}$ High	Data Setup Time
t_{DH}	Data Hold after $\overline{WR}$ High	Data Hold Time
t_{RDD}	$\overline{RD}$ Low to Data Valid	$\overline{OE}$ to Data Valid
t_{AA}	A0–A13, $\overline{xMS}$ to Data Valid	Address Access Time

$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$, $\overline{CMS}$, $\overline{IOMS}$

Parameter		Min	Max	Unit
Clock Signals				
t_{CK} is defined as 0.5 t_{CKI}. The ADSP-2181 uses an input clock with a frequency equal to half the instruction rate; a 16.67 MHz input clock (which is equivalent to 60 ns) yields a 30 ns processor cycle (equivalent to 33 MHz). t_{CK} values within the range of 0.5 t_{CKI} period should be substituted for all relevant timing parameters to obtain specification value.				
Example: $t_{CKH} = 0.5t_{CK} - 7$ ns = 0.5 (30 ns) – 7 ns = 8 ns.				
Timing Requirement:				
t_{CKI}	CLKIN Period	60	150	ns
t_{CKIL}	CLKIN Width Low	20		ns
t_{CKIH}	CLKIN Width High	20		ns
Switching Characteristic:				
t_{CKL}	CLKOUT Width Low	$0.5t_{CK} - 7$		ns
t_{CKH}	CLKOUT Width High	$0.5t_{CK} - 7$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20	ns
Control Signals				
Timing Requirement:				
t_{RSP}	RESET Width Low	$5t_{CK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator start-up time).

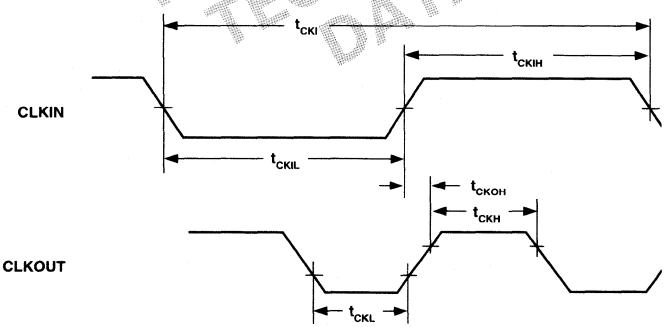


Figure 8. Clock Signals

Parameter		Min	Max	Unit
Interrupts and Flag				
Timing Requirement:				
t_{IFS}	$\overline{IRQx}$, FI, or PFx Setup before CLKOUT Low [1, 2, 3, 4]	$0.25t_{CK} + 15$		ns
t_{IFH}	$\overline{IRQx}$, FI, or PFx Hold after CLKOUT High [1, 2, 3, 4]	$0.25t_{CK}$		ns
Switching Characteristics:				
t_{FOH}	Flag Output Hold after CLKOUT Low[5]	$0.25t_{CK} - 7$		ns
t_{FOD}	Flag Output Delay from CLKOUT Low[5]	$0.25t_{CK} + 5$		ns

NOTES
[1]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise the signals will be recognized on the following cycle. (Refer to "Interrupt Controller Operation" in the Program Control chapter of the User's Manual for further information on interrupt servicing.)
[2]Edge-sensitive interrupts require pulse widths greater than 10 ns; level-sensitive interrupts must be held low until serviced.
[3]$\overline{IRQx}$ = $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$, $\overline{IRQL0}$, $\overline{IRQL1}$, $\overline{IRQE}$
[4]PFx = PF0, PF1, PF2, PF3, PF4, PF5, PF6, PF7
[5]Flag outputs = PFx, FL0, FL1, FL2, Flag_out[4]

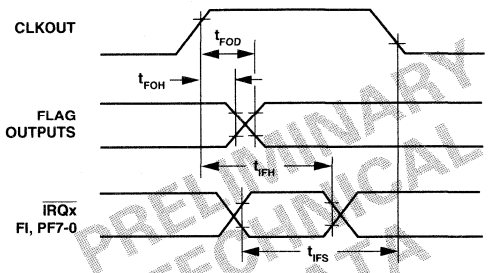


Figure 9. Interrupts and Flags

Parameter		Min	Max	Unit
Bus Request/Grant				
Timing Requirement:				
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	$0.25t_{CK} + 2$		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	$0.25t_{CK} + 17$		ns
Switching Characteristic:				
t_{SD}	CLKOUT High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable		$0.25t_{CK} + 10$	ns
t_{SDB}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0		ns
t_{SE}	$\overline{BG}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0		ns
t_{SEC}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	$0.25t_{CK} - 7$		ns
t_{SDBH}	$\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BGH}$ Low[2]	0		ns
t_{SEH}	$\overline{BGH}$ High to $\overline{xMS}$, $\overline{RD}$, $\overline{WR}$ Enable[2]	0		ns

NOTES
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$
[1]$\overline{BR}$ is an asynchronous signal. If $\overline{BR}$ meets the setup/hold requirements, it will be recognized during the current clock cycle; otherwise the signal will be recognized on the following cycle. Refer to the *ADSP-2100 Family User's Manual* for $\overline{BR}$/$\overline{BG}$ cycle relationships.
[2]$\overline{BGH}$ is asserted when the bus is granted and the processor requires control of the bus to continue.

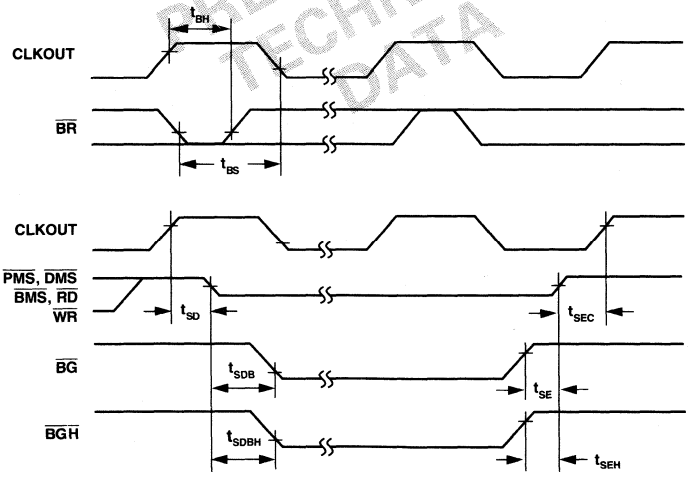


Figure 10. Bus Request–Bus Grant

Parameter		Min	Max	Unit
Memory Read				
Timing Requirement:				
t_{RDD}	$\overline{RD}$ Low to Data Valid		$0.5t_{CK} - 9 + w$	ns
t_{AA}	A0-A13, $\overline{xMS}$ to Data Valid		$0.75t_{CK} - 10.5 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0		ns
Switching Characteristic:				
t_{RP}	$\overline{RD}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	$0.25t_{CK} - 5$	$0.25t_{CK} + 7$	ns
t_{ASR}	A0-A13, $\overline{xMS}$ Setup before $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{RDA}	A0-A13, $\overline{xMS}$ Hold after $\overline{RD}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$

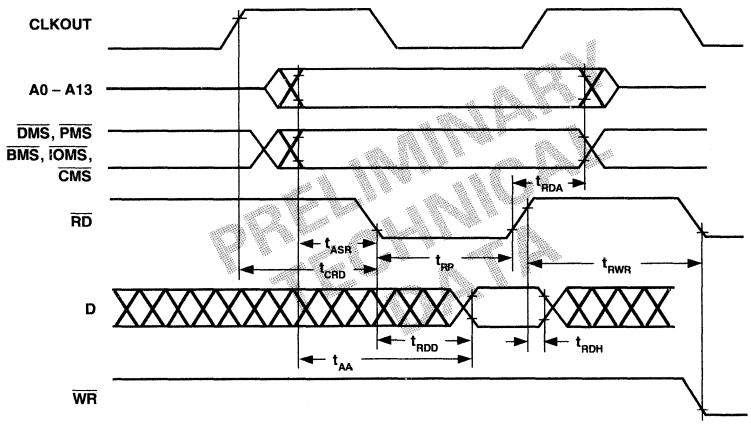


Figure 11. Memory Read

Parameter		Min	Max	Unit
Memory Write				
Switching Characteristic:				
t_{DW}	Data Setup before $\overline{WR}$ High	$0.5t_{CK} - 7 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	$0.25t_{CK} - 2$		ns
t_{WP}	$\overline{WR}$ Pulse Width	$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0		ns
t_{ASW}	A0-A13, $\overline{xMS}$ Setup before $\overline{WR}$ Low	$0.25t_{CK} - 6$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	$0.25t_{CK} - 6$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	$0.25t_{CK} - 5$	$0.25\ t_{CK} + 7$	ns
t_{AW}	A0-A13, $\overline{xMS}$, Setup before $\overline{WR}$ Deasserted	$0.75t_{CK} - 9 + w$		ns
t_{WRA}	A0-A13, $\overline{xMS}$ Hold after $\overline{WR}$ Deasserted	$0.25t_{CK} - 3$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	$0.5t_{CK} - 5$		ns

w = wait states x t_{CK}
$\overline{xMS}$ = $\overline{PMS}$, $\overline{DMS}$, $\overline{CMS}$, $\overline{IOMS}$, $\overline{BMS}$

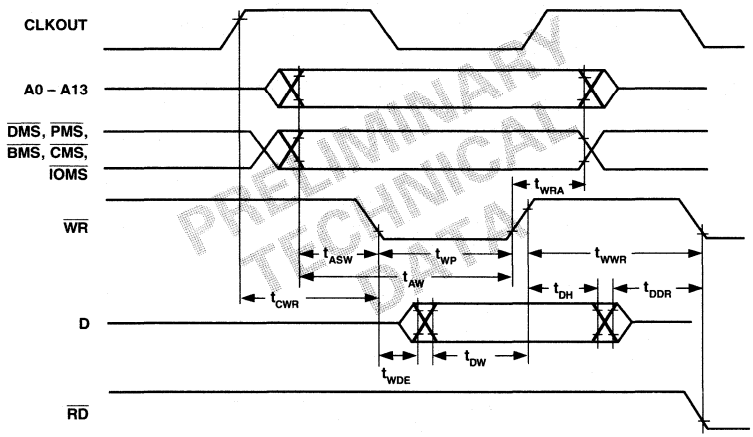


Figure 12. Memory Write

Parameter		Min	Max	Unit
Serial Ports				
Timing Requirement:				
t_{SCK}	SCLK Period	50		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	4		ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	7		ns
t_{SCP}	$SCLK_{IN}$ Width	20		ns
Switching Characteristic:				
t_{CC}	CLKOUT High to $SCLK_{OUT}$	$0.25t_{CK}$	$0.25t_{CK} + 10$	ns
t_{SCDE}	SCLK High to DT Enable	0		ns
t_{SCDV}	SCLK High to DT Valid		15	ns
t_{RH}	TFS/RFS_{OUT} Hold after SCLK High	0		ns
t_{RD}	TFS/RFS_{OUT} Delay from SCLK High		15	ns
t_{SCDH}	DT Hold after SCLK High	0		ns
t_{TDE}	TFS (Alt) to DT Enable	0		ns
t_{TDV}	TFS (Alt) to DT Valid		14	ns
t_{SCDD}	SCLK High to DT Disable		15	ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		15	ns

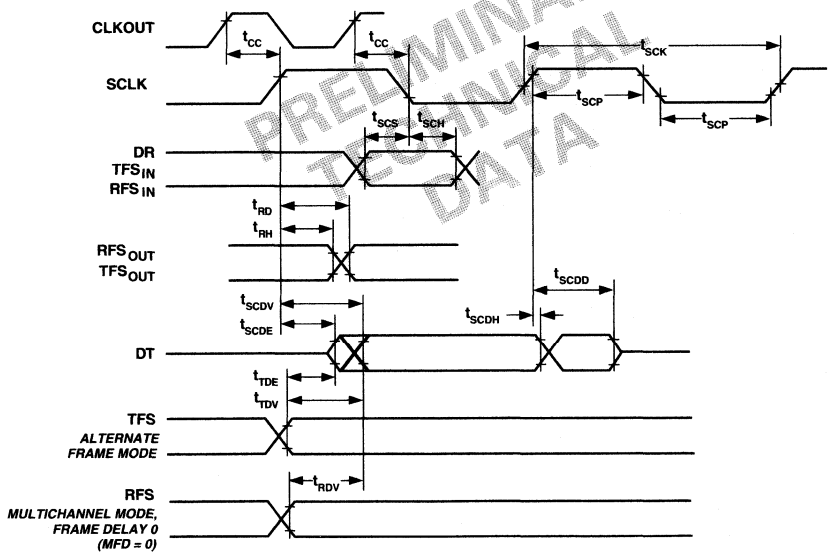


Figure 13. Serial Ports

Parameter		Min	Max	Unit
IDMA Address Latch				
Timing Requirement:				
t_{IALP}	Duration of Address Latch[1, 3]	10		ns
t_{IASU}	IAD15–0 Address Setup before Address Latch End[3]	5		ns
t_{IAH}	IAD15–0 Address Hold after Address Latch End[3]	2		ns
t_{IKA}	$\overline{IACK}$ Low before Start of Address Latch[1]	5		ns
t_{IALS}	Start of Write or Read after Address Latch End[2, 3]	5		ns

NOTES
[1]Start of Address Latch = $\overline{IS}$ Low and $\overline{IAL}$ High.
[2]Start of Write or Read = $\overline{IS}$ Low and $\overline{IWR}$ Low or $\overline{IRD}$ Low.
[3]End of Address Latch = $\overline{IS}$ High or $\overline{IAL}$ Low.

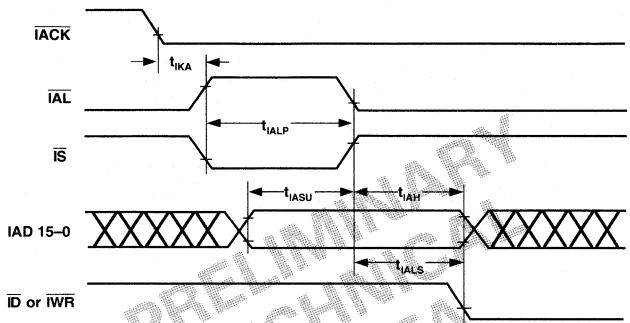


Figure 14. IDMA Address Latch

Parameter		Min	Max	Unit
IDMA Write, Short Write Cycle				
Timing Requirement:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	5		ns
t_{IWP}	Duration of Write[1, 2]	15		ns
t_{IDSU}	IAD15-0 Data Setup before End of Write[2, 3, 4]	5		ns
t_{IDH}	IAD15-0 Data Hold after End of Write[2, 3, 4]	2		ns
Switching Characteristic:				
t_{IKHW}	Start of Write to $\overline{IACK}$ High		15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]End of Write = $\overline{IS}$ High or $\overline{IWR}$ High.
[3]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[4]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.

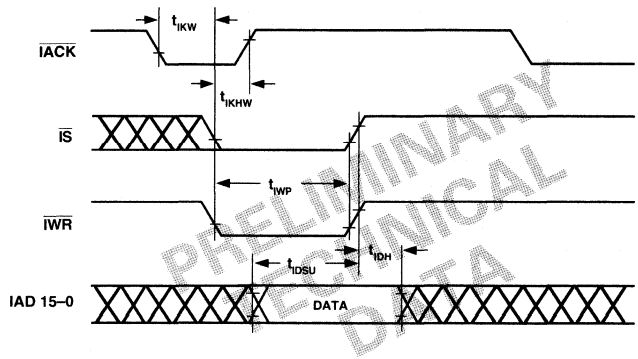


Figure 15. IDMA Write, Short Write Cycle

Parameter		Min	Max	Unit
IDMA Write, Long Write Cycle				
Timing Requirement:				
t_{IKW}	$\overline{IACK}$ Low before Start of Write[1]	5		ns
t_{IKSU}	IAD15–0 Data Setup before $\overline{IACK}$ Low[2, 3]	$0.5t_{CK}$ + 10		ns
t_{IKH}	IAD15–0 Data Hold after $\overline{IACK}$ Low[2, 3]	2		ns
Switching Characteristic:				
t_{IKLW}	Start of Write to $\overline{IACK}$ Low[4]	$1.5t_{CK}$		ns
t_{IKHW}	Start of Write to $\overline{IACK}$ High		15	ns

NOTES
[1]Start of Write = $\overline{IS}$ Low and $\overline{IWR}$ Low.
[2]If Write Pulse ends before $\overline{IACK}$ Low, use specifications t_{IDSU}, t_{IDH}.
[3]If Write Pulse ends after $\overline{IACK}$ Low, use specifications t_{IKSU}, t_{IKH}.
[4]This is the earliest time for $\overline{IACK}$ Low from Start of Write. For IDMA Write cycle relationships, please refer to the User's Manual.

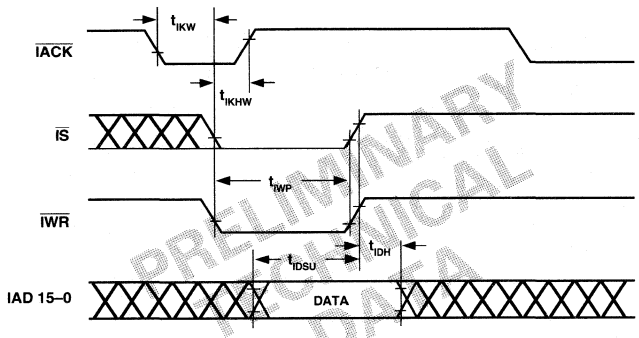


Figure 16. IDMA Write, Long Write Cycle

Parameter		Min	Max	Unit
IDMA Read				
Timing Requirement:				
t_{IKR}	$\overline{IACK}$ Low before Start of Read[1]	5		ns
t_{IRP}	Duration of Read	15		ns
Switching Characteristic:				
t_{IKHR}	$\overline{IACK}$ High after Start of Read[1]		15	ns
t_{IKDS}	IAD15–0 Data Setup before IACK Low	$0.5t_{CK}$ –10		ns
t_{IKDH}	IAD15–0 Data Hold after End of Read[2]	0		ns
t_{IKDD}	IAD15–0 Data Disabled after End of Read[2]		10	ns
t_{IRDE}	IAD15–0 Previous Data Enabled after Start of Read	TBD		ns
t_{IRDV}	IAD15–0 Previous Data Valid after Start of Read		TBD	ns
t_{IRDH}	IAD15–0 Previous Data Hold after Start of Read	TBD		ns

NOTES
[1]Start of Read = $\overline{IS}$ Low and $\overline{IRD}$ Low.
[2]End of Read = $\overline{IS}$ High or $\overline{IRD}$ High.

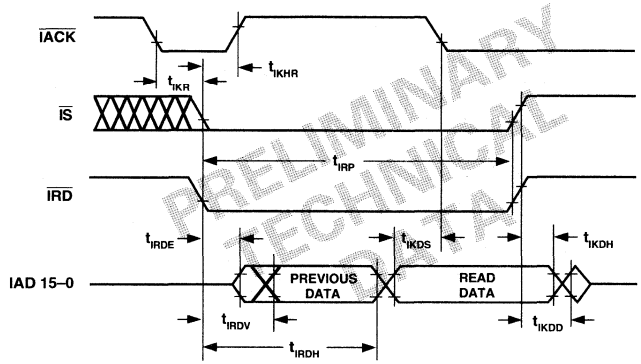


Figure 17. IDMA Read

ENVIRONMENTAL CONDITIONS

Ambient Temperature Rating:

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$
T_{CASE} = Case Temperature in °C
PD = Power Dissipation in W
θ_{CA} = Thermal Resistance (Case-to-Ambient)
θ_{JA} = Thermal Resistance (Junction-to-Ambient)
θ_{JC} = Thermal Resistance (Junction-to-Case)

Package	θ_{JA}	θ_{JC}	θ_{CA}
TQFP	50°C/W	2°C/W	48°C/W
PQFP	41°C/W	10°C/W	31°C/W

POWER DISSIPATION

To determine total power dissipation in a specific application, the following equation should be applied for each output:

$$C \times V_{DD}^2 \times f$$

C = load capacitance, f = output switching frequency.

Example:
In an application where external data memory is used and no other outputs are active, power dissipation is calculated as follows:

Assumptions:

- External data memory is accessed every cycle with 50% of the address pins switching.
- External data memory writes occur every other cycle with 50% of the data pins switching.
- Each address and data pin has a 10 pF total load at the pin.
- The application operates at V_{DD} = 5.0 V and t_{CK} = 30 ns.

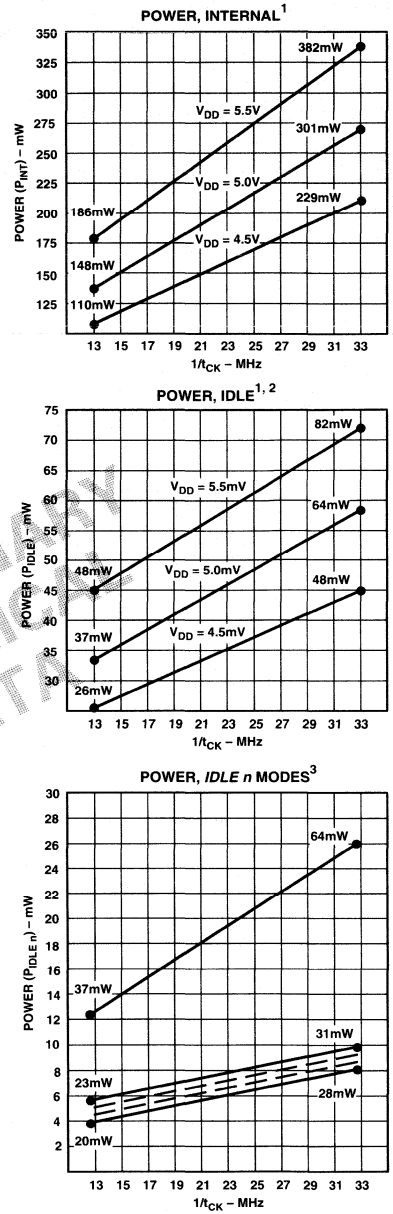
Total Power Dissipation = P_{INT} + $(C \times V_{DD}^2 \times f)$

P_{INT} = internal power dissipation from Power vs. Frequency graph (Figure 18).

$(C \times V_{DD}^2 \times f)$ is calculated for each output:

	# of Pins	× C	× V_{DD}^2	× f		
Address, $\overline{DMS}$	8	× 10 pF	× 5^2 V	× 33.3 MHz	=	66.6 mW
Data Output, $\overline{WR}$	9	× 10 pF	× 5^2 V	× 16.67 MHz	=	37.5 mW
$\overline{RD}$	1	× 10 pF	× 5^2 V	× 16.67 MHz	=	4.2 mW
CLKOUT	1	× 10 pF	× 5^2 V	× 33.3 MHz	=	8.3 mW
						116.6 mW

Total power dissipation for this example is P_{INT} + 116.6 mW.



VALID FOR ALL TEMPERATURE GRADES.
[1] POWER REFLECTS DEVICE OPERATING WITH NO OUTPUT LOADS.
[2] IDLE REFERS TO ADSP-2181 STATE OF OPERATION DURING EXECUTION OF IDLE INSTRUCTION. DEASSERTED PINS ARE DRIVEN TO EITHER V_{DD} OR GND.
[3] TYPICAL POWER DISSIPATION AT 5.0V V_{DD} DURING EXECUTION OF *IDLE n* INSTRUCTION (CLOCK FREQUENCY REDUCTION).

Figure 18. Power vs. Frequency

CAPACITIVE LOADING

Figures 19 and 20 show the capacitive loading characteristics of the ADSP-2181.

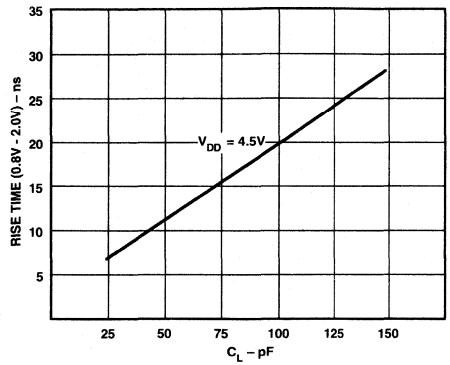


Figure 19. Typical Output Rise Time vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

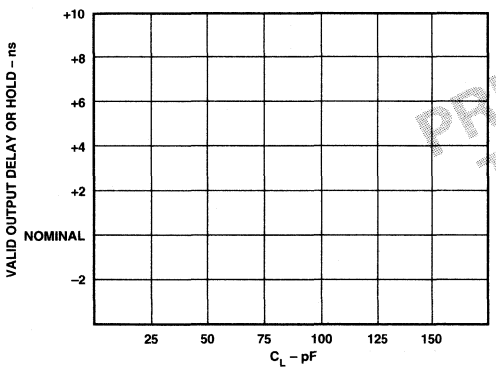


Figure 20. Typical Output Valid Delay or Hold vs. Load Capacitance, C_L (at Maximum Ambient Operating Temperature)

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \bullet 0.5V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

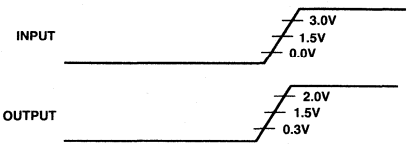


Figure 21. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time

Output pins are considered to be enabled when that have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

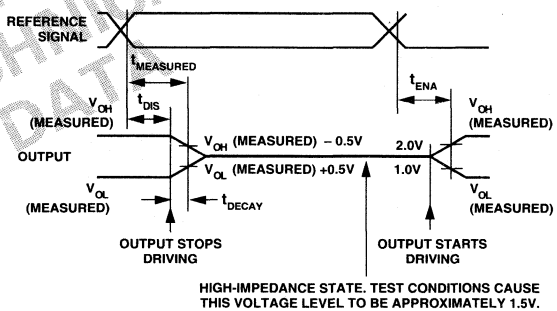


Figure 22. Output Enable/Disable

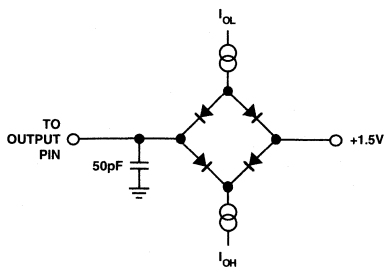
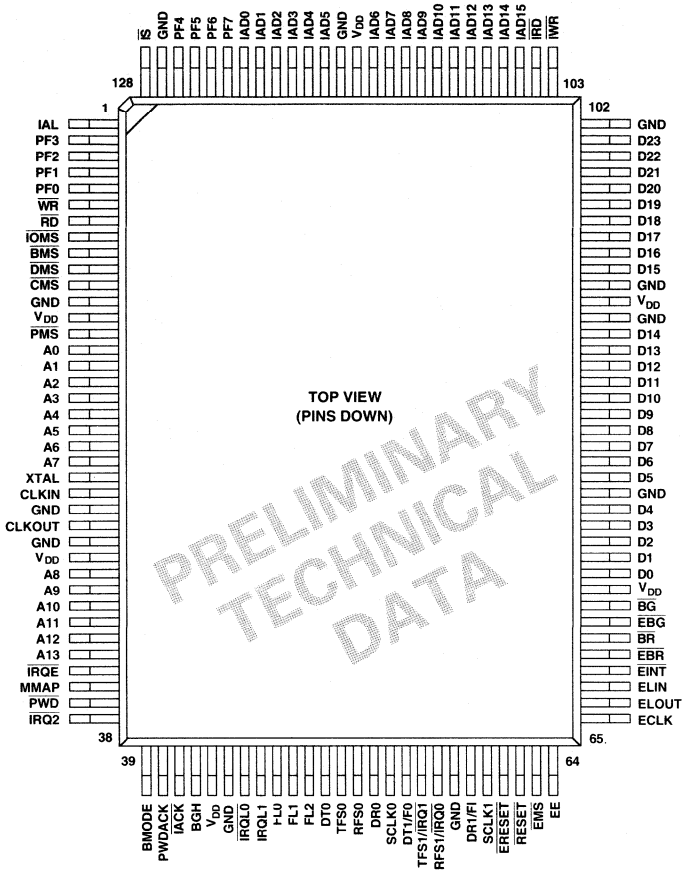


Figure 23. Equivalent Device Loading for AC Measurements (Including All Fixtures)

128-Lead TQFP Package Pinout



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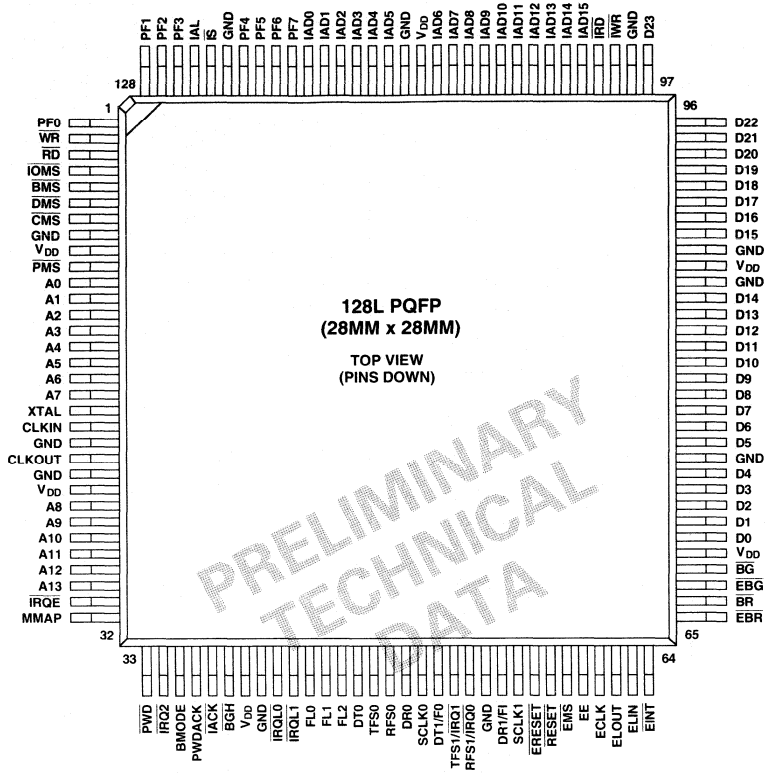
This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

TQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	IAL	33	A12	65	ECLK	97	D19
2	PF3	34	A13	66	ELOUT	98	D20
3	PF2	35	$\overline{\text{IRQE}}$	67	ELIN	99	D21
4	PF1	36	MMAP	68	$\overline{\text{EINT}}$	100	D22
5	PF0	37	$\overline{\text{PWD}}$	69	$\overline{\text{EBR}}$	101	D23
6	$\overline{\text{WR}}$	38	$\overline{\text{IRQ2}}$	70	$\overline{\text{BR}}$	102	GND
7	$\overline{\text{RD}}$	39	BMODE	71	$\overline{\text{EBG}}$	103	$\overline{\text{IWR}}$
8	$\overline{\text{IOMS}}$	40	PWDACK	72	$\overline{\text{BG}}$	104	$\overline{\text{IRD}}$
9	$\overline{\text{BMS}}$	41	$\overline{\text{IACK}}$	73	VDD	105	IAD15
10	$\overline{\text{DMS}}$	42	BGH	74	D0	106	IAD14
11	$\overline{\text{CMS}}$	43	VDD	75	D1	107	IAD13
12	GND	44	GND	76	D2	108	IAD12
13	VDD	45	$\overline{\text{IRQL0}}$	77	D3	109	IAD11
14	$\overline{\text{PMS}}$	46	$\overline{\text{IRQL1}}$	78	D4	110	IAD10
15	A0	47	FL0	79	GND	111	IAD9
16	A1	48	FL1	80	D5	112	IAD8
17	A2	49	FL2	81	D6	113	IAD7
18	A3	50	DT0	82	D7	114	IAD6
19	A4	51	TFS0	83	D8	115	VDD
20	A5	52	RFS0	84	D9	116	GND
21	A6	53	DR0	85	D10	117	IAD5
22	A7	54	SCLK0	86	D11	118	IAD4
23	XTAL	55	DT1/F0	87	D12	119	IAD3
24	CLKIN	56	TFS1/$\overline{\text{IRQ1}}$	88	D13	120	IAD2
25	GND	57	RFS1/$\overline{\text{IRQ0}}$	89	D14	121	IAD1
26	CLKOUT	58	GND	90	GND	122	IAD0
27	GND	59	DR1/FI	91	VDD	123	PF7
28	VDD	60	SCLK1	92	GND	124	PF6
29	A8	61	$\overline{\text{ERESET}}$	93	D15	125	PF5
30	A9	62	$\overline{\text{RESET}}$	94	D16	126	PF4
31	A10	63	$\overline{\text{EMS}}$	95	D17	127	GND
32	A11	64	EE	96	D18	128	$\overline{\text{IS}}$

128-Lead PQFP Package Pinout



PQFP Pin Configurations

TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name	TQFP Number	Pin Name
1	PF0	33	$\overline{PWD}$	65	$\overline{EBR}$	97	D23
2	$\overline{WR}$	34	$\overline{IRQ2}$	66	$\overline{BR}$	98	GND
3	$\overline{RD}$	35	BMODE	67	$\overline{EBG}$	99	$\overline{IWR}$
4	$\overline{IOMS}$	36	PWDACK	68	$\overline{BG}$	100	$\overline{IRD}$
5	$\overline{BMS}$	37	$\overline{IACK}$	69	VDD	101	IAD15
6	$\overline{DMS}$	38	$\overline{BGH}$	70	D0	102	IAD14
7	$\overline{CMS}$	39	VDD	71	D1	103	IAD13
8	GND	40	GND	72	D2	104	IAD12
9	VDD	41	$\overline{IRQL0}$	73	D3	105	IAD11
10	$\overline{PMS}$	42	$\overline{IRQL1}$	74	D4	106	IAD10
11	A0	43	FL0	75	GND	107	IAD9
12	A1	44	FL1	76	D5	108	IAD8
13	A2	45	FL2	77	D6	109	IAD7
14	A3	46	DT0	78	D7	110	IAD6
15	A4	47	TFS0	79	D8	111	VDD
16	A5	48	RFS0	80	D9	112	GND
17	A6	49	DR0	81	D10	113	IAD5
18	A7	50	SCLK0	82	D11	114	IAD4
19	XTAL	51	DT1/F0	83	D12	115	IAD3
20	CLKIN	52	TFS1/$\overline{IRQ1}$	84	D13	116	IAD2
21	GND	53	RFS1/$\overline{IRQ0}$	85	D14	117	IAD1
22	CLKOUT	54	GND	86	GND	118	IAD0
23	GND	55	DR1/FI	87	VDD	119	PF7
24	VDD	56	SCLK1	88	GND	120	PF6
25	A8	57	$\overline{ERESET}$	89	D15	121	PF5
26	A9	58	$\overline{RESET}$	90	D16	122	PF4
27	A10	59	$\overline{EMS}$	91	D17	123	GND
28	A11	60	EE	92	D18	124	$\overline{IS}$
29	A12	61	ECLK	93	D19	125	IAL
30	A13	62	ELOUT	94	D20	126	PF3
31	$\overline{IRQE}$	63	ELIN	95	D21	127	PF2
32	MMAP	64	$\overline{EINT}$	96	D22	128	PF1

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option[1, 2]
ADSP-2181KST-115	0°C to +70°C	28.8	128-Lead TQFP[3]	ST-128
ADSP-2181BST-115	–40°C to +85°C	28.8	128-Lead TQFP[3]	ST-128
ADSP-2181KS-115	0°C to +70°C	28.8	128-Lead PQFP	ST-128
ADSP-2181BS-115	–40°C to +85°C	28.8	128-Lead PQFP	ST-128
ADSP-2181KST-133	0°C to +70°C	33.3	128-Lead TQFP[3]	ST-128
ADSP-2181BST-133	–40°C to +85°C	33.3	128-Lead TQFP[3]	ST-128
ADSP-2181KS-133	0°C to +70°C	33.3	128-Lead PQFP	S-128
ADSP-2181BS-133	–40°C to +85°C	33.3	128-Lead PQFP	S-128

NOTES
[1]S = Plastic Quad Flatpack, ST = Plastic Thin Quad Flatpack
[2]For outline information see Package Information section.
[3]128-lead TQFP available in quantities of 10,000 units or more.

ANALOG DEVICES

32/40-Bit IEEE Floating-Point DSP Microprocessor

ADSP-21020

FEATURES

Superscalar IEEE Floating-Point Processor
Off-Chip Harvard Architecture Maximizes Signal Processing Performance
30 ns, 33.3 MIPS Instruction Rate, Single-Cycle Execution
100 MFLOPS Peak, 66 MFLOPS Sustained Performance
1024-Point Complex FFT Benchmark: 0.58 ms
Divide (y/x): 180 ns
Inverse Square Root ($1/\sqrt{x}$): 270 ns
32-Bit Single-Precision and 40-Bit Extended-Precision IEEE Floating-Point Data Formats
32-Bit Fixed-Point Formats, Integer and Fractional, with 80-Bit Accumulators
IEEE Exception Handling with Interrupt on Exception
Three Independent Computation Units: Multiplier, ALU, and Barrel Shifter
Dual Data Address Generators with Indirect, Immediate, Modulo, and Bit Reverse Addressing Modes
Two Off-Chip Memory Transfers in Parallel with Instruction Fetch and Single-Cycle Multiply & ALU Operations
Multiply with Add & Subtract for FFT Butterfly Computation
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
Single-Cycle Register File Context Switch
15 (or 25) ns External RAM Access Time for Zero-Wait-State, 30 (or 40) ns Instruction Execution
IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation Circuitry
223-Pin PGA Package (Ceramic)

GENERAL DESCRIPTION

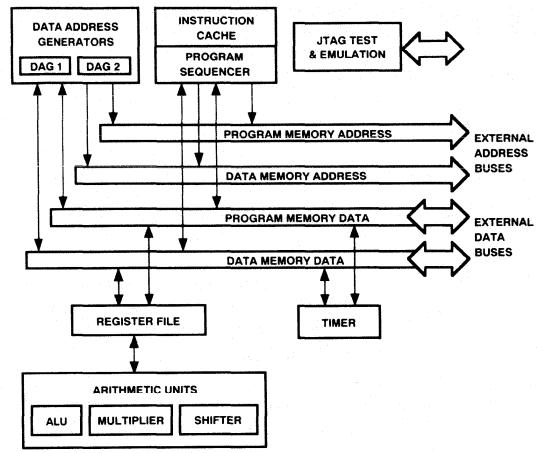
The ADSP-21020 is the first member of Analog Devices' family of single-chip IEEE floating-point processors optimized for digital signal processing applications. Its architecture is similar to that of Analog Devices' ADSP-2100 family of fixed-point DSP processors.

Fabricated in a high-speed, low-power CMOS process, the ADSP-21020 has a 30 ns instruction cycle time. With a high-performance on-chip instruction cache, the ADSP-21020 can execute every instruction in a single cycle.

The ADSP-21020 features:

- **Independent Parallel Computation Units**
  The arithmetic/logic unit (ALU), multiplier and shifter perform single-cycle instructions. The units are architecturally arranged in parallel, maximizing computational throughput. A single multifunction instruction executes parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.

FUNCTIONAL BLOCK DIAGRAM



- **Data Register File**
  A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port (16-register) register file, combined with the ADSP-21020's Harvard architecture, allows unconstrained data flow between computation units and off-chip memory.
- **Single-Cycle Fetch of Instruction and Two Operands**
  The ADSP-21020 uses a modified Harvard architecture in which data memory stores data and program memory stores both instructions and data. Because of its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch an operand from data memory, an operand from program memory, and an instruction from the cache, all in a single cycle.
- **Memory Interface**
  Addressing of external memory devices by the ADSP-21020 is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM.
  The ADSP-21020 provides programmable memory wait states, and external memory acknowledge controls allow interfacing to peripheral devices with variable access times.
- **Instruction Cache**
  The ADSP-21020 includes a high performance instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the

instructions whose fetches conflict with program memory data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.

- **Hardware Circular Buffers**
  The ADSP-21020 provides hardware to implement circular buffers in memory, which are common in digital filters and Fourier transform implementations. It handles address pointer wraparound, reducing overhead (thereby increasing performance) and simplifying implementation. Circular buffers can start and end at any location.
- **Flexible Instruction Set**
  The ADSP-21020's 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-21020 can conditionally execute a multiply, an add, a subtract and a branch in a single instruction.

DEVELOPMENT SYSTEM

The ADSP-21020 is supported with a complete set of software and hardware development tools. The ADSP-21000 Family Development System includes development software, an evaluation board and an in-circuit emulator.

- **Assembler**
  Creates relocatable, COFF (Common Object File Format) object files from ADSP-21xxx assembly source code. It accepts standard C preprocessor directives for conditional assembly and macro processing. The algebraic syntax of the ADSP-21xxx assembly language facilitates coding and debugging of DSP algorithms.
- **Linker/Librarian**
  The Linker processes separately assembled object files and library files to create a single executable program. It assigns memory locations to code and to data in accordance with a user-defined architecture file that describes the memory and I/O configuration of the target system. The Librarian allows you to group frequently used object files into a single library file that can be linked with your main program.
- **Simulator**
  The Simulator performs interactive, instruction-level simulation of ADSP-21xxx code within the hardware configuration described by a system architecture file. It flags illegal operations and supports full symbolic disassembly. It provides an easy-to-use, window oriented, graphical user interface that is identical to the one used by the ADSP-21020 EZ-ICE Emulator. Commands are accessed from pull-down menus with a mouse.
- **PROM Splitter**
  Formats an executable file into files that can be used with an industry-standard PROM programmer.
- **C Compiler and Runtime Library**
  The C Compiler complies with ANSI specifications. It takes advantage of the ADSP-21020's high-level language architectural features and incorporates optimizing algorithms to speed up the execution of code. It includes an extensive runtime library with over 100 standard and DSP-specific functions.
- **C Source Level Debugger**
  A full-featured C source level debugger that works with the simulator or EZ-ICE emulator to allow debugging of assembler source, C source, or mixed assembler and C.
- **Numerical C Compiler**
  Supports ANSI Standard (X3J11.1) Numerical C as defined by the Numeric C Extensions Group. The compiler accepts C source input containing Numerical C extensions for array selection, vector math operations, complex data types, circular pointers, and variably dimensioned arrays, and outputs ADSP-21xxx assembly language source code.
- **ADSP-21020 EZ-LAB® Evaluation Board**
  The EZ-LAB Evaluation Board is a general-purpose, stand-alone ADSP-21020 system that includes 32K words of program memory and 32K words of data memory as well as analog I/O. A PC RS-232 download path enables the user to download and run programs directly on the EZ-LAB. In addition, it may be used in conjunction with the EZ-ICE Emulator to provide a powerful software debug environment.
- **ADSP-21020 EZ-ICE® Emulator**
  This in-circuit emulator provides the system designer with a PC-based development environment that allows nonintrusive access to the ADSP-21020's internal registers through the processor's 5-pin JTAG Test Access Port. This use of on-chip emulation circuitry enables reliable, full-speed performance in any target. The emulator uses the same graphical user interface as the ADSP-21020 Simulator, allowing an easy transition from software to hardware debug. (See "Target System Requirements for Use of EZ-ICE Emulator" on page 27.)

ADDITIONAL INFORMATION

This data sheet provides a general overview of ADSP-21020 functionality. For additional information on the architecture and instruction set of the processor, refer to the *ADSP-21020 User's Manual*. For development system and programming reference information, refer to the *ADSP-21000 Family Development Software Manuals* and the *ADSP-21020 Programmer's Quick Reference*. Applications code listings and benchmarks for key DSP algorithms are available on the DSP Applications BBS; call (617) 461-4258, 8 data bits, no parity, 1 stop bit, 300/1200/2400/9600 baud.

ARCHITECTURE OVERVIEW

Figure 1 shows a block diagram of the ADSP-21020. The processor features:

- Three Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Two Data Address Generators (DAG 1, DAG 2)
- Program Sequencer with Instruction Cache
- 32-Bit Timer
- Memory Buses and Interface
- JTAG Test Access Port and On-Chip Emulation Support

Computation Units

The ADSP-21020 contains three independent computation units: an ALU, a multiplier with fixed-point accumulator, and a shifter. In order to meet a wide variety of processing needs, the computation units process data in three formats: 32-bit fixed-point, 32-bit floating-point and 40-bit floating-point. The floating-point operations are single-precision IEEE-compatible (IEEE Standard 754/854). The 32-bit floating-point format is the standard IEEE format, whereas the 40-bit IEEE extended-precision format has eight additional LSBs of mantissa for greater accuracy.

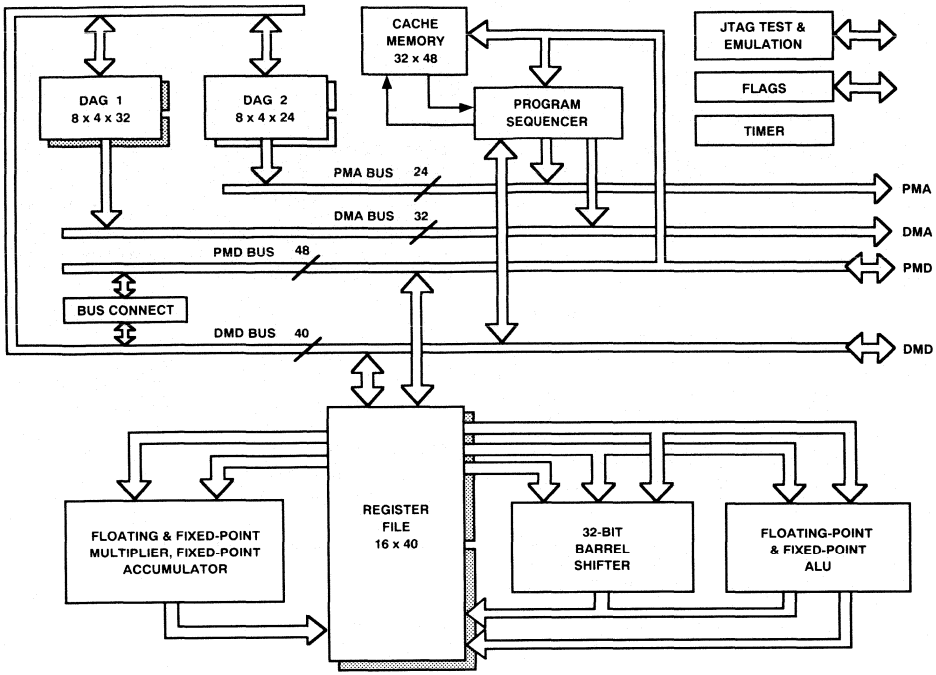


Figure 1. ADSP-21020 Block Diagram

The multiplier performs floating-point and fixed-point multiplication as well as fixed-point multiply/add and multiply/subtract operations. Integer products are 64 bits wide, and the accumulator is 80 bits wide. The ALU performs 45 standard arithmetic and logic operations, supporting both fixed-point and floating-point formats. The shifter performs 19 different operations on 32-bit operands. These operations include logical and arithmetic shifts, bit manipulation, field deposit, and extract and derive exponent operations.

The computation units perform single-cycle operations; there is *no* computation pipeline. The three units are connected in parallel rather than serially, via multiple-bus connections with the 10-port data register file. The output of any computation unit may be used as the input of any unit on the next cycle. In a *multifunction* computation, the ALU and multiplier perform independent, simultaneous operations.

Data Register File

The ADSP-21020's general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. The register file has two sets (primary and alternate) of sixteen 40-bit registers each, for fast context switching.

With a large number of buses connecting the registers to the computation units, data flow between computation units and from/to off-chip memory is unconstrained and free from bottlenecks. The 10-port register file and Harvard architecture of the ADSP-21020 allow the following nine data transfers to be performed every cycle:

- Off-chip read/write of two operands to or from the register file
- Two operands supplied to the ALU
- Two operands supplied to the multiplier
- Two results received from the ALU and multiplier (three, if the ALU operation is a combined addition/subtraction)

The processor's 48-bit orthogonal instruction word supports fully parallel data transfer and arithmetic operations in the same instruction.

Address Generators and Program Sequencer

Two dedicated address generators and a program sequencer supply addresses for memory accesses. Because of this, the computation units need never be used to calculate addresses. Because of its instruction cache, the ADSP-21020 can simultaneously fetch an instruction and data values from both off-chip program memory and off-chip data memory in a single cycle.

The data address generators (DAGs) provide memory addresses when external memory data is transferred over the parallel memory ports to or from internal registers. Dual data address generators enable the processor to output two simultaneous addresses for dual operand reads and writes. DAG 1 supplies 32-bit addresses to data memory. DAG 2 supplies 24-bit addresses to program memory for program memory data accesses.

Each DAG keeps track of up to eight address pointers, eight modifiers, eight buffer length values and eight base values. A pointer used for indirect addressing can be modified by a value in a specified register, either before (premodify) or after (post-modify) the access. To implement automatic modulo addressing for circular buffers, the ADSP-21020 provides buffer length registers that can be associated with each pointer. Base values for pointers allow circular buffers to be placed at arbitrary locations. Each DAG register has an alternate register that can be activated for fast context switching.

The program sequencer supplies instruction addresses to program memory. It controls loop iterations and evaluates conditional instructions. To execute looped code with zero overhead, the ADSP-21020 maintains an internal loop counter and loop stack. No explicit jump or decrement instructions are required to maintain the loop.

The ADSP-21020 derives its high clock rate from pipelined *fetch, decode* and *execute* cycles. Approximately 70% of the machine cycle is available for memory accesses; consequently, ADSP-21020 systems can be built using slower and therefore less expensive memory chips.

Instruction Cache

The program sequencer includes a high performance, selective instruction cache that enables three-bus operation for fetching an instruction and two data values. This two-way, set-associative cache holds 32 instructions. The cache is selective—only the instructions whose fetches conflict with program memory data accesses are cached, so the ADSP-21020 can perform a program memory data access and can execute the corresponding instruction in the same cycle. The program sequencer fetches the instruction from the cache instead of from program memory, enabling the ADSP-21020 to simultaneously access data in both program memory and data memory.

Context Switching

Many of the ADSP-21020's registers have alternate register sets that can be activated during interrupt servicing to facilitate a fast context switch. The data registers in the register file, DAG registers and the multiplier result register all have alternate sets. Registers active at reset are called *primary* registers; the others are called *alternate* registers. Bits in the MODE1 control register determine which registers are active at any particular time.

The primary/alternate select bits for each half of the register file (top eight or bottom eight registers) are independent. Likewise, the top four and bottom four register sets in each DAG have independent primary/alternate select bits. This scheme allows passing of data between contexts.

Interrupts

The ADSP-21020 has four external hardware interrupts, nine internally generated interrupts, and eight software interrupts. For the external interrupts and the internal timer interrupt, the ADSP-21020 automatically stacks the arithmetic status and mode (MODE1) registers when servicing the interrupt, allowing five nesting levels of fast service for these interrupts.

An interrupt can occur at any time while the ADSP-21020 is executing a program. Internal events that generate interrupts include arithmetic exceptions, which allow for fast trap handling and recovery.

Timer

The programmable interval timer provides periodic interrupt generation. When enabled, the timer decrements a 32-bit count register every cycle. When this count register reaches zero, the ADSP-21020 generates an interrupt and asserts its TIMEXP output. The count register is automatically reloaded from a 32-bit period register and the count resumes immediately.

System Interface

Figure 2 shows an ADSP-21020 basic system configuration.

The external memory interface supports memory-mapped peripherals and slower memory with a user-defined combination of programmable wait states and hardware acknowledge signals. Both the program memory and data memory interfaces support addressing of page-mode DRAMs.

The ADSP-21020's internal functions are supported by four internal buses: the program memory address (PMA) and data memory address (DMA) buses are used for addresses associated with program and data memory. The program memory data (PMD) and data memory data (DMD) buses are used for data associated with the two memory spaces. These buses are extended off chip. Four data memory select (DMS) signals select one of four user-configurable banks of data memory. Similarly, two program memory select (PMS) signals select between two user-configurable banks of program memory. All banks are independently programmable for 0–7 wait states.

The PX registers permit passing data between program memory and data memory spaces. They provide a bridge between the 48-bit PMD bus and the 40-bit DMD bus or between the 40-bit register file and the PMD bus.

The PMA bus is 24 bits wide allowing direct access of up to 16M words of mixed instruction code and data. The PMD is 48 bits wide to accommodate the 48-bit instruction width. For access of 40-bit data the lower 8 bits are unused. For access of 32-bit data the lower 16 bits are ignored.

The DMA bus is 32 bits wide allowing direct access of up to 4 Gigawords of data. The DMD bus is 40 bits wide. For 32-bit data, the lower 8 bits are unused. The DMD bus provides a path for the contents of any register in the processor to be transferred to any other register or to any external data memory location in a single cycle. The data memory address comes from one of two sources: an absolute value specified in the instruction code (direct addressing) or the output of a data address generator (indirect addressing).

External devices can gain control of the processor's memory buses from the ADSP-21020 by means of the bus request/grant signals ($\overline{BR}$ and $\overline{BG}$). To grant its buses in response to a bus request, the ADSP-21020 halts internal operations and places its program and data memory interfaces in a high impedance state. In addition, three-state controls ($\overline{DMTS}$ and $\overline{PMTS}$) allow an external device to place either the program or data memory interface in a high impedance state without affecting the other interface and without halting the ADSP-21020 unless it requires a memory access from the affected interface. The three-state controls make it easy for an external cache controller to hold the ADSP-21020 off the bus while it updates an external cache memory.

JTAG Test and Emulation Support

The ADSP-21020 implements the boundary scan testing provisions specified by IEEE Standard 1149.1 of the Joint Testing Action Group (JTAG). The ADSP-21020's test access port and on-chip JTAG circuitry is fully compliant with the IEEE 1149.1 specification. The test access port enables boundary scan testing of circuitry connected to the ADSP-21020's I/O pins.

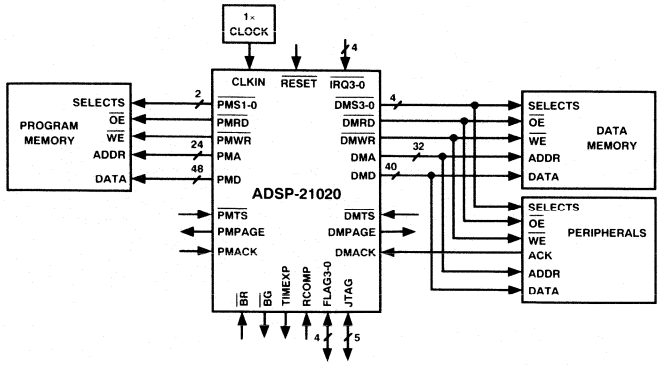


Figure 2. Basic System Configuration

The ADSP-21020 also implements on-chip emulation through the JTAG test access port. The processor's eight sets of breakpoint range registers enable program execution at full speed until reaching a desired breakpoint address range. The processor can then halt and allow reading/writing of all the processor's internal registers and external memories through the JTAG port.

PIN DESCRIPTIONS

This section describes the pins of the ADSP-21020. When groups of pins are identified with subscripts, e.g. PMD_{47-0}, the highest numbered pin is the MSB (in this case, PMD_{47}). Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI, and $\overline{TRST}$). Those that are asynchronous (A) can be asserted asynchronously to CLKIN.

O = Output; I = Input; S = Synchronous; A = Asynchronous; P = Power Supply; G = Ground.

Pin Name	Type	Function
$\overline{PMA}_{23-0}$	O	Program Memory Address. The ADSP-21020 outputs an address in program memory on these pins.
PMD_{47-0}	I/O	Program Memory Data. The ADSP-21020 inputs and outputs data and instructions on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 47–16 of the PMD bus.
$\overline{PMS}_{1-0}$	O	Program Memory Select lines. These pins are asserted as chip selects for the corresponding banks of program memory. Memory banks must be defined in the memory control registers. These pins are decoded program memory address lines and provide an early indication of a possible bus cycle.
$\overline{PMRD}$	O	Program Memory Read strobe. This pin is asserted when the ADSP-21020 reads from program memory.
$\overline{PMWR}$	O	Program Memory Write strobe. This pin is asserted when the ADSP-21020 writes to program memory.
PMACK	I/S	Program Memory Acknowledge. An external device deasserts this input to add wait states to a memory access.
PMPAGE	O	Program Memory Page Boundary. The ADSP-21020 asserts this pin to signal that a program memory page boundary has been crossed. Memory pages must be defined in the memory control registers.
$\overline{PMTS}$	I/S	Program Memory Three-State Control. $\overline{PMTS}$ places the program memory address, data, selects, and strobes in a high-impedance state. If $\overline{PMTS}$ is asserted while a PM access is occurring, the processor will halt and the memory access will not be completed. PMACK must be asserted for at least one cycle when $\overline{PMTS}$ is deasserted to allow any pending memory access to complete properly. $\overline{PMTS}$ should only be asserted (low) during an active memory access cycle.
DMA_{31-0}	O	Data Memory Address. The ADSP-21020 outputs an address in data memory on these pins.
DMD_{39-0}	I/O	Data Memory Data. The ADSP-21020 inputs and outputs data on these pins. 32-bit fixed-point data and 32-bit single-precision floating-point data is transferred over bits 39-8 of the DMD bus.
$\overline{DMS}_{3-0}$	O	Data Memory Select lines. These pins are asserted as chip selects for the corresponding banks of data memory. Memory banks must be defined in the memory control registers. These pins are decoded data memory address lines and provide an early indication of a possible bus cycle.
$\overline{DMRD}$	O	Data Memory Read strobe. This pin is asserted when the ADSP-21020 reads from data memory.
$\overline{DMWR}$	O	Data Memory Write strobe. This pin is asserted when the ADSP-21020 writes to data memory.
DMACK	I/S	Data Memory Acknowledge. An external device deasserts this input to add wait states to a memory access.

Pin Name	Type	Function
$\overline{\text{DMPAGE}}$	O	Data Memory Page Boundary. The ADSP-21020 asserts this pin to signal that a data memory page boundary has been crossed. Memory pages must be defined in the memory control registers.
$\overline{\text{DMTS}}$	I/S	Data Memory Three-State Control. $\overline{\text{DMTS}}$ places the data memory address, data, selects, and strobes in a high-impedance state. If $\overline{\text{DMTS}}$ is asserted while a DM access is occurring, the processor will halt and the memory access will not be completed. DMACK must be asserted for at least one cycle when $\overline{\text{DMTS}}$ is deasserted to allow any pending memory access to complete properly. $\overline{\text{DMTS}}$ should only be asserted (low) during an active memory access cycle.
CLKIN	I	External clock input to the ADSP-21020. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{\text{RESET}}$	I/A	Sets the ADSP-21020 to a known state and begins execution at the program memory location specified by the hardware reset vector (address). This input must be asserted (low) at power-up.
$\overline{\text{IRQ}}_{3-0}$	I/A	Interrupt request lines; may be either edge-triggered or level-sensitive.
FLAG_{3-0}	I/O/A	External Flags. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
$\overline{\text{BR}}$	I/A	Bus Request. Used by an external device to request control of the memory interface. When $\overline{\text{BR}}$ is asserted, the processor halts execution after completion of the current cycle, places all memory data, addresses, selects, and strobes in a high-impedance state, and asserts $\overline{\text{BG}}$. The processor continues normal operation when $\overline{\text{BR}}$ is released.
$\overline{\text{BG}}$	O	Bus Grant. Acknowledges a bus request ($\overline{\text{BR}}$), indicating that the external device may take control of the memory interface. $\overline{\text{BG}}$ is asserted (held low) until $\overline{\text{BR}}$ is released.
TIMEXP	O	Timer Expired. Asserted for four cycles when the value of TCOUNT is decremented to zero.
RCOMP		Compensation Resistor input. Controls compensated output buffers. Connect RCOMP through a 1.8 kΩ ± 15% resistor to EVDD. Use of a capacitor (approximately 100 pF), placed in parallel with the 1.8 kΩ resistor is recommended.
EVDD	P	Power supply (for output drivers), nominally +5 V dc (10 pins).
EGND	G	Power supply return (for output drivers); (16 pins).
IVDD	P	Power supply (for internal circuitry), nominally +5 V dc (4 pins).
IGND	G	Power supply return (for internal circuitry); (7 pins).
TCK	I	Test Clock. Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select. Used to control the test state machine. TMS has a 20 kΩ internal pullup resistor.
TDI	I/S	Test Data Input. Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pullup resistor.
TDO	O	Test Data Output. Serial scan output of the boundary scan path.
$\overline{\text{TRST}}$	I/A	Test Reset. Resets the test state machine. $\overline{\text{TRST}}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-21020. $\overline{\text{TRST}}$ has a 20 kΩ internal pullup resistor.
NC		No Connect. No Connects are reserved pins that must be left open and unconnected.

INSTRUCTION SET SUMMARY

The ADSP-21020 instruction set provides a wide variety of programming capabilities. Every instruction assembles into a single word and can execute in a single processor cycle. Multifunction instructions enable simultaneous multiplier and ALU operations, as well as computations executed in parallel with data transfers. The addressing power of the ADSP-21020 gives you flexibility in moving data both internally and externally. The ADSP-21020 assembly language uses an algebraic syntax for ease of coding and readability.

The instruction types are grouped into four categories:

Compute and Move or Modify
Program Flow Control
Immediate Move
Miscellaneous

The instruction types are numbered; there are 22 types. Some instructions have more than one syntactical form; for example, Instruction 4 has four distinct forms. The instruction number itself has no bearing on programming, but corresponds to the opcode recognized by the ADSP-21020 device.

Because of the width and orthogonality of the instruction word, there are many possible instructions. For example, the ALU supports 21 fixed-point operations and 24 floating-point operations; each of these operations can be the compute portion of an instruction.

The following pages provide an overview and summary of the ADSP-21020 instruction set. For complete information, see the *ADSP-21020 User's Manual*. For additional reference information, see the *ADSP-21020 Programmer's Quick Reference*.

This section also contains several reference tables for using the instruction set.

- Table I describes the notation and abbreviations used.
- Table II lists all condition and termination code mnemonics.
- Table III lists all register mnemonics.
- Tables IV through VII list the syntax for all compute (ALU, multiplier, shifter or multifunction) operations.
- Table VIII lists interrupts and their vector addresses.

COMPUTE AND MOVE OR MODIFY INSTRUCTIONS

1. *compute*, | DM(Ia, Mb) = dreg1 | dreg1 = DM(Ia, Mb) | , | PM(Ic, Md) = dreg2 | dreg2 = PM(Ic, Md) | ;

2. *IF condition* compute ;

3a. *IF condition* *compute*, | DM(Ia, Mb) | PM(Ic, Md) | = ureg ;

3b. *IF condition* *compute*, | DM(Mb, Ia) | PM(Md, Ic) | = ureg ;

3c. *IF condition* *compute*, ureg = | DM(Ia, Mb) | PM(Ic, Md) | ;

3d. *IF condition* *compute*, ureg = | DM(Mb, Ia) | PM(Md, Ic) | ;

4a. *IF condition* *compute*, | DM(Ia, <data6>) | PM(Ic, <data6>) | = dreg ;

4b. *IF condition* *compute*, | DM(<data6>, Ia) | PM(<data6>, Ic) | = dreg ;

4c. *IF condition* *compute*, dreg = | DM(Ia, <data6>) | PM(Ic, <data6>) | ;

4d. *IF condition* *compute*, dreg = | DM(<data6>, Ia) | PM(<data6>, Ic) | ;

5. *IF condition* *compute*, ureg1 = ureg2 ;

6a. *IF condition* shiftimm, | *DM(Ia, Mb)* | *PM(Ic, Md)* | = *dreg* ;

6b. *IF condition* shiftimm, *dreg* = | *DM(Ia, Mb)* | *PM(Ic, Md)* | ;

7. *IF condition* *compute*, MODIFY | (Ia, Mb) | (Ic, Md) | ;

PROGRAM FLOW CONTROL INSTRUCTIONS

8. *IF condition* | JUMP | CALL | | <addr24> | (PC, <reladdr24>) | (| *DB* | *LA* | *DB, LA* |) ;

9. *IF condition* | JUMP | CALL | | (Md, Ic) | (PC, <reladdr6>) | (| *DB* | *LA* | *DB, LA* |) , *compute* ;

11. *IF condition* | RTS | RTI | (| *DB* | *LA* | *DB, LA* |) , *compute* ;

12. LCNTR = | <data16> | ureg | , DO | <addr24> | (<PC, <reladdr24>) | UNTIL LCE ;

13. DO | <addr24> | (PC, <reladdr24>) | UNTIL termination ;

(DB) Delayed branch
(LA) Loop abort (pop loop PC stacks on branch)

IMMEDIATE MOVE INSTRUCTIONS

14a. | DM(<addr32>) | = ureg ;
| PM(<addr24>) |

14b. ureg = | DM(<addr32>) | ;
| PM(<addr24>) |

15a. | DM(<data32>, Ia) | = ureg ;
| PM(<data24>, Ic) |

15b. ureg = | DM(<data32>, Ia) | ;
| PM(<data24>, Ic) |

16. | DM(Ia, Mb) | = <data32>;
| PM(Ic, Md) |

17. ureg = <data32>;

MISCELLANEOUS INSTRUCTIONS

18. BIT | SET | sreg <data32>;
| CLR |
| TGL |
| TST |
| XOR |

19a. MODIFY | (Ia, <data32>) | ;
| (Ic, <data32>) |

19b. BITREV (Ia, <data32>) ;

20. | *PUSH* | *LOOP* , | *PUSH* | *STS* ;
| *POP* | | POP |

21. NOP ;

22. IDLE ;

Table I. Syntax Notation Conventions

Notation	Meaning
UPPERCASE	Explicit syntax—assembler keyword (notation only; assembler is not case-sensitive and lowercase is the preferred programming convention)
;	Instruction terminator
,	Separates parallel operations in an instruction
italics	Optional part of instruction
| between lines |	List of options (choose one)
<data*n*>	*n*-bit immediate data value
<addr*n*>	*n*-bit immediate address value
<reladdr*n*>	*n*-bit immediate PC-relative address value
compute	ALU, multiplier, shifter or multifunction operation (from Tables IV–VII)
shiftimm	Shifter immediate operation (from Table VI)
condition	Status condition (from Table II)
termination	Termination condition (from Table II)
ureg	Universal register (from Table III)
sreg	System register (from Table III)
dreg	R15-R0, F15-F0; register file location
Ia	I7-I0; DAG1 index register
Mb	M7-M0; DAG1 modify register
Ic	I15-I8; DAG2 index register
Md	M15-M8; DAG2 modify register

Table II. Condition and Termination Codes

Name	Description
eq	ALU equal to zero
ne	ALU not equal to zero
ge	ALU greater than or equal to zero
lt	ALU less than zero
le	ALU less than or equal to zero
gt	ALU greater than zero
ac	ALU carry
not ac	Not ALU carry
av	ALU overflow
not av	Not ALU overflow
mv	Multiplier overflow
not mv	Not multiplier overflow
ms	Multiplier sign
not ms	Not multiplier sign
sv	Shifter overflow
not sv	Not shifter overflow
sz	Shifter zero
not sz	Not shifter zero
flag0_in	Flag 0
not flag0_in	Not Flag 0
flag1_in	Flag 1
not flag1_in	Not Flag 1
flag2_in	Flag 2
not flag2_in	Not Flag 2
flag3_in	Flag 3
not flag3_in	Not Flag 3
tf	Bit test flag
not tf	Not bit test flag
lce	Loop counter expired (DO UNTIL)
not lce	Loop counter not expired (IF)
forever	Always False (DO UNTIL)
true	Always True (IF)

In a conditional instruction, the execution of the entire instruction is based on the specified condition.

Table III. Universal Registers

Name	Function
Register File	
R15–R0	Register file locations
Program Sequencer	
PC*	Program counter; address of instruction currently executing
PCSTK	Top of PC stack
PCSTKP	PC stack pointer
FADDR*	Fetch address
DADDR*	Decode address
LADDR	Loop termination address, code; top of loop address stack
CURLCNTR	Current loop counter; top of loop count stack
LCNTR	Loop count for next nested counter-controlled loop
Data Address Generators	
I7–I0	DAG1 index registers
M7–M0	DAG1 modify registers
L7–L0	DAG1 length registers
B7–B0	DAG1 base registers
I15–I8	DAG2 index registers
M15–M8	DAG2 modify registers
L15–L8	DAG2 length registers
B15–B8	DAG2 base registers
Bus Exchange	
PX1	PMD-DMD bus exchange 1 (16 bits)
PX2	PMD-DMD bus exchange 2 (32 bits)
PX	48-bit PX1 and PX2 combination
Timer	
TPERIOD	Timer period
TCOUNT	Timer counter
Memory Interface	
DMWAIT	Wait state and page size control for data memory
DMBANK1	Data memory bank 1 upper boundary
DMBANK2	Data memory bank 2 upper boundary
DMBANK3	Data memory bank 3 upper boundary
DMADR*	Copy of last data memory address
PMWAIT	Wait state and page size control for program memory
PMBANK1	Program memory bank 1 upper boundary
PMADR*	Copy of last program memory address
System Registers	
MODE1	Mode control bits for bit-reverse, alternate registers, interrupt nesting and enable, ALU saturation, floating-point rounding mode and boundary
MODE2	Mode control bits for interrupt sensitivity, cache disable and freeze, timer enable, and I/O flag configuration
IRPTL	Interrupt latch
IMASK	Interrupt mask
IMASKP	Interrupt mask pointer (for nesting)
ASTAT	Arithmetic status flags, bit test, I/O flag values, and compare accumulator
STKY	Sticky arithmetic status flags, circular buffer overflow flags, stack status flags (not sticky)
USTAT1	User status register 1
USTAT2	User status register 2

*read-only
Refer to User's Manual for bit-level definitions of each register.

Table IV. ALU Compute Operations

Fixed-Point	Floating-Point
Rn = Rx + Ry	Fn = Fx + Fy
Rn = Rx − Ry	Fn = Fx − Fy
Rn = Rx + Ry, Rm = Rx − Ry	Fn = Fx + Fy, Fm = Fx − Fy
Rn = Rx + Ry + CI	Fn = ABS (Fx + Fy)
Rn = Rx − Ry + CI − 1	Fn = ABS (Fx − Fy)
Rn = (Rx + Ry)/2	Fn = (Fx + Fy)/2
COMP(Rx, Ry)	COMP(Fx, Fy)
Rn = −Rx	Fn = −Fx
Rn = ABS Rx	Fn = ABS Fx
Rn = PASS Rx	Fn = PASS Fx
Rn = MIN(Rx, Ry)	Fn = MIN(Fx, Fy)
Rn = MAX(Rx, Ry)	Fn = MAX(Fx, Fy)
Rn = CLIP Rx BY Ry	Fn = CLIP Fx BY Fy
Rn = Rx + CI	Fn = RND Fx
Rn = Rx + CI − 1	Fn = SCALB Fx BY Ry
Rn = Rx + 1	Rn = MANT Fx
Rn = Rx − 1	Rn = LOGB Fx
Rn = Rx AND Ry	Rn = FIX Fx BY Ry
Rn = Rx OR Ry	Rn = FIX Fx
Rn = Rx XOR Ry	Fn = FLOAT Rx BY Ry
Rn = NOT Rx	Fn = FLOAT Rx
	Fn = RECIPS Fx
	Fn = RSQRTS Fx
	Fn = Fx COPYSIGN Fy

Rn, Rx, Ry R15–R0; register file location, fixed-point
Fn, Fx, Fy F15–F0; register file location, floating point

2

Table V. Multiplier Compute Operations

Rn / MRF / MRB = Rx * Ry (S/U, S/U, F/I/FR)	Fn = Fx * Fy
Rn / MRF / MRB = MRF / MRB + Rx * Ry (S/U, S/U, F/I/FR)	Rn / MRF / MRB = MRF / MRB − Rx * Ry (S/U, S/U, F/I/FR)
Rn / MRF / MRB = SAT MRF / MRB (SI/UI/SF/UF)	Rn / MRF / MRB = RND MRF / MRB (SF/UF)
MRF / MRB = 0	
MRxF / MRxB = Rn	Rn = MRxF / MRxB

Rn, Rx, Ry R15–R0; register file location, fixed-point
Fn, Fx, Fy F15–F0; register file location, floating-point
MRxF MR2F, MR1F; MR0F; multiplier result accumulators, foreground
MRxB MR2B, MR1B, MR0B; multiplier result accumulators, background

(x-input, y-input, data format, rounding)

S Signed input
U Unsigned input
I Integer input(s)
F Fractional input(s)
FR Fractional inputs, Rounded output

(SF) Default format for 1-input operations
(SSF) Default format for 2-input operations

Table VI. Shifter and Shifter Immediate Compute Operations

Shifter	Shifter Immediate
Rn = LSHIFT Rx BY Ry	Rn = LSHIFT Rx BY<data8>
Rn = Rn OR LSHIFT Rx BY Ry	Rn = Rn OR LSHIFT Rx BY<data8>
Rn = ASHIFT Rx BY Ry	Rn = ASHIFT Rx BY<data8>
Rn = Rn OR ASHIFT Rx BY Ry	Rn = Rn OR ASHIFT Rx BY<data8>
Rn = ROT Rx BY RY	Rn = ROT Rx BY<data8>
Rn = BCLR Rx BY Ry	Rn = BCLR Rx BY<data8>
Rn = BSET Rx BY Ry	Rn = BSET Rx BY<data8>
Rn = BTGL Rx BY Ry	Rn = BTGL Rx BY<data8>
BTST Rx BY Ry	BTST Rx BY<data8>
Rn = FDEP Rx BY Ry	Rn = FDEP Rx BY <bit6>: <len6>
Rn = Rn OR FDEP Rx BY Ry	Rn = Rn OR FDEP Rx BY <bit6>:<len6>
Rn = FDEP Rx BY Ry (SE)	Rn = FDEP Rx BY <bit6>:<len6> (SE)
Rn = Rn OR FDEP Rx BY Ry (SE)	Rn = Rn OR FDEP Rx BY <bit6>:<len6> (SE)
Rn = FEXT Rx BY Ry	Rn = FEXT Rx BY <bit6>:<len6>
Rn = FEXT Rx BY Ry (SE)	Rn = FEXT Rx BY <bit6>:<lcn6> (SE)
Rn = EXP Rx	
Rn = EXP Rx (EX)	
Rn = LEFTZ Rx	
Rn = LEFTO Rx	

Rn, Rx, Ry R15–R0; register file location, fixed-point
<bit6>:<len6> 6-bit immediate bit position and length values (for shifter immediate operations)

Table VII. Multifunction Compute Operations

Fixed-Point

Rm=R3-0 * R7-4 (SSFR), Ra=R11-8 + R15-12
Rm=R3-0 * R7-4 (SSFR), Ra=R11-8 − R15-12
Rm=R3-0 * R7-4 (SSFR), Ra=(R11-8 + R15-12)/2
MRF=MRF + R3-0 * R7-4 (SSF), Ra=R11-8 + R15-12
MRF=MRF + R3-0 * R7-4 (SSF), Ra=R11-8 − R15-12
MRF=MRF + R3-0 * R7-4 (SSF), Ra=(R11-8 + R15-12)/2
Rm=MRF + R3-0 * R7-4 (SSFR), Ra=R11-8 + R15-12
Rm=MRF + R3-0 * R7-4 (SSFR), Ra=R11-8 − R15-12
Rm=MRF + R3-0 * R7-4 (SSFR), Ra=(R11-8 + R15-12)/2
MRF=MRF − R3-0 * R7-4 (SSF), Ra=R11-8 + R15-12
MRF=MRF − R3-0 * R7-4 (SSF), Ra=R11-8 − R15-12
MRF=MRF − R3-0 * R7-4 (SSF), Ra=(R11-8 + R15-12)/2
Rm=MRF − R3-0 * R7-4 (SSFR), Ra=R11-8 + R15-12
Rm=MRF − R3-0 * R7-4 (SSFR), Ra=R11-8 − R15-12
Rm=MRF − R3-0 * R7-4 (SSFR), Ra=(R11-8 + R15-12)/2
Rm=R3-0 * R7-4 (SSFR), Ra=R11-8 + R15-12,
Rs=R11-8 − R15-12

Floating-Point

Fm=F3-0 * F7-4, Fa=F11-8 + F15-12
Fm=F3-0 * F7-4, Fa=F11-8 − F15-12
Fm=F3-0 * F7-4, Fa=FLOAT R11-8 by R15-12
Fm=F3-0 * F7-4, Fa=FIX R11-8 by R15-12
Fm=F3-0 * F7-4, Fa=(F11-8 + F15-12)/2
Fm=F3-0 * F7-4, Fa=ABS F11-8
Fm=F3-0 * F7-4, Fa=MAX (F11-8, F15-12)
Fm=F3-0 * F7-4, Fa=MIN (F11-8, F15-12)
Fm=F3-0 * F7-4, Fa=F11-8 + F15-12,
Fs=F11-8 − F15-12

Ra, Rm	Any register file location (fixed-point)
R3-0	R3, R2, R1, R0
R7-4	R7, R6, R5, R4
R11-8	R11, R10, R9, R8
R15-12	R15, R14, R13, R12
Fa, Fm	Any register file location (floating-point)
F3-0	F3, F2, F1, F0
F7-4	F7, F6, F5, F4
F11-8	F11, F10, F9, F8
F15-12	F15, F14, F13, F12
(SSF)	X-input signed, Y-input signed, fractional inputs
(SSFR)	X-input signed, Y-input signed, fractional inputs, rounded output

Table VIII. Interrupt Vector Addresses and Priorities

No.	Vector Address (Hex)	Function
0	0x00	Reserved
1*	0x08	Reset
2	0x10	Reserved
3	0x18	Status stack or loop stack overflow or PC stack full
4	0x20	Timer=0 (high priority option)
5	0x28	$\overline{IRQ3}$ asserted
6	0x30	$\overline{IRQ2}$ asserted
7	0x38	$\overline{IRQ1}$ asserted
8	0x40	$\overline{IRQ0}$ asserted
9	0x48	Reserved
10	0x50	Reserved
11	0x58	DAG 1 circular buffer 7 overflow
12	0x60	DAG 2 circular buffer 15 overflow
13	0x68	Reserved
14	0x70	Timer=0 (low priority option)
15	0x78	Fixed-point overflow
16	0x80	Floating-point overflow
17	0x88	Floating-point underflow
18	0x90	Floating-point invalid operation
19–23	0x98-0xB8	Reserved
24–31	0xC0–OxF8	User software interrupts

*Nonmaskable

ADSP-21020—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	T Grade Min	T Grade Max	Unit
V_{DD}	Supply Voltage	4.50	5.50	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	−55	+125	°C

Refer to Environmental Conditions for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	Hi-Level Input Voltage[1]	V_{DD} = max	2.0		V
V_{IHCR}	Hi-Level Input Voltage[2, 12]	V_{DD} = max	3.0		V
V_{IL}	Lo-Level Input Voltage[1, 12]	V_{DD} = min		0.8	V
V_{ILC}	Lo-Level Input Voltage[2]	V_{DD} = max		0.6	V
V_{OH}	Hi-Level Output Voltage[3, 11]	V_{DD} = min, I_{OH} = −1.0 mA	2.4		V
V_{OL}	Lo-Level Output Voltage[3, 11]	V_{DD} = min, I_{OL} = 4.0 mA		0.4	V
I_{IH}	Hi-Level Input Current[4, 5]	V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{IL}	Lo-Level Input Current[4]	V_{DD} = max, V_{IN} = 0 V		10	μA
I_{ILT}	Lo-Level Input Current[5]	V_{DD} = max, V_{IN} = 0 V		350	μA
I_{OZH}	Tristate Leakage Current[6]	V_{DD} = max, V_{IN} = V_{DD} max		10	μA
I_{OZL}	Tristate Leakage Current[6]	V_{DD} = max, V_{IN} = 0 V		10	μA
I_{DDIN}	Supply Current (Internal)[7]	t_{CK} = 30–33 ns, V_{DD} = max, V_{IHCR} = 3.0 V, V_{IH} = 2.4 V, V_{IL} = V_{ILC} = 0.4 V		490	mA
I_{DDIDLE}	Supply Current (Idle)[8]	V_{DD} = max, V_{IN} = 0 V or V_{DD} max		150	mA
C_{IN}	Input Capacitance[9, 10]	f_{IN} = 1 MHz, T_{CASE} = 25°C, V_{IN} = 2.5 V		10	pF

NOTES
[1]Applies to: PMD47–0, PMACK, $\overline{\text{PMTS}}$, DMD39–0, DMACK, $\overline{\text{DMTS}}$, $\overline{\text{IRQ}}$3–0, FLAG3–0, $\overline{\text{BR}}$, TMS, TDI.
[2]Applies to: CLKIN, TCK.
[3]Applies to: PMA23–0, PMD47–0, $\overline{\text{PMS}}$1–0, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMPAGE, DMA31–0, DMD39–0, $\overline{\text{DMS}}$3–0, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$, DMPAGE, FLAG3–0, TIMEXP, $\overline{\text{BG}}$.
[4]Applies to: PMACK, $\overline{\text{PMTS}}$, DMACK, $\overline{\text{DMTS}}$, $\overline{\text{IRQ}}$3–0, $\overline{\text{BR}}$, CLKIN, $\overline{\text{RESET}}$, TCK.
[5]Applies to: TMS, TDI, $\overline{\text{TRST}}$.
[6]Applies to: PMA23–0, PMD47–0, $\overline{\text{PMS}}$1–0, $\overline{\text{PMRD}}$, $\overline{\text{PMWR}}$, PMPAGE, DMA31–0, DMD39–0, $\overline{\text{DMS}}$3–0, $\overline{\text{DMRD}}$, $\overline{\text{DMWR}}$, DMPAGE, FLAG3–0, TDO.
[7]Applies to IVDD pins. At t_{CK} = 30–33 ns, I_{DDIN} (typical) = 230 mA; at t_{CK} = 40 ns, I_{DDIN} (max) = 420 mA and I_{DDIN} (typical) = 200 mA; at t_{CK} = 50 ns, I_{DDIN} (max) = 370 mA and I_{DDIN} (typical) = 115 mA. See "Power Dissipation" for calculation of external (EVDD) supply current for total supply current.
[8]Applies to IVDD pins. Idle refers to ADSP-21020 state of operation during execution of the IDLE instruction.
[9]Guaranteed but not tested.
[10]Applies to all signal pins.
[11]Although specified for TTL outputs, all ADSP-21020 outputs are CMOS-compatible and will drive to V_{DD} and GND assuming no dc loads.
[12]Applies to $\overline{\text{RESET}}$, $\overline{\text{TRST}}$.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} + 0.3 V
Load Capacitance . . . . . 200 pF
Operating Temperature Range (Ambient) . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (10 seconds) CPGA . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The ADSP-21020 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per method 3015 of MIL-STD-883, the ADSP-21020 has been classified as a Class 3 device, with the ability to withstand up to 4000 V ESD.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed. For further information on ESD precautions, refer to *Analog Devices' ESD Prevention Manual.*

TIMING PARAMETERS

General Notes

See Figure 15 on page 24 for voltage reference levels. Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive other specifications.

Clock Signal

		K/B/T Grade		K/B/T Grade		B/T Grade		K Grade		
		20 MHz		25 MHz		30 MHz		33.3 MHz		
Parameter		Min	Max	Min	Max	Min	Max	Min	Max	Unit
Timing Requirement:										
t_{CK}	CLKIN Period	50	150	40	150	33	150	30	150	ns
t_{CKH}	CLKIN Width High	10		10		10		10		ns
t_{CKL}	CLKIN Width Low	10		10		10		10		ns

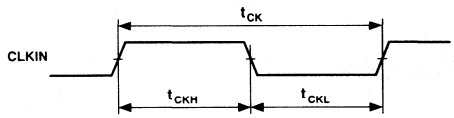


Figure 3. Clock

Reset

	K/B/T Grade		K/B/T Grade		B/T Grade		K Grade				
	20 MHz		25 MHz		30 MHz		33.3 MHz		Frequency Dependency*		
Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Timing Requirement:											
t_{WRST}[1] RESET Width Low	200		160		132		120		$4t_{CK}$		ns
t_{SRST}[2] RESET Setup before CLKIN High	29	50	24	40	21	33	19	30	29 + DT/2	30	ns

NOTES

*DT = t_{CK} – 50 ns

[1]Applies after the power-up sequence is complete. At power up, the Internal Phase Locked Loop requires no more than 1000 CLKIN cycles while RESET is low, assuming stable V_{DD} and CLKIN (not including clock oscillator start-up time).

[2]Specification only applies in cases where multiple ADSP-21020 processors are required to execute in program counter lock-step (all processors start execution at location 8 in the same cycle). See the Hardware Configuration chapter of the *ADSP-21020 User's Manual* for reset sequence information.

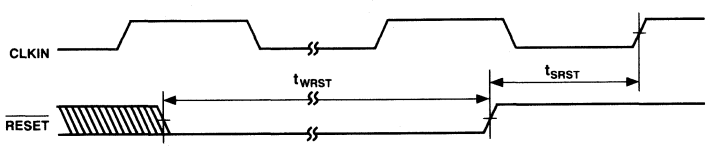


Figure 4. Reset

Interrupts

Parameter	K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Timing Requirement:											
t_{SIR} $\overline{IRQ3-0}$ Setup before CLKIN High	38		31		25		23		38 + 3DT/4		ns
t_{HIR} $\overline{IRQ3-0}$ Hold after CLKIN High	0		0		0		0				ns
t_{IPW} $\overline{IRQ3-0}$ Pulse Width	55		45		38		35		t_{CK} + 5		ns

NOTE
*DT = t_{CK} − 50 ns
Meeting setup and hold guarantees interrupts will be latched in that cycle. Meeting the pulse width is not necessary if the setup and hold is met. Likewise, meeting the setup and hold is not necessary if the pulse width is met. See the Hardware Configuration chapter of the *ADSP-21020 User's Manual* for interrupt servicing information.

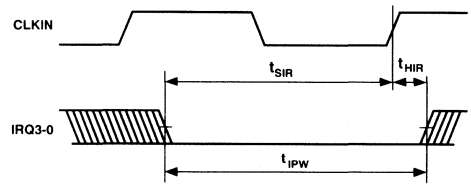


Figure 5. Interrupts

Timer

Parameter	K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Switching Characteristic:											
t_{DTEX} CLKIN High to TIMEXP		24		24		24		24			ns

NOTE
*DT − t_{CK} − 50 ns

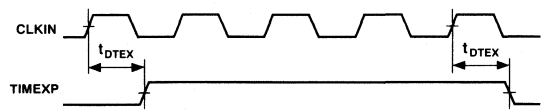


Figure 6. TIMEXP

Flags

Parameter		K/B/T Grade 20 MHz Min	K/B/T Grade 20 MHz Max	K/B/T Grade 25 MHz Min	K/B/T Grade 25 MHz Max	B/T Grade 30 MHz Min	B/T Grade 30 MHz Max	K Grade 33.3 MHz Min	K Grade 33.3 MHz Max	Frequency Dependency* Min	Frequency Dependency* Max	Unit
Timing Requirement:[1]												
t_{SFI}	FLAG3-0_{IN} Setup before CLKIN High	19		16		14		13		19+5DT/16		ns
t_{HFI}	FLAG3-0_{IN} Hold after CLKIN High	0		0		0		0				ns
t_{DWRFI}	FLAG3-0_{IN} Delay from $\overline{xRD}$, $\overline{xWR}$ Low		12		8		5		3		12+7DT/16	ns
t_{HFIWR}	FLAG3-0_{IN} Hold after $\overline{xRD}$, $\overline{xWR}$ Deasserted	0		0		0		0				ns
Switching Characteristic:												
t_{DFO}	FLAG3-0_{OUT} Delay from CLKIN High		24		24		24		24			ns
t_{HFO}	FLAG3-0_{OUT} Hold after CLKIN High	5		5		5		5				ns
t_{DFOE}	CLKIN High to FLAG3-0_{OUT} Enable	1		1		1		1				ns
t_{DFOD}	CLKIN High to FLAG3-0_{OUT} Disable		24		24		24		24			ns

NOTES
*DT = t_{CK} – 50 ns
[1]Flag inputs meeting these setup and hold times will affect conditional operations in the next instruction cycle. See the Hardware Configuration chapter of the *ADSP-21020 User's Manual* for additional flag servicing information.
x = PM or DM.

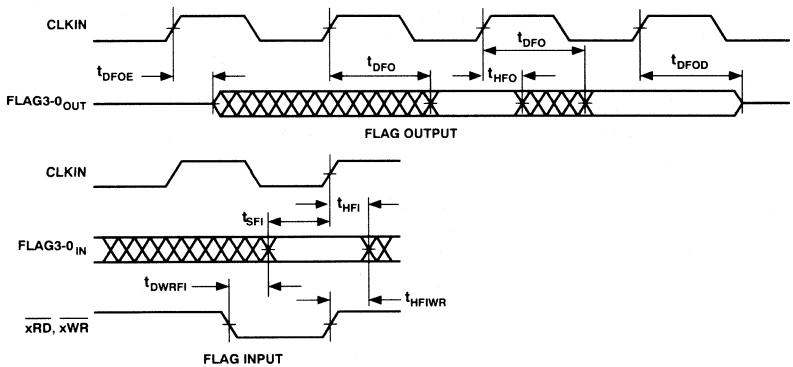


Figure 7. Flags

Bus Request/Bus Grant

Parameter		K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Timing Requirement:												
t_{HBR}	$\overline{BR}$ Hold after CLKIN High	0		0		0		0				ns
t_{SBR}	$\overline{BR}$ Setup before CLKIN High	18		15		13		12		18 + 5DT/16		ns
Switching Characteristic:												
t_{DMDBGL}	Memory Interface Disable to $\overline{BG}$ Low	−2		−2		−2		−2				ns
t_{DME}	CLKIN High to Memory Interface Enable	25		20		16		15		25 + DT/2		ns
t_{DBGL}	CLKIN High to $\overline{BG}$ Low		22		22		22		22			ns
t_{DBGH}	CLKIN High to $\overline{BG}$ High		22		22		22		22			ns

NOTES
*DT = t_{CK} − 50 ns.
Memory Interface = PMA23-0, PMD47-0, $\overline{PMS1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA31-0, DMD39-0, $\overline{DMS3-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE.
Buses are not granted until completion of current memory access.
See the Memory Interface chapter of the *ADSP-21020 User's Manual* for $\overline{BG}$, $\overline{BR}$ cycle relationships.

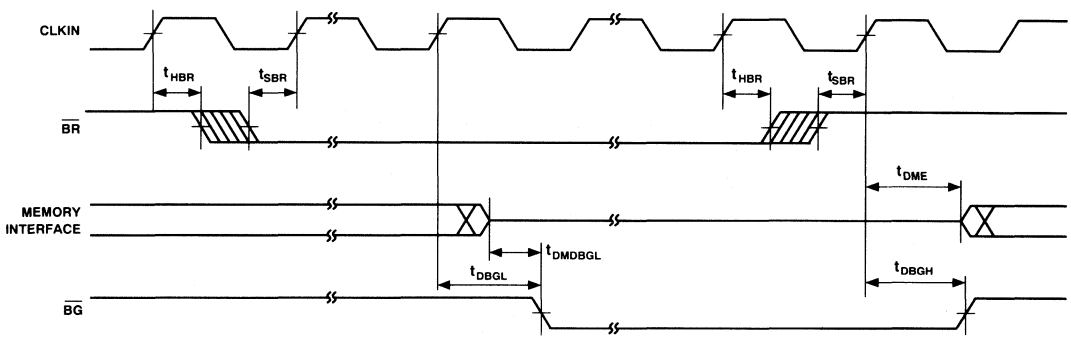


Figure 8. Bus Request/Bus Grant

External Memory Three-State Control

Parameter		K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Timing Requirement:												
t_{STS}	$\overline{xTS}$, Setup before CLKIN High	14	50	12	40	10	33	9	30	14 + DT/4	t_{CK}	ns
t_{DADTS}	$\overline{xTS}$ Delay after Address, Select		28		19		13		10		28 + 7DT/8	ns
t_{DSTS}	$\overline{xTS}$ Delay after $\overline{XRD}$, $\overline{XWR}$ Low		16		11		7		6		16 + DT/2	ns
Switching Characteristic:												
t_{DTSD}	Memory Interface Disable before CLKIN High	0		−2		−4		−5		DT/4		ns
t_{DTSAE}	$\overline{xTS}$ High to Address, Select Enable	0		0		0		0				ns

NOTES
*DT = t_{CK} − 50 ns.
$\overline{xTS}$ should only be asserted (low) during an active memory access cycle.
Memory Interface = PMA23-0, PMD47-0, $\overline{PMS1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMPAGE, DMA31-0, DMD39-0, $\overline{DMS3-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMPAGE.
Address = PMA23-0, DMA31-0. Select = $\overline{PMS1-0}$, $\overline{DMS3-0}$.
x = PM or DM.

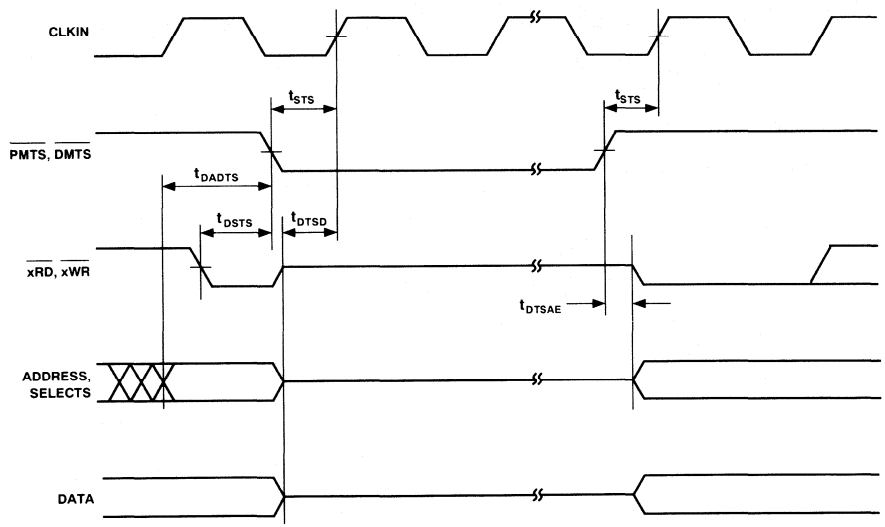


Figure 9. External Memory Three-State Control

Memory Read

Parameter		K/B/T Grade 20 MHz Min	K/B/T Grade 20 MHz Max	K/B/T Grade 25 MHz Min	K/B/T Grade 25 MHz Max	B/T Grade 30 MHz Min	B/T Grade 30 MHz Max	K Grade 33.3 MHz Min	K Grade 33.3 MHz Max	Frequency Dependence* Min	Frequency Dependence* Max	Unit
Timing Requirement:												
t_{DAD}	Address, Select to Data Valid		37		27		20		17		37 + DT	ns
t_{DRLD}	$\overline{xRD}$ Low to Data Valid		24		18		13		11		24 + 5DT/8	ns
t_{HDA}	Data Hold from Address, Select	0		0		0		0				ns
t_{HDRH}	Data Hold from $\overline{xRD}$ High	−1		−1		−1		−1				ns
t_{DAAK}	xACK Delay from Address		27		18		12		9		27 + 7DT/8	ns
t_{DRAK}	xACK Delay from $\overline{xRD}$ Low		15		10		6		5		15 + DT/2	ns
t_{SAK}	xACK Setup before CLKIN High	14		12		10		9		14 + DT/4		ns
t_{HAK}	xACK Hold after CLKIN High	0		0		0		0				ns
Switching Characteristic:												
t_{DARL}	Address, Select to $\overline{xRD}$ Low	8		4		2		0		8 + 3DT/8		ns
t_{DAP}	xPAGE Delay from Address, Select		1		1		1		1			ns
t_{DCKRL}	CLKIN High to $\overline{xRD}$ Low	16	26	13	24	12	22	11	21	16 + DT/4	26 + DT/4	ns
t_{RW}	$\overline{xRD}$ Pulse Width	26		20		15		13		26 + 5DT/8		ns
t_{RWR}	$\overline{xRD}$ High to $\overline{xRD}$, $\overline{xWR}$ Low	17		13		11		9		17 + 3DT/8		ns

NOTES
*DT = t_{CK} − 50 ns
x = PM or DM; Address = PMA23-0, DMA31-0; Data = PMD47-0, DMD39-0; Select = $\overline{PMS1-0}$, $\overline{DMS3-0}$.

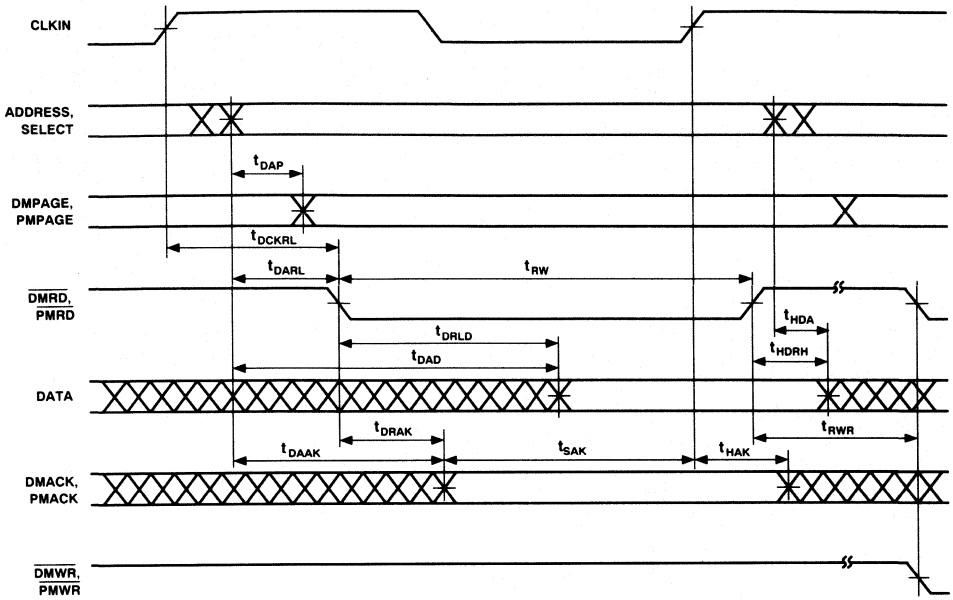


Figure 10. Memory Read

Memory Write

Parameter		K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Timing Requirement:							12					
t_{DAAK}	xACK Delay from Address, Select		27		18		6		9		27 + 7DT/8	ns
t_{DWAK}	xACK Delay from $\overline{xWR}$ Low		15		10	10			5		15 + DT/2	ns
t_{SAK}	xACK Setup before CLKIN High	14		12		0		9		14 + DT/4		ns
t_{HAK}	xACK Hold after CLKIN High	0		0				0				ns
Switching Characteristic:												
t_{DAWH}	Address, Select to $\overline{xWR}$ Deasserted	37		28		21		18		37 + 15DT/16		ns
t_{DAWL}	Address, Select to $\overline{xWR}$ Low	11		7		5		3		11 + 3DT/8		ns
t_{WW}	$\overline{xWR}$ Pulse Width	26		20		16		15		26 + 9DT/16		ns
t_{DDWH}	Data Setup before $\overline{xWR}$ High	23		18		14		13		23 + DT/2		ns
t_{DWHA}	Address, Select Hold after $\overline{xWR}$ Deasserted	1		0		0		0		1 + DT/16		ns
t_{HDWH}	Data Hold after $\overline{xWR}$ Deasserted[1]	0		−1		−1		−1		DT/16		ns
t_{DAP}	xPAGE Delay from Address, Select		1		1		1		1			ns
t_{DCKWL}	CLKIN High to $\overline{xWR}$ Low	16	26	13	24	12	22	11	21	16 + DT/4	26 + DT/4	ns
t_{WWR}	$\overline{xWR}$ High to $\overline{xWR}$ or $\overline{xRD}$ Low	17		13		10		8		17 + 7DT/16		ns
t_{DDWR}	Data Disable before $\overline{xWR}$ or $\overline{xRD}$ Low	13		9		7		5		13 + 3DT/8		ns
t_{WDE}	$\overline{xWR}$ Low to Data Enabled	0		−1		−1		−1		DT/16		ns

NOTES
*DT = t_C − 50 ns
[1]See "System Hold Time Calculation" in "Test Conditions" section for calculating hold times given capacitive and DC loads.
x = PM or DM; Address = PMA23-0, DMA31-0; Data = PMD47-0, DMD39-0; Select = $\overline{PMS1-0}$, $\overline{DMS3-0}$.

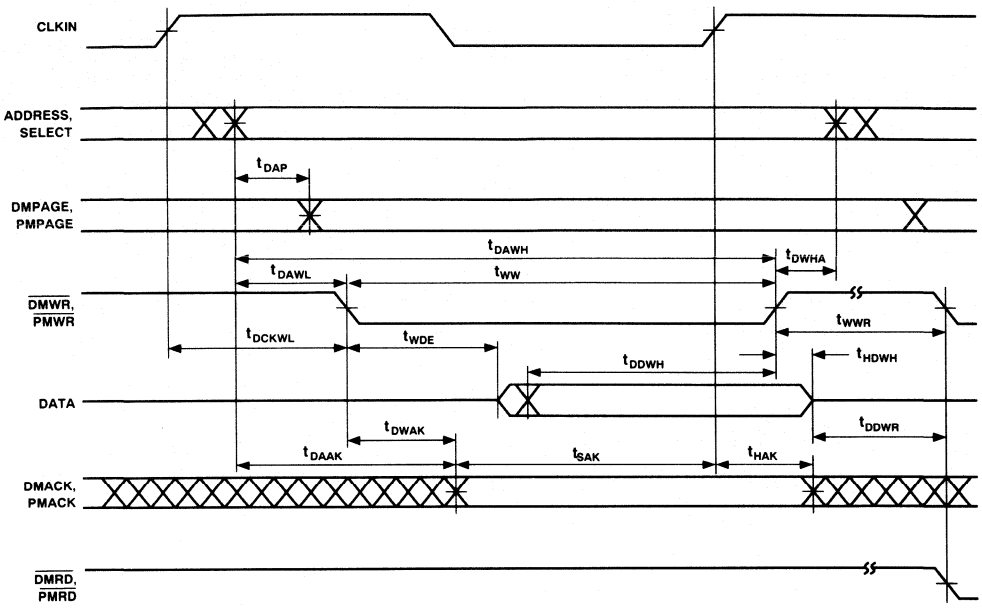


Figure 11. Memory Write

IEEE 1149.1 Test Access Port

Parameter		K/B/T Grade 20 MHz Min	Max	K/B/T Grade 25 MHz Min	Max	B/T Grade 30 MHz Min	Max	K Grade 33.3 MHz Min	Max	Frequency Dependency* Min	Max	Unit
Timing Requirement:												
t_{TCK}	TCK Period	50		40		33		30		t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5		5		5		5				ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		6		6		6				ns
t_{SSYS}	System Inputs Setup before TCK High	7		7		7		7				ns
t_{HSYS}	System Inputs Hold after TCK High	9		9		9		9				ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	200		160		132		120				ns
Switching Characteristic:												
t_{DTDO}	TDO Delay from TCK Low		15		15		15		15			ns
t_{DSYS}	System Outputs Delay from TCK Low		26		26		26		26			ns

NOTES
*DT = t_{CK} – 50 ns
System Inputs = PMD47-0, PMACK, $\overline{PMTS}$, DMD39-0, DMACK, $\overline{DMTS}$, CLKIN, $\overline{IRQ3-0}$, $\overline{RESET}$, FLAG3-0, $\overline{BR}$.
System Outputs = PMA23-0, $\overline{PMS1-0}$, $\overline{PMRD}$, $\overline{PMWR}$, PMD47-0, PMPAGE, DMA31-0, $\overline{DMS1-0}$, $\overline{DMRD}$, $\overline{DMWR}$, DMD39-0, DMPAGE, FLAG3-0, $\overline{BG}$, TIMEXP.
See the IEEE 1149.1 Test Access Port chapter of the *ADSP-21020 User's Manual* for further detail.

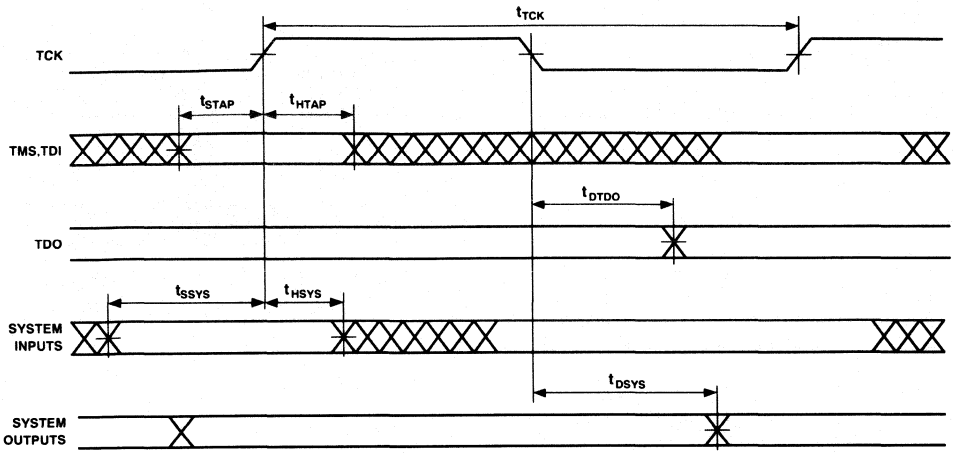


Figure 12. IEEE 1149.1 Test Access Port

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \, \Delta V}{I_L}$$

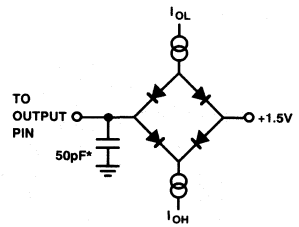
The output disable time (t_{DIS}) is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 13. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with ΔV equal to 0.5 V, and test loads C_L and I_L.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the above equation. Choose ΔV to be the difference between the ADSP-21020's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or three-state current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e. t_{HDWD} for the write cycle).



*AC TIMING SPECIFICATIONS ARE CALCULATED FOR 100pF DERATING ON THE FOLLOWING PINS: PMA23–0, PMS1–0, PMRD, PMWR, PMPAGE, DMA31–0, DMS3–0, DMRD, DMWR, DMPAGE

Figure 14. Equivalent Device Loading For AC Measurements (Includes All Fixtures)

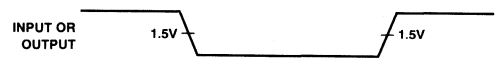


Figure 15. Voltage Reference Levels For AC Measurements (Except Output Enable/Disable)

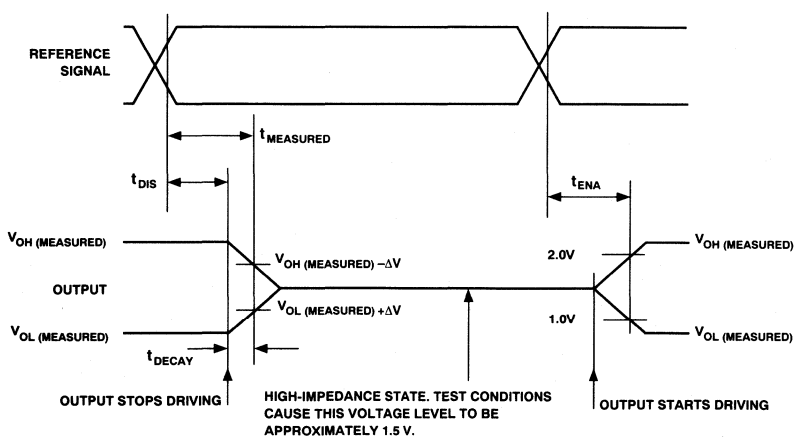
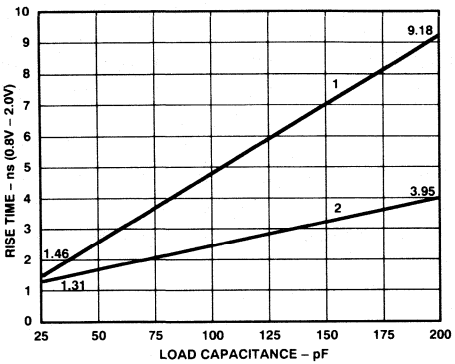


Figure 13. Output Enable/Disable

Capacitive Loading

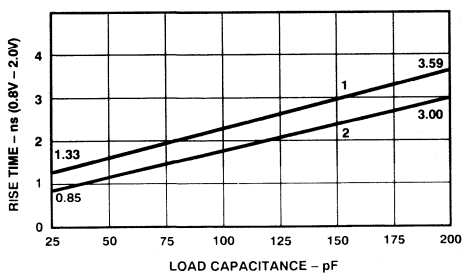
Output delays are based on standard capacitive loads: 100 pF on address, select, page and strobe pins, and 50 pF on all others (see Figure 14). For different loads, these timing parameters should be derated. See the Hardware Configuration chapter of the *ADSP-21020 User's Manual* for further information on derating of timing specifications.

Figures 16 and 17 show how the output rise time varies with capacitance. Figures 18 and 19 show how output delays vary with capacitance. Note that the graphs may not be linear outside the ranges shown.



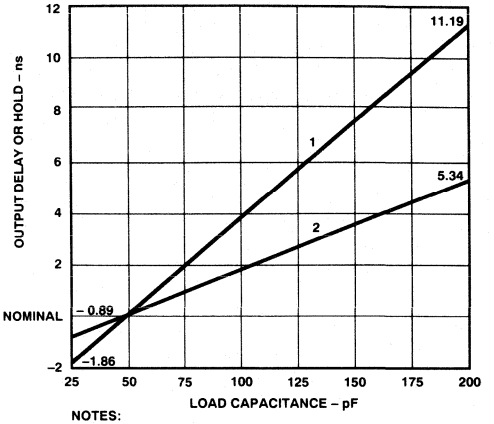
NOTES:
(1) OUTPUT PINS $\overline{BG}$, TIMEXP
(2) OUTPUT PINS PMD47–0, DMD39–0, FLAG3–0

Figure 16. Typical Output Rise Time vs. Load Capacitance (at Maximum Case Temperature)



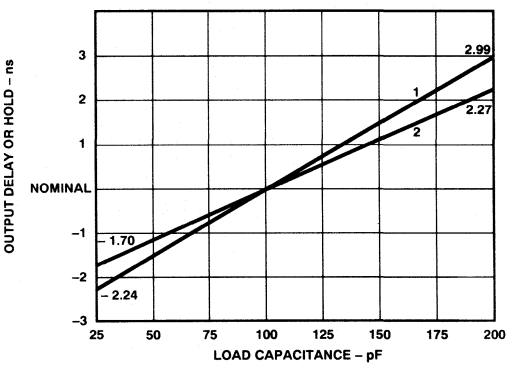
NOTES:
(1) OUTPUT PINS PMA23–0, $\overline{PMS1–0}$, PMPAGE, DMA31–0, $\overline{DMS3–0}$, DMPAGE, TDO
(2) OUTPUT PINS $\overline{PMRD}$, $\overline{PMWR}$, $\overline{DMRD}$, $\overline{DMWR}$

Figure 17. Typical Output Rise Time vs. Load Capacitance (at Maximum Case Temperature)



NOTES:
(1) OUTPUT PINS $\overline{BG}$, TIMEXP
(2) OUTPUT PINS PMD47–0, DMD39–0, FLAG3–0

Figure 18. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature)



NOTES:
(1) OUTPUT PINS PMA23–0, $\overline{PMS1–0}$, PMPAGE, DMA31–0, $\overline{DMS3–0}$, DMPAGE, TDO
(2) OUTPUT PINS $\overline{PMRD}$, $\overline{PMWR}$, $\overline{DMRD}$, $\overline{DMWR}$

Figure 19. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature)

ENVIRONMENTAL CONDITIONS

The ADSP-21020 is available in a Ceramic Pin Grid Array (CPGA). The package uses a cavity-down configuration which gives it favorable thermal characteristics. The top surface of the package contains a raised copper slug from which much of the die heat is dissipated. The slug provides a surface for mounting a heat sink (if required).

The commercial grade (K grade) ADSP-21020 is specified for operation at T_{AMB} of 0°C to +70°C. Maximum T_{CASE} (case temperature) can be calculated from the following equation:

$$T_{CASE} = T_{AMB} + (PD \times \theta_{CA})$$

where PD is power dissipation and θ_{CA} is the case-to-ambient thermal resistance. The value of PD depends on your application; the method for calculating PD is shown under "Power Dissipation" below. θ_{CA} varies with airflow and with the presence or absence of a heat sink. Table IX shows a range of θ_{CA} values.

Table IX. Maximum θ_{CA} for Various Airflow Values

Airflow (Linear ft./min.)	0	100	200	300
CPGA with No Heat Sink	12.8°C/W	9.2°C/W	6.6°C/W	5.5°C/W

NOTES
θ_{JC} is approximately 1°C/W.
Maximum recommended T_J is 130°C.
As per method 1012 MIL-STD-883. Ambient temperature: 25°C. Power: 3.5 W.

Power Dissipation

Total power dissipation has two components: one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data values involved. Internal power dissipation is calculated in the following way:

$$\mathbf{P_{INT} = I_{DDIN} \times V_{DD}}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

1) the number of output pins that switch during each cycle (O),
2) the maximum frequency at which they can switch (f),
3) their load capacitance (C), and
4) their voltage swing (V_{DD}).

It is calculated by:

$$\mathbf{P_{EXT} = O \times C \times V_{DD}^2 \times f}$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive high and low at a maximum rate of $1/(2t_{CK})$. The write strobes can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but 2 DM and 2 PM selects can switch on each cycle. If only one bank is accessed, no select line will switch.

Example:

Estimate P_{EXT} with the following assumptions:

- A system with one RAM bank each of PM (48 bits) and DM (32 bits).
- 32K × 8 RAM chips are used, each with a load of 10 pF.
- Single-precision mode is enabled so that only 32 data pins can switch at once.
- PM and DM writes occur every other cycle, with 50% of the pins switching.
- The instruction cycle rate is 20 MHz (t_{CK} = 50 ns) and V_{DD} = 5.0 V.

The P_{EXT} equation is calculated for each class of pins that can drive:

Pin Type	# Pins	% Switch	× C	× f	$\times V_{DD}^2$	P_{EXT}
PMA	15	50	68 pF	5 MHz	25 V	0.064 W
$\overline{\text{PMS}}$	2	0	68 pF	5 MHz	25 V	0.000 W
$\overline{\text{PMWR}}$	1	—	68 pF	10 MHz	25 V	0.017 W
PMD	32	50	18 pF	5 MHz	25 V	0.036 W
DMA	15	50	48 pF	5 MHz	25 V	0.045 W
$\overline{\text{DMS}}$	2	0	48 pF	5 MHz	25 V	0.000 W
$\overline{\text{DMWR}}$	1	—	48 pF	10 MHz	25 V	0.012 W
DMD	32	50	18 pF	5 MHz	25 V	0.036 W
					P_{EXT} =	0.210 W

A typical power consumption can now be calculated for this situation by adding a typical internal power dissipation:

$$\mathbf{P_{TOTAL} = P_{EXT} + (5\ V \times I_{DDIN}\ (typ)) = 0.210 + 1.15}$$
$$\mathbf{= 1.36\ W}$$

Note that the conditions causing a worst case P_{EXT} are different from those causing a worst case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Also note that it is not common for a program to have 100% or even 50% of the outputs switching simultaneously.

Power and Ground Guidelines

To achieve its fast cycle time, including instruction fetch, data access, and execution, the ADSP-21020 is designed with high speed drivers on all output pins. Large peak currents may pass through a circuit board's ground and power lines, especially when many output drivers are simultaneously charging or discharging their load capacitances. These transient currents can cause disturbances on the power and ground lines. To minimize these effects, the ADSP-21020 provides separate supply pins for its internal logic (IGND and IVDD) and for its external drivers (EGND and EVDD).

To reduce system noise at low temperatures when transistors switch fastest, the ADSP-21020 employs compensated output drivers. These drivers equalize slew rate over temperature extremes and process variations. A 1.8 kΩ resistor placed between the RCOMP pin and EVDD (+5 V) provides a reference for the compensated drivers. Use of a capacitor (approximately 100 pF), placed in parallel with the 1.8 kΩ resistor, is recommended.

All GND pins should have a low impedance path to ground. A ground plane is required in ADSP-21020 systems to reduce this impedance, minimizing noise.

The EVDD and IVDD pins should be bypassed to the ground plane using approximately 14 high-frequency capacitors (0.1 μF ceramic). Keep each capacitor's lead and trace length to the pins as short as possible. This low inductive path provides the ADSP-21020 with the peak currents required when its output drivers switch. The capacitors' ground leads should also be short and connect directly to the ground plane. This provides a low

impedance return path for the load capacitance of the ADSP-21020's output drivers.

If a V_{DD} plane is not used, the following recommendations apply. Traces from the +5 V supply to the 10 EVDD pins should be designed to satisfy the minimum V_{DD} specification while carrying average dc currents of [$I_{DDEX}/10 \times$ (number of EVDD pins per trace)]. I_{DDEX} is the calculated external supply current. A similar calculation should be made for the four IVDD pins using the I_{DDIN} specification. The traces connecting +5 V to the IVDD pins should be separate from those connecting to the EVDD pins.

A low frequency bypass capacitor (20 μF tantalum) located near the junction of the IVDD and EVDD traces is also recommended.

Target System Requirements For Use Of EZ-ICE Emulator

The ADSP-21020 EZ-ICE uses the IEEE 1149.1 JTAG test access port of the ADSP-21020 to monitor and control the target board processor during emulation. The EZ-ICE probe requires that CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, and GND be made accessible on the target system via a 12-pin connector (pin strip header) such as that shown in Figure 20. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation; you must add this connector to your target board design if you intend to use the ADSP-21020 EZ-ICE. Figure 21 shows the dimensions of the EZ-ICE probe; be sure to allow enough space in your system to fit the probe onto the 12-pin connector.

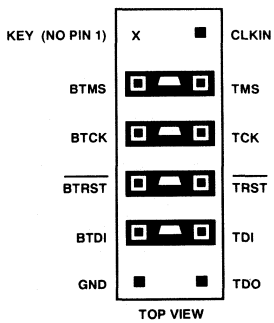


Figure 20. Target Board Connector for EZ-ICE Emulator (Jumpers In Place)

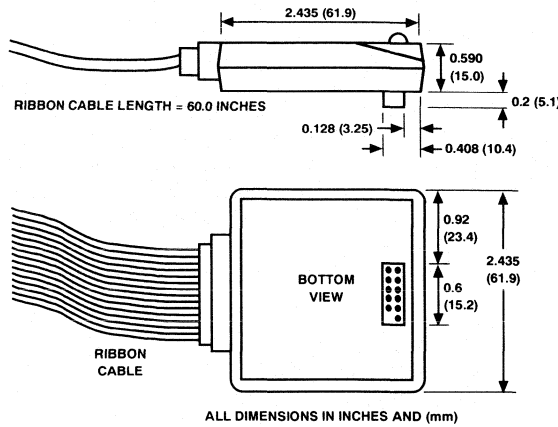


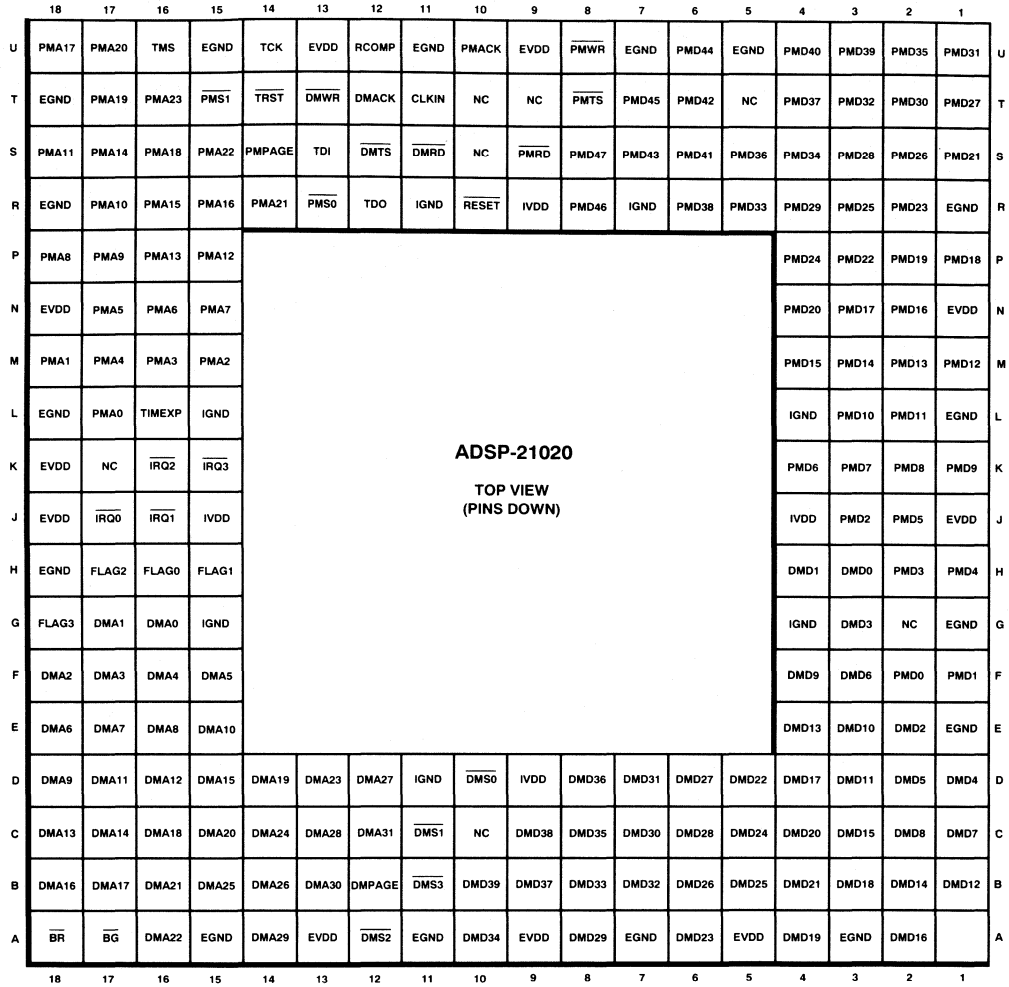
Figure 21. EZ-ICE Probe

The 12-pin, 2-row pin strip header is keyed at the Pin 1 location —you must clip Pin 1 off of the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing is 0.1 × 0.1 inches.

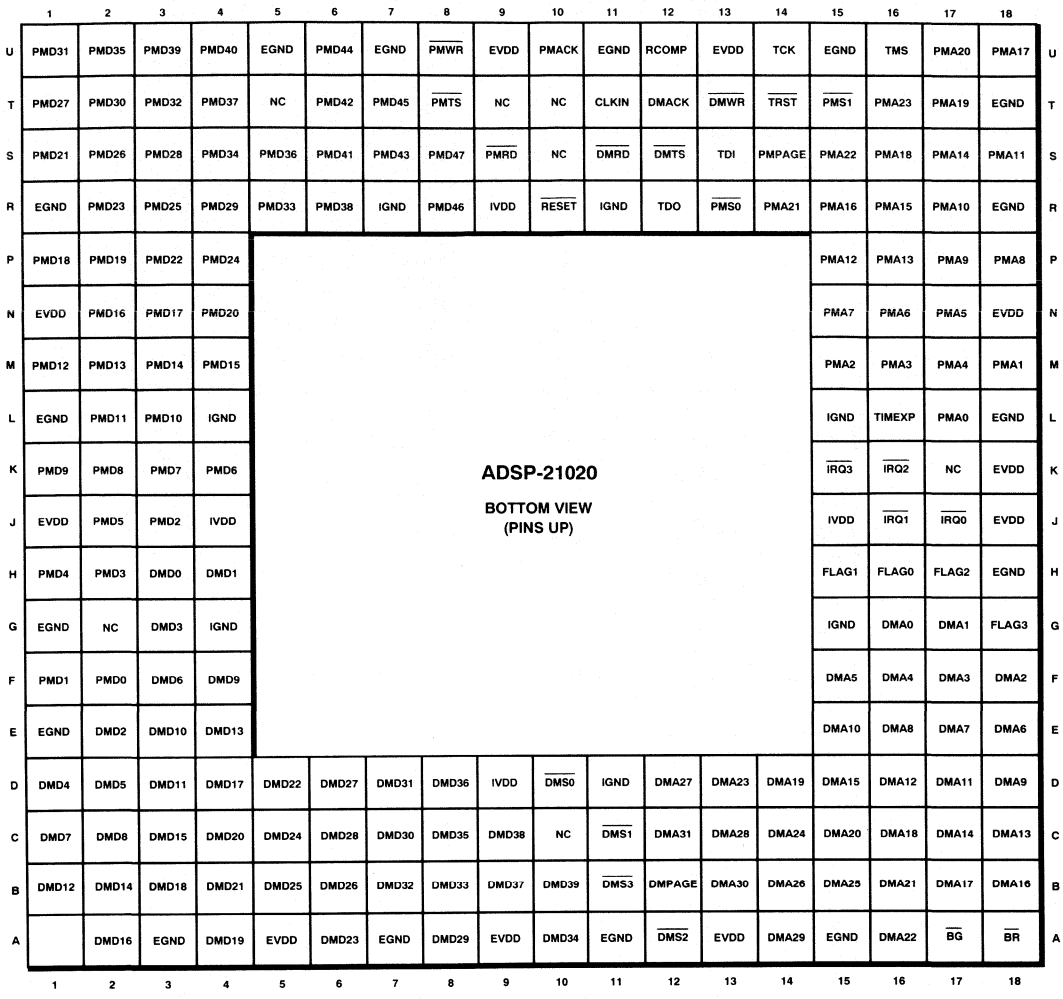
The tip of the pins must be at least 0.10 inch higher than the tallest component under the probe to allow clearance for the bottom of the probe. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

The length of the traces between the EZ-ICE probe connector and the ADSP-21020 test access port pins should be less than 1 inch. Note that the EZ-ICE probe adds two TTL loads to the CLKIN pin of the ADSP-21020.

The BMTS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the BXXX pins and the XXX pins as shown in Figure 20. If you are not going to use the test access port for board test, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to VDD. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-21020.



	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
U	PMA17	PMA20	TMS	EGND	TCK	EVDD	RCOMP	EGND	PMACK	EVDD	$\overline{\text{PMWR}}$	EGND	PMD44	EGND	PMD40	PMD39	PMD35	PMD31	U
T	EGND	PMA19	PMA23	$\overline{\text{PMS1}}$	$\overline{\text{TRST}}$	$\overline{\text{DMWR}}$	DMACK	CLKIN	NC	NC	$\overline{\text{PMTS}}$	PMD45	PMD42	NC	PMD37	PMD32	PMD30	PMD27	T
S	PMA11	PMA14	PMA18	PMA22	PMPAGE	TDI	$\overline{\text{DMTS}}$	$\overline{\text{DMRD}}$	NC	$\overline{\text{PMRD}}$	PMD47	PMD43	PMD41	PMD36	PMD34	PMD28	PMD26	PMD21	S
R	EGND	PMA10	PMA15	PMA16	PMA21	$\overline{\text{PMS0}}$	TDO	IGND	$\overline{\text{RESET}}$	IVDD	PMD46	IGND	PMD38	PMD33	PMD29	PMD25	PMD23	EGND	R
P	PMA8	PMA9	PMA13	PMA12											PMD24	PMD22	PMD19	PMD18	P
N	EVDD	PMA5	PMA6	PMA7											PMD20	PMD17	PMD16	EVDD	N
M	PMA1	PMA4	PMA3	PMA2											PMD15	PMD14	PMD13	PMD12	M
L	EGND	PMA0	TIMEXP	IGND											IGND	PMD10	PMD11	EGND	L
K	EVDD	NC	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ3}}$											PMD6	PMD7	PMD8	PMD9	K
J	EVDD	$\overline{\text{IRQ0}}$	$\overline{\text{IRQ1}}$	IVDD											IVDD	PMD2	PMD5	EVDD	J
H	EGND	FLAG2	FLAG0	FLAG1											DMD1	DMD0	PMD3	PMD4	H
G	FLAG3	DMA1	DMA0	IGND											IGND	DMD3	NC	EGND	G
F	DMA2	DMA3	DMA4	DMA5											DMD9	DMD6	PMD0	PMD1	F
E	DMA6	DMA7	DMA8	DMA10											DMD13	DMD10	DMD2	EGND	E
D	DMA9	DMA11	DMA12	DMA15	DMA19	DMA23	DMA27	IGND	$\overline{\text{DMS0}}$	IVDD	DMD36	DMD31	DMD27	DMD22	DMD17	DMD11	DMD5	DMD4	D
C	DMA13	DMA14	DMA18	DMA20	DMA24	DMA28	DMA31	$\overline{\text{DMS1}}$	NC	DMD38	DMD35	DMD30	DMD28	DMD24	DMD20	DMD15	DMD8	DMD7	C
B	DMA16	DMA17	DMA21	DMA25	DMA26	DMA30	DMPAGE	$\overline{\text{DMS3}}$	DMD39	DMD37	DMD33	DMD32	DMD26	DMD25	DMD21	DMD18	DMD14	DMD12	B
A	$\overline{\text{BR}}$	$\overline{\text{BG}}$	DMA22	EGND	DMA29	EVDD	$\overline{\text{DMS2}}$	EGND	DMD34	EVDD	DMD29	EGND	DMD23	EVDD	DMD19	EGND	DMD16		A
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
U	PMD31	PMD35	PMD39	PMD40	EGND	PMD44	EGND	$\overline{\text{PMWR}}$	EVDD	PMACK	EGND	RCOMP	EVDD	TCK	EGND	TMS	PMA20	PMA17	U
T	PMD27	PMD30	PMD32	PMD37	NC	PMD42	PMD45	$\overline{\text{PMTS}}$	NC	NC	CLKIN	DMACK	$\overline{\text{DMWR}}$	$\overline{\text{TRST}}$	$\overline{\text{PMS1}}$	PMA23	PMA19	EGND	T
S	PMD21	PMD26	PMD28	PMD34	PMD36	PMD41	PMD43	PMD47	$\overline{\text{PMRD}}$	NC	$\overline{\text{DMRD}}$	$\overline{\text{DMTS}}$	TDI	PMPAGE	PMA22	PMA18	PMA14	PMA11	S
R	EGND	PMD23	PMD25	PMD29	PMD33	PMD38	IGND	PMD46	IVDD	$\overline{\text{RESET}}$	IGND	TDO	$\overline{\text{PMS0}}$	PMA21	PMA16	PMA15	PMA10	EGND	R
P	PMD18	PMD19	PMD22	PMD24											PMA12	PMA13	PMA9	PMA8	P
N	EVDD	PMD16	PMD17	PMD20											PMA7	PMA6	PMA5	EVDD	N
M	PMD12	PMD13	PMD14	PMD15											PMA2	PMA3	PMA4	PMA1	M
L	EGND	PMD11	PMD10	IGND											IGND	TIMEXP	PMA0	EGND	L
K	PMD9	PMD8	PMD7	PMD6											$\overline{\text{IRQ3}}$	$\overline{\text{IRQ2}}$	NC	EVDD	K
J	EVDD	PMD5	PMD2	IVDD											IVDD	$\overline{\text{IRQ1}}$	$\overline{\text{IRQ0}}$	EVDD	J
H	PMD4	PMD3	DMD0	DMD1											FLAG1	FLAG0	FLAG2	EGND	H
G	EGND	NC	DMD3	IGND											IGND	DMA0	DMA1	FLAG3	G
F	PMD1	PMD0	DMD6	DMD9											DMA5	DMA4	DMA3	DMA2	F
E	EGND	DMD2	DMD10	DMD13											DMA10	DMA8	DMA7	DMA6	E
D	DMD4	DMD5	DMD11	DMD17	DMD22	DMD27	DMD31	DMD36	IVDD	$\overline{\text{DMS0}}$	IGND	DMA27	DMA23	DMA19	DMA15	DMA12	DMA11	DMA9	D
C	DMD7	DMD8	DMD15	DMD20	DMD24	DMD28	DMD30	DMD35	DMD38	NC	$\overline{\text{DMS1}}$	DMA31	DMA28	DMA24	DMA20	DMA18	DMA14	DMA13	C
B	DMD12	DMD14	DMD18	DMD21	DMD25	DMD26	DMD32	DMD33	DMD37	DMD39	$\overline{\text{DMS3}}$	DMPAGE	DMA30	DMA26	DMA25	DMA21	DMA17	DMA16	B
A		DMD16	EGND	DMD19	EVDD	DMD23	EGND	DMD29	EVDD	DMD34	EGND	$\overline{\text{DMS2}}$	EVDD	DMA29	EGND	DMA22	$\overline{\text{BG}}$	$\overline{\text{BR}}$	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

2

PGA LOCATION	PIN NAME	PGA LOCATION	PIN NAME	PGA LOCATION	PIN NAME	PGA LOCATION	PIN NAME
G16	DMA0	B5	DMD25	K1	PMD9	L16	TIMEXP
G17	DMA1	B6	DMD26	L3	PMD10	U12	RCOMP
F18	DMA2	D6	DMD27	L2	PMD11	T11	CLKIN
F17	DMA3	C6	DMD28	M1	PMD12	T14	TRST
F16	DMA4	A8	DMD29	M2	PMD13	R12	TD0
F15	DMA5	C7	DMD30	M3	PMD14	S13	TDI
E18	DMA6	D7	DMD31	M4	PMD15	U16	TMS
E17	DMA7	B7	DMD32	N2	PMD16	U14	TCK
E16	DMA8	B8	DMD33	N3	PMD17	H18	EGND
D18	DMA9	A10	DMD34	P1	PMD18	A3	EGND
E15	DMA10	C8	DMD35	P2	PMD19	A7	EGND
D17	DMA11	D8	DMD36	N4	PMD20	A11	EGND
D16	DMA12	B9	DMD37	S1	PMD21	A15	EGND
C18	DMA13	C9	DMD38	P3	PMD22	E1	EGND
C17	DMA14	B10	DMD39	R2	PMD23	G1	EGND
D15	DMA15	D10	$\overline{\text{DMS0}}$	P4	PMD24	L1	EGND
B18	DMA16	C11	$\overline{\text{DMS1}}$	R3	PMD25	L18	EGND
B17	DMA17	A12	$\overline{\text{DMS2}}$	S2	PMD26	R1	EGND
C16	DMA18	B11	$\overline{\text{DMS3}}$	T1	PMD27	R18	EGND
D14	DMA19	T13	$\overline{\text{DMWR}}$	S3	PMD28	T18	EGND
C15	DMA20	S11	$\overline{\text{DMRD}}$	R4	PMD29	U5	EGND
B16	DMA21	B12	$\overline{\text{DMPAGE}}$	T2	PMD30	U7	EGND
A16	DMA22	S12	$\overline{\text{DMTS}}$	U1	PMD31	U11	EGND
D13	DMA23	T12	$\overline{\text{DMACK}}$	T3	PMD32	U15	EGND
C14	DMA24	L17	PMA0	R5	PMD33	D11	IGND
B15	DMA25	M18	PMA1	S4	PMD34	G4	IGND
B14	DMA26	M15	PMA2	U2	PMD35	G15	IGND
D12	DMA27	M16	PMA3	S5	PMD36	L4	IGND
C13	DMA28	M17	PMA4	T4	PMD37	L15	IGND
A14	DMA29	N17	PMA5	R6	PMD38	R7	IGND
B13	DMA30	N16	PMA6	U3	PMD39	R11	IGND
C12	DMA31	N15	PMA7	U4	PMD40	A5	EVDD
H3	DMD0	P18	PMA8	S6	PMD41	A9	EVDD
H4	DMD1	P17	PMA9	T6	PMD42	A13	EVDD
E2	DMD2	R17	PMA10	S7	PMD43	J1	EVDD
G3	DMD3	S18	PMA11	U6	PMD44	J18	EVDD
D1	DMD4	P15	PMA12	T7	PMD45	N1	EVDD
D2	DMD5	P16	PMA13	R8	PMD46	N18	EVDD
F3	DMD6	S17	PMA14	S8	PMD47	U9	EVDD
C1	DMD7	R16	PMA15	R13	$\overline{\text{PMS0}}$	U13	EVDD
C2	DMD8	R15	PMA16	T15	$\overline{\text{PMS1}}$	K18	EVDD
F4	DMD9	U18	PMA17	U8	$\overline{\text{PMWR}}$	D9	IVDD
E3	DMD10	S16	PMA18	S9	$\overline{\text{PMRD}}$	J4	IVDD
D3	DMD11	T17	PMA19	S14	$\overline{\text{PMPAGE}}$	J15	IVDD
B1	DMD12	U17	PMA20	T8	$\overline{\text{PMTS}}$	R9	IVDD
E4	DMD13	R14	PMA21	U10	$\overline{\text{PMACK}}$	C10	NC
B2	DMD14	S15	PMA22	A17	$\overline{\text{BG}}$	S10	NC
C3	DMD15	T16	PMA23	A18	$\overline{\text{BR}}$	T10	NC
A2	DMD16	F2	PMD0	H16	FLAG0	T9	NC
D4	DMD17	F1	PMD1	H15	FLAG1	K17	NC
B3	DMD18	J3	PMD2	H17	FLAG2	T5	NC
A4	DMD19	H2	PMD3	G18	FLAG3	G2	NC
C4	DMD20	H1	PMD4	J17	$\overline{\text{IRQ0}}$		
B4	DMD21	J2	PMD5	J16	$\overline{\text{IRQ1}}$		
D5	DMD22	K4	PMD6	K16	$\overline{\text{IRQ2}}$		
A6	DMD23	K3	PMD7	K15	$\overline{\text{IRQ3}}$		
C5	DMD24	K2	PMD8	R10	$\overline{\text{RESET}}$		

ORDERING GUIDE

Part Number	Ambient Temperature Range	Instruction Rate (MHz)	Cycle Time (ns)	Package Description	Package Option*
ADSP-21020KG-80	0°C to +70°C	20	50	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020KG-100	0°C to +70°C	25	40	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020KG-133	0°C to +70°C	33.3	30	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020BG-80	−40°C to +85°C	20	50	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020BG-100	−40°C to +85°C	25	40	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020BG-120	−40°C to +85°C	30	33.3	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-80	−55°C to +125°C	20	50	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-100	−55°C to +125°C	25	40	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-120	−55°C to +125°C	30	33.3	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-80/883B	−55°C to +125°C	20	50	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-100/883B	−55°C to +125°C	25	40	223-Lead Ceramic Pin Grid Array	G-223
ADSP-21020TG-120/883B	−55°C to +125°C	30	33.3	223-Lead Ceramic Pin Grid Array	G-223

*G = Ceramic Pin Grid Array. For outline information see Package Information section.

ANALOG DEVICES

SHARC
Super Harvard Architecture Computers

ADSP-21060/ADSP-21062

SUMMARY

High Performance Signal Processor for Speech, Sound, Graphics, and Imaging Applications
Super Harvard Architecture—Four Independent Buses for Dual Data, Instructions, and I/O
32-Bit IEEE Floating-Point Computation Units—Multiplier, ALU, and Shifter
Dual-Ported On-Chip SRAM and Integrated I/O Peripherals—A Complete System-on-a-Chip
Integrated Multiprocessing Features

KEY FEATURES

40 MIPS, 25 ns Instruction Rate, Single-Cycle Instruction Execution
120 MFLOPS Peak, 80 MFLOPS Sustained Performance
Dual Data Address Generators with Modulo and Bit-Reverse Addressing
Efficient Program Sequencing with Zero-Overhead Looping: Single-Cycle Loop Setup
IEEE JTAG Standard 1149.1 Test Access Port and On-Chip Emulation
240-Lead Thermally Enhanced PQFP Package
ADSP-21062 Pin Compatible with ADSP-21060

Flexible Data Formats & 40-Bit Extended-Precision

32-Bit Single-Precision & 40-Bit Extended-Precision IEEE Floating-Point Data Formats
32-Bit Fixed-Point Data Format, Integer & Fractional, with 80-Bit Accumulators

Parallel Computations

Single-Cycle Multiply & ALU Operations in Parallel with Dual Memory Read/Writes & Instruction Fetch
Multiply with Add & Subtract for Accelerated FFT Butterfly Computation
1024-Point Complex FFT Benchmark: 0.46 ms (18,221 Cycles)

4 Mbit/2 Mbit On-Chip SRAM (ADSP-21060/ADSP-21062)

Dual-Ported for Independent Access by Core Processor and DMA
Configurable as 128K Words Data Memory (32-Bit), 80K Words Program Memory (48-Bit), or Combinations of Both Up To 4 Mbits (ADSP-21060)
Configurable as 64K Words Data Memory (32-Bit), 40K Words Program Memory (48-Bit), or Combinations of Both Up To 2 Mbits (ADSP-21062)

Off-Chip Memory Interfacing

4 Gigawords Addressable (32-Bit Address)
Programmable Wait State Generation, Page-Mode DRAM Support

DMA Controller

10 DMA Channels
Background DMA Transfers at 40 MHz, in Parallel with Full-Speed Processor Execution
Performs Transfers Between ADSP-2106x Internal Memory and External Memory, External Peripherals, Host Processor, Serial Ports, or Link Ports

Host Processor Interface

Efficient Interface to 16- & 32-Bit Microprocessors
Host Can Directly Read/Write ADSP-2106x Internal Memory

Multiprocessing

Glueless Connection for Scalable DSP Multiprocessing Architecture
Distributed On-Chip Bus Arbitration for Parallel Bus Connect of Up to Six ADSP-2106xs Plus Host
Six Link Ports for Point-to-Point Connectivity and Array Multiprocessing
240 Mbytes/s Transfer Rate Over Parallel Bus
240 Mbytes/s Transfer Rate Over Link Ports

Serial Ports

Two 40 Mbits/ Synchronous Serial Ports
Independent Transmit & Receive Functions
3- to 32-Bit Data Word Width
μ-Law/A-Law Hardware Companding
TDM Multichannel Mode

This is a preliminary data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

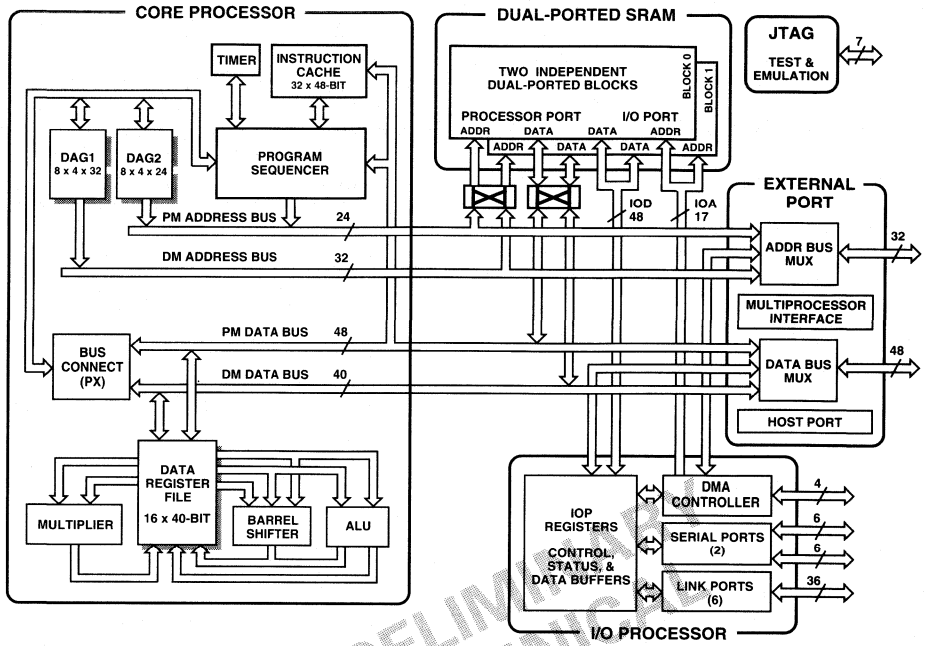


Figure 1. ADSP-21060/ADSP-21062 Block Diagram

GENERAL DESCRIPTION

The ADSP-21060 and ADSP-21062 SHARC—Super Harvard Architecture Computers—are signal processing microcomputers that offer new capabilities and levels of performance. The ADSP-2106x SHARCs are 32-bit processors optimized for high performance DSP applications. The ADSP-2106x builds on the ADSP-21000 DSP core to form a complete system-on-a-chip, adding a dual-ported on-chip SRAM and integrated I/O peripherals supported by a dedicated I/O bus.

Fabricated in a high speed, low power CMOS process, the ADSP-2106x has a 25 ns instruction cycle time operating at 40 MIPS. With its on-chip instruction cache, the processor can execute every instruction in a single cycle. Table I shows performance benchmarks for the ADSP-2106x.

The ADSP-2106x SHARC represents a new standard of integration for signal computers, combining a high performance floating-point DSP core with integrated, on-chip system features including a 4 Mbit SRAM memory (2 Mbit on the ADSP-21062), host processor interface, DMA controller, serial ports, and link port and parallel bus connectivity for glueless DSP multiprocessing.

Figure 1 shows a block diagram of the ADSP-2106x, illustrating the following architectural features:

- Computation Units (ALU, Multiplier, and Shifter) with a Shared Data Register File
- Data Address Generators (DAG1, DAG2)
- Program Sequencer with Instruction Cache
- Interval Timer
- On-Chip SRAM
- External Port for Interfacing to Off-Chip Memory & Peripherals
- Host Port & Multiprocessor Interface
- DMA Controller
- Serial Ports & Link Ports
- JTAG Test Access Port

Figure 2 shows a typical single-processor system. A multiprocessing system is shown in Figure 3.

Table I. ADSP-21060/ADSP-21062 Benchmarks (@ 40 MHz)

1024-Pt Complex FFT (Radix 4, with Digit Reverse)	0.46 ms	18,221 Cycles
FIR Filter (Per Tap)	25 ns	1 Cycle
IIR Filter (Per Biquad)	100 ns	4 Cycles
Divide (y/x)	150 ns	6 Cycles
Inverse Square Root ($1/\sqrt{x}$)	225 ns	9 Cycles
DMA Transfer Rate	240 Mbyte/s	

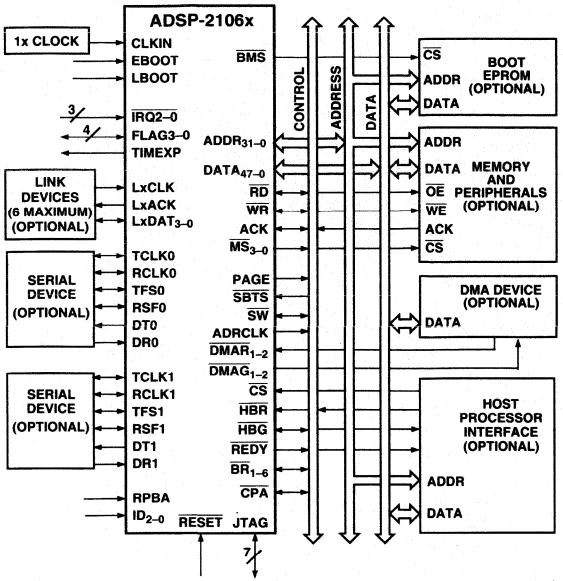


Figure 2. ADSP-21060x System

ADSP-21000 FAMILY CORE ARCHITECTURE

The ADSP-2106x includes the following architectural features of the ADSP-21000 Family core. The ADSP-21060 and ADSP-21062 are code- and function-compatible with the ADSP-21020.

- **Independent, Parallel Computation Units**
  The arithmetic/logic unit (ALU), multiplier, and shifter all perform single-cycle instructions. The three units are arranged in parallel, maximizing computational throughput. Single multifunction instructions execute parallel ALU and multiplier operations. These computation units support IEEE 32-bit single-precision floating-point, extended precision 40-bit floating-point, and 32-bit fixed-point data formats.
- **Data Register File**
  A general-purpose data register file is used for transferring data between the computation units and the data buses, and for storing intermediate results. This 10-port, 32-register (16 primary, 16 secondary) register file, combined with the ADSP-21000 Harvard architecture, allows unconstrained data flow between computation units and internal memory.
- **Single-Cycle Fetch of Instruction and Two Operands**
  The ADSP-2106x features an enhanced Harvard architecture in which the data memory (DM) bus transfers data and the program memory (PM) bus transfers both instructions and data (see Figure 1). With its separate program and data memory buses and on-chip instruction cache, the processor can simultaneously fetch two operands and an instruction (from the cache), all in a single cycle.
- **Instruction Cache**
  The ADSP-2106x includes an on-chip instruction cache that enables three-bus operation for fetching an instruction and two data values. The cache is selective—only the instructions whose fetches conflict with PM bus data accesses are cached. This allows full-speed execution of core, looped operations such as digital filter multiply-accumulates and FFT butterfly processing.
- **Data Address Generators with Hardware Circular Buffers**
  The ADSP-2106x's two data address generators (DAGs) implement circular data buffers in hardware. Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing, and are commonly used in digital filters and Fourier transforms. The ADSP-2106x's two DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets, 16 secondary). The DAGs automatically handle address pointer wraparound, reducing overhead, increasing performance, and simplifying implementation. Circular buffers can start and end at any memory location.
- **Flexible Instruction Set**
  The 48-bit instruction word accommodates a variety of parallel operations, for concise programming. For example, the ADSP-2106x can conditionally execute a multiply, an add, a subtract and a branch, all in a single instruction.

ADSP-21060/ADSP-21062 Features

Augmenting the ADSP-21000 family core, the ADSP-21060 and ADSP-21062 add the following architectural features:

- **Dual-Ported On-Chip Memory**
  The ADSP-21060 contains 4 megabits of on-chip SRAM, organized as two blocks of 2 Mbits each, which can be configured for different combinations of code and data storage. The ADSP-21062 includes a 2 Mbit SRAM, organized as two 1 Mbit blocks. Each memory block is dual-ported for single-cycle, independent accesses by the core processor and I/O processor or DMA controller. The dual-ported memory and separate on-chip buses allow two data transfers from the core and one from I/O, all in a single cycle.

  On the ADSP-21060, the memory can be configured as a maximum of 128K words of 32-bit data, 256K words of 16-bit data, 80K words of 48-bit instructions (and 40-bit data), or combinations of different word sizes up to 4 megabits. On the ADSP-21062, the memory can be configured as a maximum of 64K words of 32-bit data, 128K words of 16-bit data, 40K words of 48-bit instructions (and 40-bit data), or combinations of different word sizes up to 2 megabits. All of the memory can be accessed as 16-bit, 32-bit, or 48-bit words.

  A 16-bit floating-point storage format is supported which effectively doubles the amount of data that may be stored on chip. Conversion between the 32-bit floating-point and 16-bit floating-point formats is done in a single instruction.

  While each memory block can store combinations of code and data, accesses are most efficient when one block stores data, using the DM bus for transfers, and the other block stores instructions and data, using the PM bus for transfers. Using the DM bus and PM bus in this way, with one dedicated to each memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. Single-cycle execution is also maintained when one of the data operands is transferred to or from off-chip, via the ADSP-2106x's external port.

- **Off-Chip Memory & Peripherals Interface**
  The ADSP-2106x's external port provides the processor's interface to off-chip memory and peripherals. The 4 gigaword off-chip address space is included in the ADSP-2106x's unified address space. The separate on-chip buses—for PM addresses, PM data, DM addresses, DM data, I/O addresses, and I/O data—are multiplexed at the external port to create an external system bus with a single 32-bit address bus and a single 48-bit (or 32-bit) data bus.

  Addressing of external memory devices is facilitated by on-chip decoding of high-order address lines to generate memory bank select signals. Separate control lines are also generated for simplified addressing of page-mode DRAM. The ADSP-2106x provides programmable memory wait states and external memory acknowledge controls to allow interfacing to DRAM and peripherals with variable access, hold, and disable time requirements.

- **Host Processor Interface**
  The ADSP-2106x's host interface allows easy connection to standard microprocessor buses, both 16-bit and 32-bit, with little additional hardware required. Asynchronous transfers at speeds up to the full clock rate of the processor are supported. The host interface is accessed through the ADSP-2106x's external port and is memory-mapped into the unified address space. Four channels of DMA are available for the host interface; code and data transfers are accomplished with low software overhead.

  The host processor requests the ADSP-2106x's external bus with the host bus request ($\overline{HBR}$), host bus grant ($\overline{HBG}$), and ready (REDY) signals. The host can directly read and write the internal memory of the ADSP-2106x, and can access the DMA channel setup and mailbox registers. Vector interrupt support is provided for efficient execution of host commands.

- **DMA Controller**
  The ADSP-2106x's on-chip DMA controller allows zero-overhead data transfers without processor intervention. The DMA controller operates independently and invisibly to the processor core, allowing DMA operations to occur while the core is simultaneously executing its program instructions.

  DMA transfers can occur between the ADSP-2106x's internal memory and either external memory, external peripherals, or a host processor. DMA transfers can also occur between the ADSP-2106x's internal memory and its serial ports or link ports. DMA transfers between external memory and external peripheral devices are another option. External bus packing to 16-, 32-, or 48-bit words is performed during DMA transfers.

  Ten channels of DMA are available on the ADSP-2106x—two via the link ports, four via the serial ports, and four via the processor's external port (for either host processor, other ADSP-2106xs, memory or I/O transfers). Four additional link port DMA channels are shared with serial port 1 and the external port. Programs can be downloaded to the ADSP-2106x using DMA transfers. Asynchronous off-chip peripherals can control two DMA channels using DMA Request/Grant lines ($\overline{DMAR}_{1-2}$, $\overline{DMAG}_{1-2}$). Other DMA features include interrupt generation upon completion of DMA transfers and DMA chaining for automatic linked DMA transfers.

- **Serial Ports**
  The ADSP-2106x features two synchronous serial ports that provide an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. The serial ports can operate at the full clock rate of the processor, providing each with a maximum data rate of 40 Mbit/s. Independent transmit and receive functions provide greater flexibility for serial communications. Serial port data can be automatically transferred to and from on-chip memory via DMA. Each of the serial ports offers TDM multichannel mode.

  The serial ports can operate with little-endian or big-endian transmission formats, with word lengths selectable from 3 to 32 bits. They offer selectable synchronization and transmit modes as well as optional μ-law or A-law companding. Serial port clocks and frame syncs can be internally or externally generated.

- **Multiprocessing**
  The ADSP-2106x offers powerful features tailored to multiprocessing DSP systems. The unified address space allows direct interprocessor accesses of each ADSP-2106x's internal memory. Distributed bus arbitration logic is included on-chip for simple, glueless connection of systems containing up to six ADSP-2106xs and a host processor. Master processor changeover incurs only one cycle of overhead. Bus arbitration is selectable as either fixed or rotating priority. Bus lock allows indivisible *read-modify-write* sequences for semaphores. A vector interrupt is provided for interprocessor commands. Maximum throughput for interprocessor data transfer is 240 Mbytes/s over the link ports or external port. *Broadcast writes* allow simultaneous transmission of data to all ADSP-2106xs and can be used to implement reflective semaphores.

- **Link Ports**
  The ADSP-2106x features six 4-bit link ports that provide additional I/O capabilities. The link ports can be clocked twice per cycle, allowing each to transfer 8 bits per cycle. Link port I/O is especially useful for point-to-point interprocessor communication in multiprocessing systems.

  The link ports can operate independently and simultaneously, with a maximum data throughput of 240 Mbytes/s. Link port data is packed into 32-bit or 48-bit words, and can be directly read by the core processor or DMA-transferred to on-chip memory.

  Each link port has its own double-buffered input and output registers. Clock/acknowledge handshaking controls link port transfers. Transfers are programmable as either transmit or receive.

- **Program Booting**
  The internal memory of the ADSP-2106x can be booted at system powerup from either an 8-bit EPROM, a host processor, or through one of the link ports. Selection of the boot source is controlled by the $\overline{BMS}$ (Boot Memory Select), EBOOT (EPROM Boot), and LBOOT (Link/Host Boot) pins. Thirty-two-bit and 16-bit host processors can be used for booting.

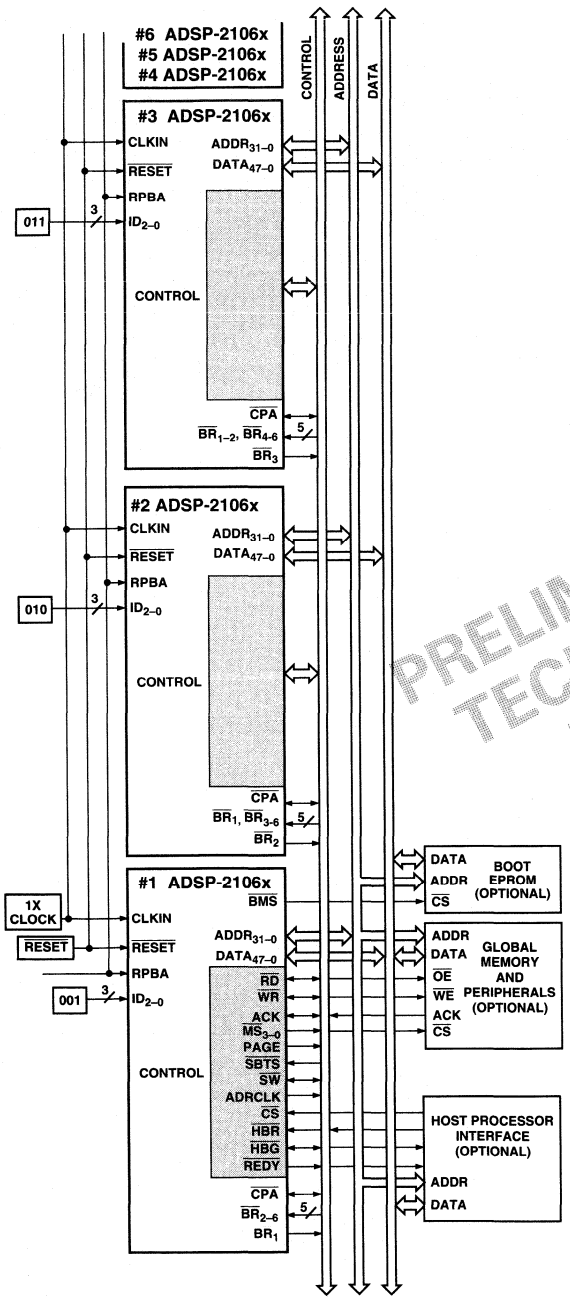


Figure 3. Multiprocessing System

ADSP-21060 MEMORY MAP

The ADSP-21060/ADSP-21062 memory map is divided into three spaces: internal memory space, multiprocessor memory space, and external memory space. Internal memory space consists of the ADSP-2106x's on-chip memory and resources. Multiprocessor memory space corresponds to the on-chip memory and resources of other ADSP-2106x's in a multiprocessor system. External memory space corresponds to off-chip memory and memory-mapped I/O devices.

As shown in Figure 4, the address boundaries of each memory space are:

Internal Memory Space	0x0000 0000	to	0x0007 FFFF
Multiprocessor Memory Space	0x0008 0000	to	0x003F FFFF
External Memory Space	0x0040 0000	to	0xFFFF FFFF

The internal memory space of the ADSP-21060 is shown in Figure 5. This memory has three address regions:

I/O Processor (IOP) Registers	0x0000 0000	to	0x0000 00FF
Normal Word Addresses	0x0002 0000	to	0x0003 FFFF
Interrupt Vector Table	*0x0002 0000*	*to*	*0x0002 003F*
Short Word Addresses	0x0004 0000	to	0x0007 FFFF

Memory Block 0 starts at the beginning of normal word space, at address 0x0002 0000. Block 1 starts at the middle of normal word space, at address 0x0003 0000.

Table II. ADSP-21060 Internal Memory Addresses

0x0000 0000–0x0000 00FF	IOP Registers *(Control/Status Registers)*
0x0000 0100–0x0001 FFFF	Reserved Addresses
0x0002 0000–0x0002 FFFF	Block 0—Normal Word Addressing *(32-Bit, 48-Bit Words)*
0x0003 0000–0x0003 FFFF	Block 1—Normal Word Addressing *(32-Bit, 48-Bit Words)*
0x0004 0000–0x0005 FFFF	Block 0—Short Word Addressing *(16-Bit Words)*
0x0006 0000–0x0007 FFFF	Block 1—Short Word Addressing *(16-Bit Words)*

The normal word address space and short word address space actually access *the same physical memory*. For example, the normal word address 0x0002 0000 represents the same locations as short word addresses 0x0004 0000 and 0x0004 0001 (for a 32-bit data access in normal word space).

The 4 megabits of on-chip memory can be accessed with either normal word addressing, short word addressing, or combinations of both. The range of normal word addresses, from 0x0002 0000 through 0x0003 FFFF, is exactly 4 megabits when each word is 32 bits wide (128K × 32). (The normal word addressing range also accesses 4 megabits of 48-bit wide instruction words, 80K × 48, but with missing addresses at the end of Block 0 and Block 1.) The range of short word addresses, from 0x0004 0000 through 0x0007 FFFF, is also exactly 4 megabits (256K × 16).

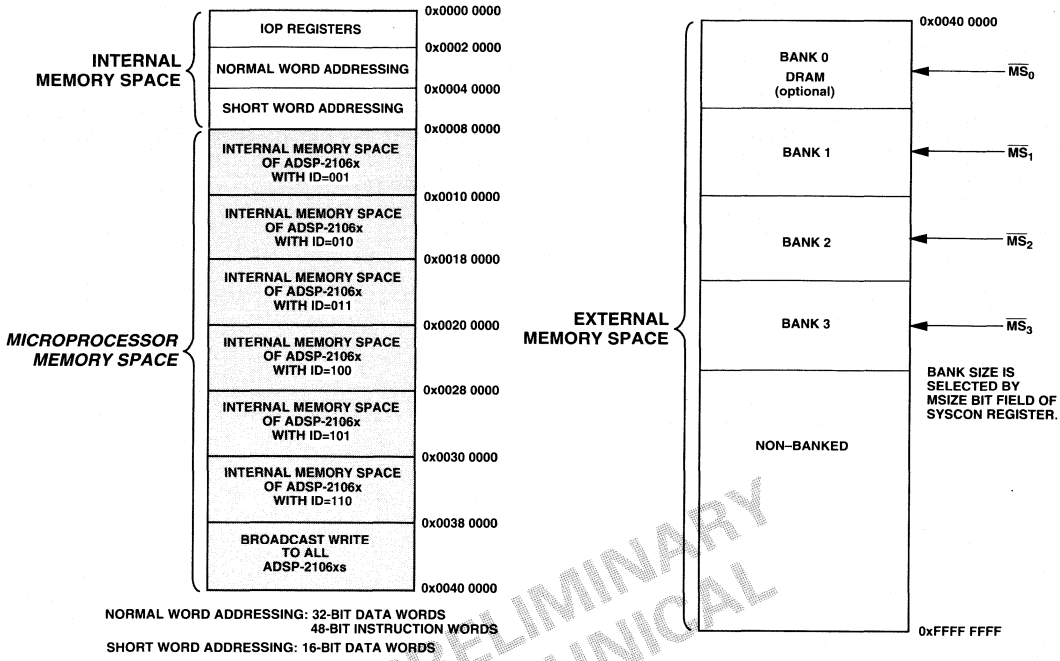


Figure 4. ADSP-21060/ADSP-21062 Memory Map

ADSP-21062 Memory Map

The ADSP-21062 is a reduced memory version of the ADSP-21060. The two processors include the following amounts of on-chip SRAM:

Processor	Total Memory	Maximum Data Memory	Maximum Program Memory
ADSP-21060	4 Mbits	128K × 32	80K × 48
ADSP-21062	2 Mbits	64K × 32	40K × 48

The on-chip memory of the ADSP-21062 is divided into two equal blocks, Block 0 and Block 1, in the same way as the ADSP-21060's. The ADSP-21062's multiprocessor memory space and external memory space are exactly the same as that of the ADSP-21060.

On the ADSP-21062, Block 0 starts at normal word address 0x0002 0000. Block 1 starts at normal word address 0x0002 8000. The memory map for the ADSP-21062's 2 Mbits of internal memory is shown in Figure 6 and in Table III. The *Block 1 Alias* address ranges will access the actual Block 1, 0x0002 8000 – 0x0002 FFFF in normal word address space and 0x0005 0000 – 0x0005 FFFF in short word address space.

Table III. ADSP-21062 Internal Memory Addresses

0x0000 0000–0x0000 00FF	IOP Registers (Control/Status Registers)
0x0000 0100–0x0001 FFFF	*Reserved Addresses*
0x0002 0000–0x0002 7FFF	Block 0—Normal Word Addressing
0x0002 8000–0x0002 FFFF	Block 1—Normal Word Addressing
0x0003 0000–0x0003 7FFF	Alias of Block 1 *(i.e., Accesses Block1)* —Normal Word Addressing
0x0003 8000–0x0003 FFFF	Alias of Block 1 *(i.e., Accesses Block1)* —Normal Word Addressing
0x0004 0000–0x0004 FFFF	Block 0—Short Word Addressing
0x0005 0000–0x0005 FFFF	Block 1—Short Word Addressing
0x0006 0000–0x0006 FFFF	Alias of Block 1 *(i.e., Accesses Block1)* —Short Word Addressing
0x0007 0000–0x0007 FFFF	Alias of Block 1 *(i.e., Accesses Block1)* —Short Word Addressing

Porting Code from ADSP-21060 to ADSP-21062

On the ADSP-21062, Block 0 starts at the beginning of internal memory, normal word address 0x0002 0000. Block 1 starts at the end of Block 0, with contiguous addresses. The remaining addresses in internal memory are divided into blocks which alias into Block 1.

This allows any code or data stored in Block 1 on the ADSP-21060 to retain the same addresses on the ADSP-21062—these addresses will alias into the actual Block 1 of each processor.

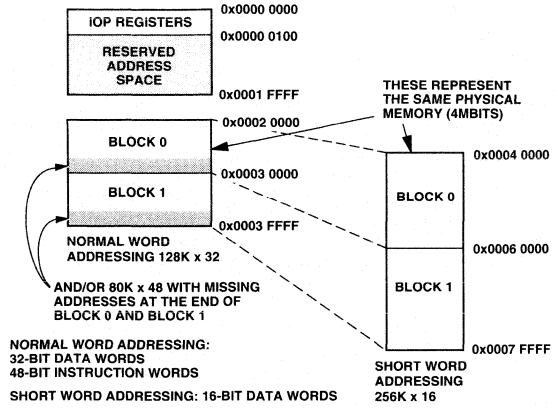


Figure 5. ADSP-21060 Internal Memory Space (4 Mbit)

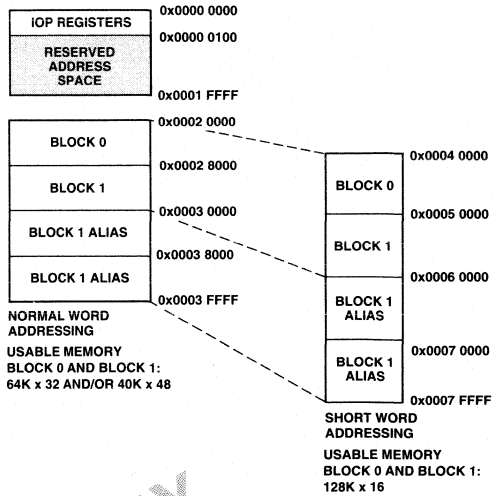


Figure 6. ADSP-21062 Internal Memory Space (2 Mbit)

DEVELOPMENT SYSTEM

The ADSP-2106x is supported with a complete set of software and hardware development tools, including an EZ-LAB® Evaluation Board, EZ-ICE® In-Circuit Emulator, and development software.

The ADSP-21000 Family Development Software includes G21K, an ANSI C Compiler based on the industry-standard GNU C Compiler of the Free Software Foundation. The G21K compiler includes Numerical C extensions based on the work of the ANSI NCEG committee (Numerical C Extensions Group); these extensions have also been incorporated into the GNU compiler, in gcc version 2.4. Numerical C provides extensions to the C language for array selection, vector math operations, complex data types, circular pointers, and variably dimensioned arrays. An Ada compiler for the ADSP-21000 Family is available from Meridian Software Systems of the Verdix Corporation. Other components of the ADSP-21000 Family Development Software include a C Runtime Library with custom DSP functions, CBUG™ C Source-Level Debugger, Assembler, Assembly Library/Librarian, Linker, and Simulator.

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x processor to monitor and control the target board processor during emulation. The EZ-ICE provides full-speed emulation, allowing inspection and modification of memory, registers, and processor stacks. Nonintrusive in-circut emulation is assured by the use of the processor's JTAG interface—the emulator does not affect target system loading or timing.

Further details and ordering information are available in the *ADSP-21000 Family Hardware & Software Development Tools* data sheet (ADDS-210xx-TOOLS). This data sheet can be requested from any Analog Devices sales office or distributor.

ADDITIONAL INFORMATION

This preliminary data sheet provides a general overview of the ADSP-2106x architecture and functionality. For detailed information on the ADSP-21000 Family core architecture and instruction set, refer to the *ADSP-21020/21010 User's Manual (2nd Edition)*, which should be used in conjunction with the *ADSP-2106x SHARC Preliminary User's Manual (3/94 Revision)*.

PIN DESCRIPTIONS

ADSP-2106x pin definitions are given in the table that follows. All pins are identical on the ADSP-21060 and ADSP-21062. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied to IV_{DD} or IGND, except for $ADDR_{31-0}$, $DATA_{47-0}$, and inputs that have internal pullup or pulldown resistors ($\overline{\text{CPA}}$, DTx, DRx, TCLKx, RCLKx, $LxDAT_{3-0}$, LxCLK, LxACK, TMS, and TDI)—these pins should be left floating. These pins have a logic level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (o/d) = Open Drain
O = Output A = Asynchronous G = Ground
T = Three-state (when $\overline{SBTS}$ or $\overline{HBR}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin Name	Type	Function
$ADDR_{31-0}$	I/O/T	External Bus Address. The ADSP-2106x outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the internal memory or IOP registers of other ADSP-2106xs. The ADSP-2106x inputs addresses when a host processor or multiprocessing bus master is reading or writing its internal memory or IOP registers.
$DATA_{47-0}$	I/O/T	External Bus Data. The ADSP-2106x inputs and outputs data and instructions on these pins. 32-bit single-precision floating-point data and 32-bit fixed-point data is transferred over Bits 47–16 of the bus. 40-bit extended-precision floating-point data is transferred over Bits 47–8 of the bus. 16-bit short word data is transferred over Bits 31–16 of the bus.
$\overline{MS}_{3-0}$	O/T	Memory Select Lines. These lines are asserted (low) as chip selects for the corresponding banks of external memory. Memory bank size must be defined in the ADSP-2106x's system control register (SYSCON). The $\overline{MS}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{MS}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. $\overline{MS}_0$ provides a select line for a bank of DRAM memory (Bank 0). In a multiprocessing system the $\overline{MS}_{3-0}$ lines are output by the bus master.
$\overline{RD}$	I/O/T	Memory Read Strobe. This pin is asserted (low) when the ADSP-2106x reads from external memory devices or from the internal memory of other ADSP-2106xs. External devices (including other ADSP-2106xs) must assert $\overline{RD}$ to read from the ADSP-2106x's internal memory. In a multiprocessing system $\overline{RD}$ is output by the bus master and is input by all other ADSP-2106xs.
$\overline{WR}$	I/O/T	Memory Write Strobe. This pin is asserted (low) when the ADSP-2106x writes to external memory devices or to the internal memory of other ADSP-2106xs. External devices must assert $\overline{WR}$ to write to the ADSP-2106x's internal memory. In a multiprocessing system $\overline{WR}$ is output by the bus master and is input by all other ADSP-2106xs.
PAGE	O/T	DRAM Page Boundary. The ADSP-2106x asserts this pin to signal that an external DRAM page boundary has been crossed. DRAM page size must be defined in the ADSP-2106x's memory control register (WAIT). DRAM can only be implemented in external memory Bank 0; the PAGE signal can only be activated for Bank 0 accesses. In a multiprocessing system PAGE is output by the bus master.
ADRCLK	O/T	Address Clock for synchronous external memories. Addresses on $ADDR_{31-0}$ are valid before the rising edge of ADRCLK. In a multiprocessing system ADRCLK is output by the bus master.
$\overline{SW}$	I/O/T	Synchronous Write Select. This signal is used to interface the ADSP-2106x to synchronous memory devices (including other ADSP-2106xs). The ADSP-2106x asserts $\overline{SW}$ (low) to provide an early indication of an impending write cycle, which can be aborted if $\overline{WR}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessing system, $\overline{SW}$ is output by the bus master and is input by all other ADSP-2106xs to determine if the multiprocessor memory access is a read or write. $\overline{SW}$ is asserted at the same time as the address output. A host processor using synchronous writes must assert this pin when writing to the ADSP-2106x(s).
ACK	I/O/S	Memory Acknowledge. External devices can deassert ACK (low) to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-2106x deasserts ACK as an output to add wait states to an access of its internal memory. In a multiprocessing system, a slave ADSP-2106x deasserts the bus master's ACK input to add wait state(s) to an access of its internal memory. The bus master has a keeper latch on its ACK pin that maintains the input at the level it was last driven to.

Pin Name	Type	Function
$\overline{SBTS}$	I/S	Suspend Bus Three-state. External devices can assert $\overline{SBTS}$ (low) to place the external bus address, data, selects, and strobes in a high-impedance state for the following cycle. If the ADSP-2106x attempts to access external memory while $\overline{SBTS}$ is asserted, the processor will halt and the memory access will not be completed until $\overline{SBTS}$ is deasserted. $\overline{SBTS}$ should only be used to recover from PAGE faults or host processor/ADSP-2106x deadlock.
$\overline{IRQ}_{2-0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$FLAG_{3-0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.
TIMEXP	O	Timer Expired. Asserted for four cycles when the value of TCOUNT is decremented to zero.
$\overline{HBR}$	I/A	Host Bus Request. Must be asserted by a host processor to request control of the ADSP-2106x's external bus. When $\overline{HBR}$ is asserted in a multiprocessing system, the ADSP-2106x that is bus master will relinquish the bus and assert $\overline{HBG}$. To relinquish the bus, the ADSP-2106x places the address, data, select, and strobe lines in a high-impedance state. $\overline{HBR}$ has priority over all ADSP-2106x bus requests ($\overline{BR}_{6-1}$) in a multiprocessing system.
$\overline{HBG}$	I/O/T	Host Bus Grant. Acknowledges an $\overline{HBR}$ bus request, indicating that thehost processor may take control of the external bus. $\overline{HBG}$ is asserted (held low) by the ADSP-2106x until $\overline{HBR}$ is released. In a multiprocessing system, $\overline{HBG}$ is output by the ADSP-2106x that is bus master and is monitored by all others.
$\overline{CS}$	I	Chip Select. Asserted by host processor to select the ADSP-2106x.
REDY (o/d)	O	Host Bus Acknowledge. The ADSP-2106x deasserts REDY (low) to add wait states to an access of its internal memory or IOP registers by a host. REDY can be connected to the IOCHRDY (I/O Channel Ready) signal of the ISA bus. Open drain output. REDY can only be output if the $\overline{CS}$ input is asserted.
$\overline{DMAR1}$	I	DMA Request 1 (Channel 1).
$\overline{DMAR2}$	I	DMA Request 2 (Channel 2).
$\overline{DMAG1}$	O/T	DMA Grant 1 (Channel 1).
$\overline{DMAG2}$	O/T	DMA Grant 2 (Channel 2).
$\overline{BR}_{6-1}$	I/O	Multiprocessing Bus Requests. Used by multiprocessing ADSP-2106xs to arbitrate for bus mastership. An ADSP-2106x only drives its own $\overline{BR}$x line (as determined by the value of its ID_{2-0} inputs) and monitors all others. Unused $\overline{BR}$x pins should be tied high.
ID_{2-0}	I	Multiprocessing ID. Determines which multiprocessing bus request ($\overline{BR1}$–$\overline{BR6}$) is used by ADSP-2106x. ID = 001 corresponds to $\overline{BR1}$, ID = 010 corresponds to $\overline{BR2}$, etc., ID = 000 in single-processor systems. These lines are a system configuration selection which should be hardwired.
RPBA	I/S	Rotating Priority Bus Arbitration Select. When RPBA is high, rotating priority for multiprocessor bus arbitration is selected. When RPBA is low, fixed priority is selected. This signal is a system configuration selection which must be set to the same value on every ADSP-2106x. If the value of RPBA is changed during system operation, it must be changed in the same CLKIN cycle on every ADSP-2106x.
$\overline{CPA}$ (o/d)	I/O	Core Priority Access. Asserting its $\overline{CPA}$ pin allows the core processor of an ADSP-2106x bus slave to interrupt background DMA transfers and gain access to the external bus. $\overline{CPA}$ is an open drain output that is connected to all ADSP-2106xs in the system. The $\overline{CPA}$ pin has an internal 5 kΩ pullup resistor. If core access priority is not required in a system, the $\overline{CPA}$ pin should be left unconnected.
DTx	O	Data Transmit (Serial Ports 0, 1). Each DT pin has a 50 kΩ internal pullup resistor.
DRx	I	Data Receive (Serial Ports 0, 1). Each DR pin has a 50 kΩ internal pullup resistor.
TCLKx	I/O	Transmit Clock (Serial Ports 0, 1). Each TCLK pin has a 50 kΩ internal pullup resistor.

Pin Name	Type	Function
RCLKx	I/O	Receive Clock (Serial Ports 0, 1). Each RCLK pin has a 50 kΩ internal pullup resistor.
TFSx	I/O	Transmit Frame Sync (Serial Ports 0, 1).
RFSx	I/O	Receive Frame Sync (Serial Ports 0, 1).
$LxDAT_{3-0}$	I/O	Link Port Data (Link Ports 0–5). Each LxDAT pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
LxCLK	I/O	Link Port Clock (Link Ports 0–5). Each LxCLK pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
LxACK	I/O	Link Port Acknowledge (Link Ports 0–5). Each LxACK pin has a 50 kΩ internal pulldown resistor which is enabled or disabled by the LPDRD bit of the LCOM register.
EBOOT	I	EPROM Boot Select. When EBOOT is high, the ADSP-2106x is set up for booting from an 8-bit EPROM. When EBOOT is low, LBOOT and $\overline{BMS}$ inputs determine booting mode. See table below. This signal is a system configuration selection which should be hardwired.
LBOOT	I	Link Boot—Host Boot Select. When LBOOT is high, the ADSP-2106x is set up for link port booting. When LBOOT is low, the ADSP-2016x is set up for host processor booting. See table below. This signal is a system configuration selection which should be hardwired.
$\overline{BMS}$	I/O/T	Boot Memory Select. Output: Used as chip select for boot EPROM devices (when EBOOT = 1, LBOOT = 0). Input: When low, indicates that no booting will occur and that ADSP-2106x will begin executing instructions from external memory. See table below. This signal is a system configuration selection which should be hardwired. *EBOOT* *LBOOT* *BMS* *Booting Mode* 1 0 output EPROM (connect $\overline{BMS}$ to EPROM chip select) 0 0 1 (input) Host processor 0 1 1 (input) Link port 0 0 0 (input) No booting. Processor executes from external memory. 0 1 0 (input) *Reserved* 1 1 x (input) *Reserved*
CLKIN	I	Clock In. External clock input to the ADSP-2106x. The instruction cycle rate is equal to CLKIN. CLKIN may not be halted, changed, or operated below the specified frequency.
$\overline{RESET}$	I/A	Processor Reset. Resets the ADSP-2106x to a known state and begins execution at the program memory location specified by the hardware reset vector address. This input must be asserted (low) at power-up.
TCK	I	Test Clock (JTAG). Provides an asynchronous clock for JTAG boundary scan.
TMS	I/S	Test Mode Select (JTAG). Used to control the test state machine. TMS has a 20 kΩ internal pullup resistor.
TDI	I/S	Test Data Input (JTAG). Provides serial data for the boundary scan logic. TDI has a 20 kΩ internal pullup resistor.
TDO	O	Test Data Output (JTAG). Serial scan output of the boundary scan path.
$\overline{TRST}$	I/A	Test Reset (JTAG). Resets the test state machine. $\overline{TRST}$ must be asserted (pulsed low) after power-up or held low for proper operation of the ADSP-2106x. $\overline{TRST}$ has a 20 kΩ internal pullup resistor.
$\overline{EMU}$	O	Emulation Status. Must be connected to the ADSP-2106x EZ-ICE target board connector *only*.
ICSA	O	In-Circuit Signal Analyzer.
EVDD	P	External power supply (for output drivers), nominally +5.0 V dc. (18 pins)
EGND	G	External power supply return (for output drivers). (20 pins)
IVDD	P	Internal power supply, nominally +5.0 V dc. (12 pins)
IGND	G	Internal power supply return. (10 pins)

TARGET SYSTEM REQUIREMENTS FOR EZ-ICE

The ADSP-2106x EZ-ICE Emulator uses the IEEE 1149.1 JTAG test access port of the ADSP-2106x to monitor and control the target board processor during emulation. The EZ-ICE probe requires the ADSP-2106x's CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, $\overline{\text{EMU}}$ and GND signals be made accessible on the target system via a 14-pin connector (pin strip header) such as that shown below in Figure 7. The EZ-ICE probe plugs directly onto this connector for chip-on-board emulation. You must add this connector to your target board design if you intend to use the ADSP-2106x EZ-ICE. Be sure to allow enough room in your system to fit the EZ-ICE probe onto the 14-pin connector.

The 14-pin, 2-row pin strip header is keyed at the Pin 3 location—you must remove Pin 3 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The tip of the pins must be at least 0.10 inch higher than the tallest component under the emulator's probe to allow clearance for the bottom of the probe. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

The length of the traces between the EZ-ICE probe connector and the ADSP-2106x's test access port pins should be as short as possible. Note that the EZ-ICE probe adds two TTL loads to the CLKIN pin.

The BTMS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the BXXX pins and the XXX pins as shown in Figure 7. If you are not going to use the test access port for board test, tie $\overline{\text{BTRST}}$ to GND and tie or pullup BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the ADSP-2106x.

Figure 8 shows JTAG scan path connections for systems that contain multiple ADSP-2106x processors.

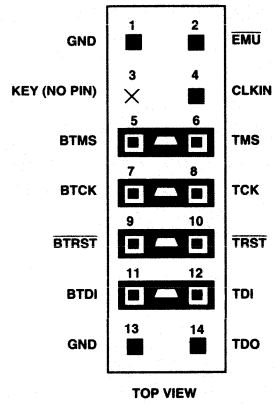


Figure 7. Target Board Connector for ADSP-2106x EZ-ICE Emulator (Jumpers in Place)

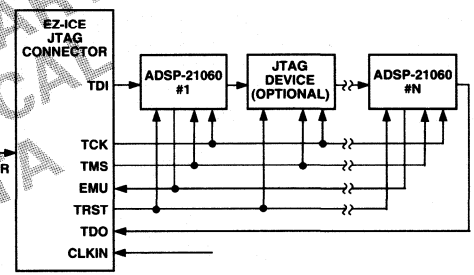


Figure 8. JTAG Scan Path Connections for Multiple ADSP-2106x Systems

ADSP-21060/ADSP-21062–SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	Unit
V_{DD}	Supply Voltage	4.75	5.25	V
T_{AMB}	Ambient Operating Temperature	0	+70	°C

See "Environmental Conditions" for information on thermal specifications.

ELECTRICAL CHARACTERISTICS

Parameter		Test Conditions	Min	Max	Unit
V_{IH}	High Level Input Voltage[1]	@ V_{DD} = max	2.0		V
V_{IHCR}	High Level Input Voltage[2]	@ V_{DD} = max	3.0		V
V_{IL}	Low Level Input Voltage[1]	@ V_{DD} = min		0.8	V
V_{ILCR}	Low Level Input Voltage[2]	@ V_{DD} = min		0.6	V
V_{OH}	High Level Output Voltage[3, 13]	@ V_{DD} = min, I_{OH} = –1.0 mA[14]	2.4		V
V_{OL}	Low Level Output Voltage[3, 13]	@ V_{DD} = min, I_{OL} = 4.0 mA[14]		0.4	V
I_{IH}	High Level Input Current[4]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{IL}	Low Level Input Current[4]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{ILP}	Low Level Input Current[5]	@ V_{DD} = max, V_{IN} = 0 V		350	µA
I_{OZH}	Tristate Leakage Current[6, 8]	@ V_{DD} = max, V_{IN} = V_{DD} max		10	µA
I_{OZL}	Tristate Leakage Current[6, 7]	@ V_{DD} = max, V_{IN} = 0 V		10	µA
I_{OZHP}	Tristate Leakage Current[7]	@ V_{DD} = max, V_{IN} = V_{DD} max		150	µA
I_{OZLP}	Tristate Leakage Current[8]	@ V_{DD} = max, V_{IN} = 0 V		150	µA
I_{DDIN}	Supply Current (Internal)[9]	t_{CK} = 25 ns, V_{DD} = max, V_{IH} = 2.4 V, V_{IHCR} = 3.0 V, V_{IL} = 0.4 V, V_{ILCR} = 0.4 V		800 (Approx)[15]	mA
I_{DDIDLE}	Supply Current (Idle)[10]	V_{DD} = max, V_{IN} = 0 V or V_{DD} max		40 (Approx)	mA
C_{IN}	Input Capacitance[11, 12]	f_{IN} = 1 MHz, T_{CASE} = +25°C, V_{IN} = 2.5 V		7	pF

NOTES

[1]Applies to input and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, $\overline{SW}$, ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $FLAG_{3-0}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR}_{6-1}$, ID_{2-0}, RPBA, $\overline{CPA}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, TMS, TDI

[2]Applies to input pins: CLKIN, $\overline{RESET}$, TCK, $\overline{TRST}$

[3]Applies to output and bidirectional pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, TIMEXP, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR}_{6-1}$, $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$, TDO, $\overline{EMU}$, ICSA

[4]Applies to input pins: ACK, $\overline{SBTS}$, $\overline{IRQ}_{2-0}$, $\overline{HBR}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, ID_{2-0}, RPBA, EBOOT, LBOOT, CLKIN, $\overline{RESET}$, TCK (Note that ACK is pulled up internally during reset in a multiprocessor system, when ID_{2-0} = 001 and one or more $\overline{BR}$x lines are low, i.e., another ADSP-2106x is requesting bus mastership.)

[5]Applies to input pins with internal pullups: DR0, DR1, $\overline{TRST}$, TMS, TDI.

[6]Applies to three-statable pins: $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS}_{3-0}$, $\overline{RD}$, $\overline{WR}$, PAGE, ADRCLK, $\overline{SW}$, ACK, $FLAG_{3-0}$, REDY, $\overline{HBG}$, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BMS}$, TDO, $\overline{EMU}$ (Note that ACK is pulled up internally during reset in a multiprocessor system, when ID_{2-0} = 001 and one or more $\overline{BR}$x lines are low, i.e., another ADSP-2106x is requesting bus mastership.)

[7]Applies to three-statable pins with internal pulldowns: $LxDAT_{3-0}$, LxCLK, LxACK.

[8]Applies to three-statable pins with internal pullups: $\overline{CPA}$, DT0, DT1, TCLK0, TCLK1, RCLK0, RCLK1.

[9]Applies to IVDD pins. See "Power Dissipation" for calculation of external supply current (at EVDD pins) and total supply current.

[10]Applies to IVDD pins. Idle denotes ADSP-2106x state during execution of IDLE instruction.

[11]Applies to all signal pins.

[12]Guaranteed but not tested.

[13]Although specified for TTL outputs, all ADSP-2106x outputs are CMOS-compatible and will drive to VDD and GND assuming no dc loads.

[14]This drive current value is a TTL threshold test condition only—see "Output Drive Currents" for typical drive current capabilities.

[15]Conditions of operation: Executing radix-2 FFT butterfly with instruction in cache, one data operand fetched from each internal memory block, and one DMA transfer occurring from/to internal memory.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . –0.3 V to +7 V
Input Voltage . . . . . –0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . –0.3 V to V_{DD} + 0.3 V
Load Capacitance . . . . . 200 pF
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (5 sec) EDQUAD . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

ESD SENSITIVITY

The ADSP-2106x is an ESD (electrostatic discharge) sensitive device. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur to devices subjected to high energy electrostatic discharges.

The ADSP-2106x processors include proprietary ESD protection circuitry to dissipate high energy discharges. Per method 3015 of MIL-STD-883, the ADSP-2106x processors have been classified as a Class x device (TBD).

Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination before devices are removed.

Preliminary Timing Specifications

GENERAL NOTES

These timing specifications are target specifications based on device simulations only.

Two speed grades of the ADSP-2106x will be offered, 40 MHz and 33.3 MHz. The specifications shown are based on a CLKIN frequency of 40 MHz (t_{CK} = 25 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see "Clock Input" below). DT is the difference between the actual CLKIN period and a CLKIN period of 25 ns:

$$DT = t_{CK} - 25\ ns$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 28 under "Test Conditions" for voltage reference levels.

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

(o/d) = Open Drain

Parameter		40 MHz Min	40 MHz Max	33.3 MHz Min	33.3 MHz Max	Unit
Clock Input						
Timing Requirements:						
t_{CK}	CLKIN Period	25	100	30	100	ns
t_{CKL}	CLKIN Width Low	5		5		ns
t_{CKH}	CLKIN Width High	5		5		ns

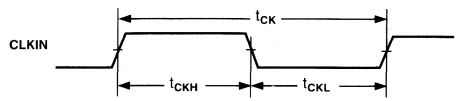


Figure 9. Clock Input

Parameter		Min	Max	Unit
Reset				
Timing Requirements:				
t_{WRST}	$\overline{\text{RESET}}$ Pulse Width Low[1]	$4t_{CK}$		ns
t_{SRST}	$\overline{\text{RESET}}$ Setup before CLKIN High[2]	14 + DT/2	t_{CK}	ns

NOTES
[1]Applies after the powerup sequence is complete. At power up, the processor's internal phase-locked loop requires no more than 2000 CLKIN cycles while $\overline{\text{RESET}}$ is low, assuming stable V_{DD} and CLKIN (not including startup time of external clock oscillator).
[2]Only required if multiple ADSP-2106xs must come out of reset synchronous to CLKIN with program counters (PC) equal (i.e., for a SIMD system). Not required for multiple ADSP-2106xs communicating over the shared bus (through the external port), because the bus arbitration logic synchronizes itself automatically after reset.

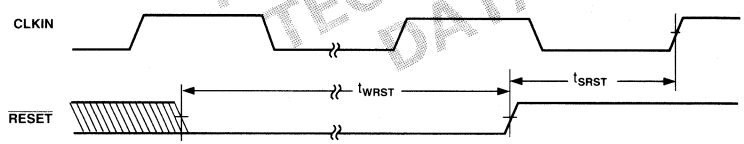


Figure 10. Reset

Parameter		Min	Max	Unit
Interrupts				
Timing Requirements:				
t_{SIR}	$\overline{\text{IRQ2-0}}$ Setup before CLKIN High[1]	20 + 3DT/4		ns
t_{HIR}	$\overline{\text{IRQ2-0}}$ Hold after CLKIN High[1]	0		ns
t_{IPW}	$\overline{\text{IRQ2-0}}$ Pulse Width[2]	$2 + t_{CK}$		ns

NOTES
[1]Only required for $\overline{\text{IRQx}}$ recognition in the following cycle.
[2]Applies only if t_{SIR} and t_{HIR} requirements are not met.

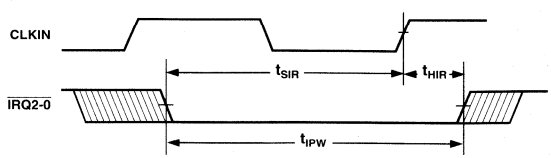


Figure 11. Interrupts

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Parameter		Min	Max	Unit
Timer				
Switching Characteristics:				
t_{DTEX}	CLKIN High to TIMEXP		15	ns

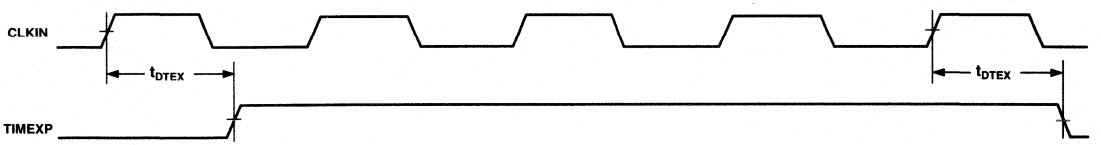


Figure 12. Timer

Parameter		Min	Max	Unit
Flags				
Timing Requirements:				
t_{SFI}	FLAG2–0_{IN} Setup before CLKIN High[1]	7 + 5DT/16		ns
t_{HFI}	FLAG2–0_{IN} Hold after CLKIN High[1]	–2 – 5DT/16		ns
t_{DWRFI}	FLAG2–0_{IN} Delay after $\overline{RD}/\overline{WR}$ Low[1]		0 + 7DT/16	ns
t_{HFIWR}	FLAG2–0_{IN} Hold after $\overline{RD}/\overline{WR}$ Deasserted[1]	0		ns
Switching Characteristics:				
t_{DFO}	FLAG2–0_{OUT} Delay after CLKIN High		14	ns
t_{HFO}	FLAG2–0_{OUT} Hold after CLKIN High	5		ns
t_{DFOE}	CLKIN High to FLAG2–0_{OUT} Enable	3		ns
t_{DFOD}	CLKIN High to FLAG2–0_{OUT} Disable		12	ns

NOTE
[1]Flag inputs meeting these setup and hold times will affect conditional instructions in the following instruction cycle.

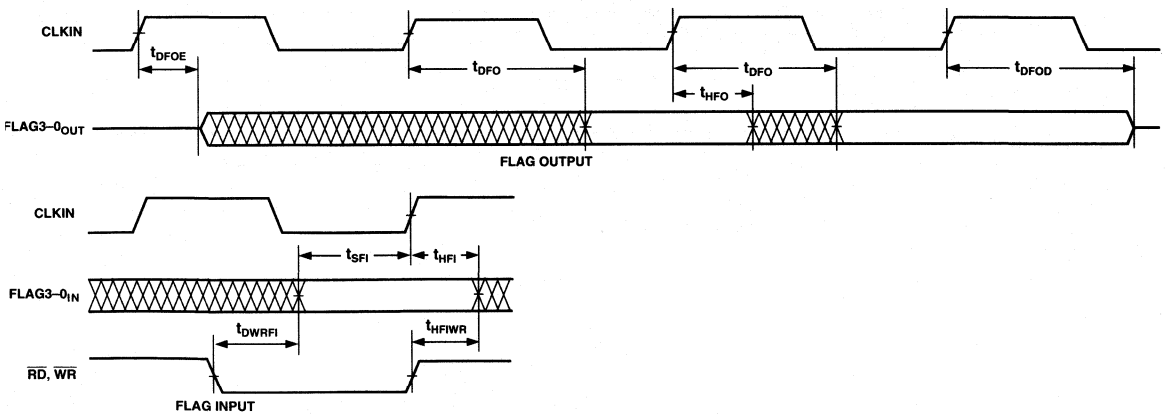


Figure 13. Flags

Memory Read–Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see "Synchronous Read/Write–Bus Master" below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAD}	Address Delay to Data Valid		17 + DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid		10 + 5DT/8 + W	ns
t_{HDA}	Data Hold from Address	0		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High	0		ns
t_{DAAK}	ACK Delay from Address		10 + 7DT/8 +W	ns
Switching Characteristics:				
t_{DARL}	Address to $\overline{RD}$ Low	4 + 3DT/8		ns
t_{RW}	$\overline{RD}$ Pulse Width	14 + 5DT/8 + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	6 + 3DT/8 + HI		ns
t_{SADADC}	Address Setup before ADRCLK High	2 + DT/4		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI=0).

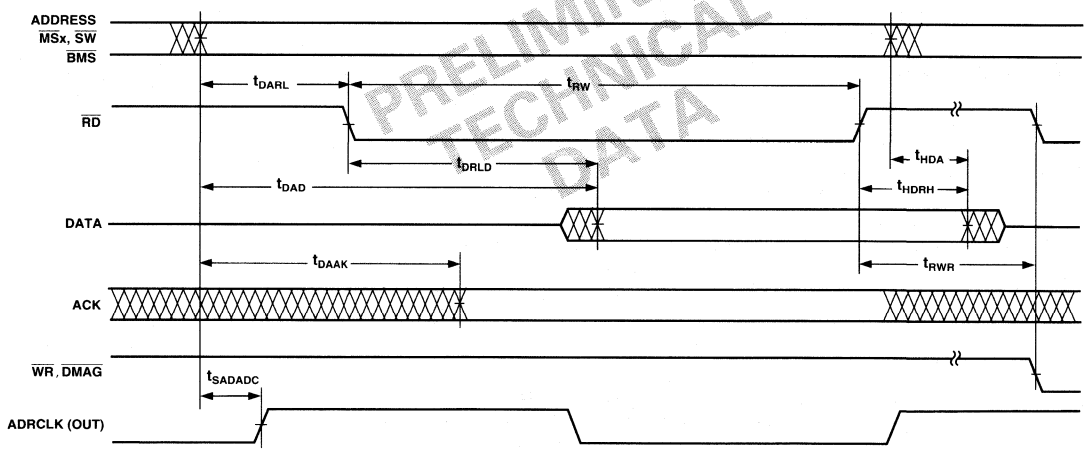


Figure 14. Memory Read—Bus Master

Memory Write–Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-2106x is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see "Synchronous Read/Write–Bus Master" below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa).

Parameter		Min	Max	Unit
Timing Requirements:				
t_{DAAK}	ACK Delay from Address		10 + 7DT/8 +W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted	17 + 15DT/16 +W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low	4 + 3DT/8		ns
t_{WW}	$\overline{WR}$ Pulse Width	12 + 9DT/16 +W		ns
t_{DDWH}	Data Setup before $\overline{WR}$ High	8 + DT/2 +W		ns
t_{DWHA}	Address Hold after $\overline{WR}$ Deasserted	0 + DT/16 + H		ns
t_{DATRWH}	Data Disable after $\overline{WR}$ Deasserted[1]	0 + DT/16 + H	7 + DT/16 + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$, $\overline{DMAG}$x Low	8 + 7DT/16 + HI		ns
t_{DDWR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	7 + 3DT/8 + HI		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	1 + DT/16		ns
t_{SADADC}	Address, Selects to ADRCLK High	2 + DT/4		ns

NOTES

[1]See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and dc loads.

W = (number of wait states specified in WAIT register) × t_{CK}.

H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).

HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).

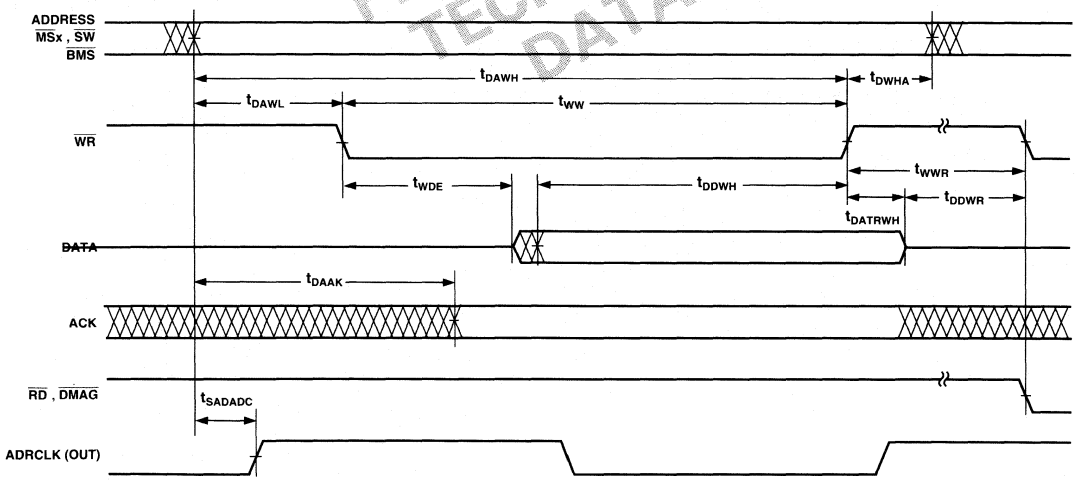


Figure 15. Memory Write—Bus Master

Synchronous Read/Write–Bus Master
Use these specifications for interfacing to external memory systems that require CLKIN-relative timing or for accessing a slave ADSP-2106x (in multiprocessor memory space). These synchronous switching characteristics are also valid during asynchronous memory reads and writes (see "Memory Read–Bus Master" and "Memory Write–Bus Master").

When accessing a slave ADSP-2106x, these switching characteristics must meet the slave's timing requirements for synchronous read/writes (see "Synchronous Read/Write–Bus Slave"). The slave ADSP-2106x must also meet these (bus master) timing requirements for data and acknowledge setup and hold times.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SSDATI}	Data Setup before CLKIN	3 + DT/8		ns
t_{HSDATI}	Data Hold after CLKIN	1 – DT/8		ns
t_{DAAK}	ACK Delay after Address, $\overline{MS}$x, $\overline{SW}$, $\overline{BMS}$		10 + 7 DT/8	ns
t_{SACKC}	ACK Setup before CLKIN	6 + DT/4		ns
t_{HACKI}	ACK Hold after CLKIN	–1 – DT/4		ns
Switching Characteristics:				
t_{DADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Delay after CLKIN		8 – DT/8	ns
t_{HADRO}	Address, $\overline{MS}$x, $\overline{BMS}$, $\overline{SW}$ Hold after CLKIN	2 – DT/8		ns
t_{DPGC}	PAGE Delay after CLKIN		14 + DT/8	ns
t_{DRDO}	$\overline{RD}$ High Delay after CLKIN	0 – DT/8	4 – DT/8	ns
t_{DWRO}	$\overline{WR}$ High Delay after CLKIN	0 – 3DT/16	4 – 3DT/16	ns
t_{DRWL}	$\overline{RD}$/$\overline{WR}$ Low Delay after CLKIN	9 + DT/4	14 + DT/4	ns
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[1]	0 – DT/8	7 – DT/8	ns
t_{DADCCK}	ADRCLK Delay after CLKIN	7 + DT/8	12 + DT/8	ns
t_{ADRCK}	ADRCLK Period	t_{CK}		ns
t_{ADRCKH}	ADRCLK Width High	(t_{CK}/2 – 3)		ns
t_{ADRCKL}	ADRCLK Width Low	(t_{CK}/2 – 3)		ns

NOTE
[1]See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and dc loads.

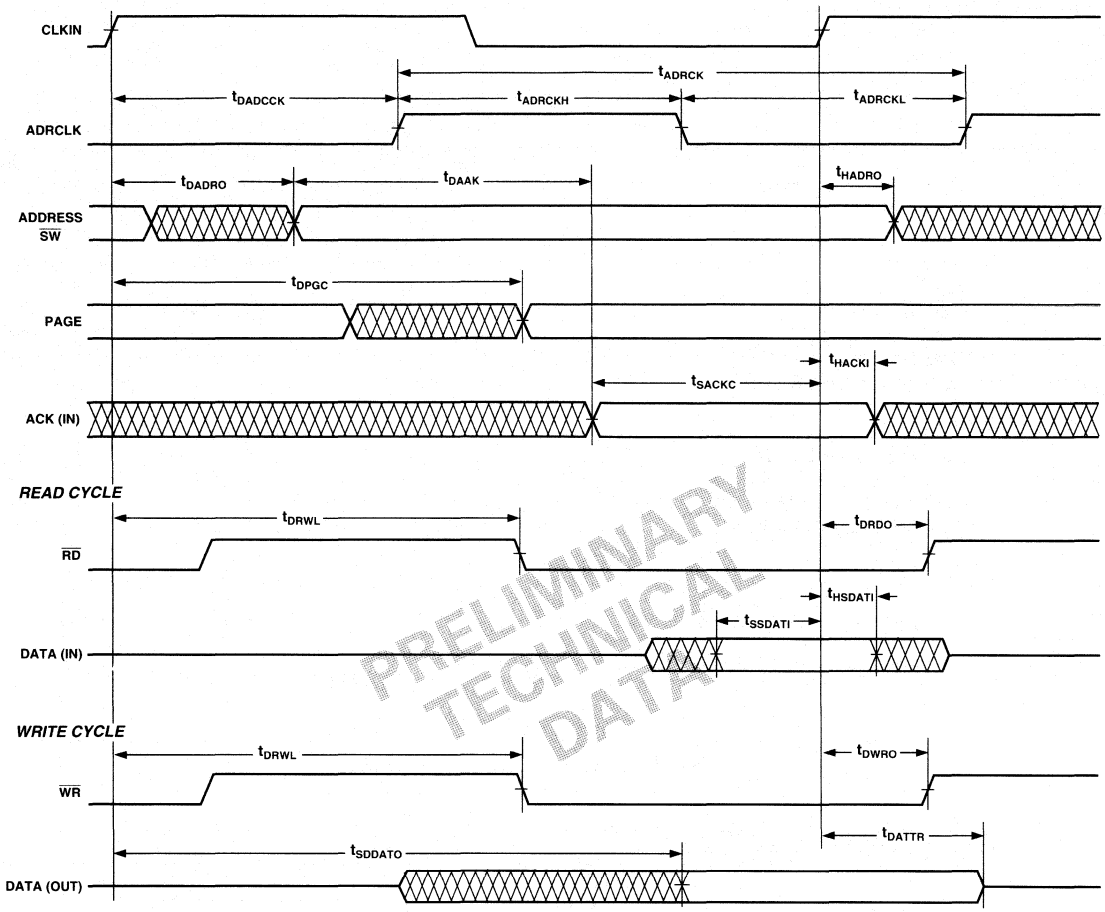


Figure 16. Synchronous Read/Write—Bus Master

Synchronous Read/Write–Bus Slave
Use these specifications for ADSP-2106x bus master accesses of a slave's IOP registers or internal memory (in multiprocessor memory space). The bus master must meet these (bus slave) timing requirements.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SADRI}	Address, $\overline{SW}$ Setup before CLKIN	13 + DT/2		ns
t_{HADRI}	Address, $\overline{SW}$ Hold before CLKIN		6 + DT/2	ns
t_{SRWLI}	$\overline{RD}/\overline{WR}$ Low Setup before CLKIN[1]	8 + 5DT/16		ns
t_{HRWLI}	$\overline{RD}/\overline{WR}$ Low Hold after CLKIN[2]	–3 – 5DT/16	5 + 7DT/16	ns
t_{RWHPI}	$\overline{RD}/\overline{WR}$ Pulse High	3		ns
t_{SDATWH}	Data Setup before $\overline{WR}$ High	3		ns
t_{HDATWH}	Data Hold after $\overline{WR}$ High	0		ns
Switching Characteristics:				
t_{SDDATO}	Data Delay after CLKIN		19 + 5DT/16	ns
t_{DATTR}	Data Disable after CLKIN[3]	0 – DT/8	7 – DT/8	ns
t_{DACKAD}	ACK Delay after Address, $\overline{SW}$[4]		8	ns
t_{ACKTR}	ACK Disable after CLKIN[3]	0 – DT/8	7 – DT/8	ns

NOTES
[1]t_{SRWLI} (min) = 8 + 5DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{SRWLI} (min) = 4 + DT/8.
[2]t_{HRWLI} (max) = 5 + 7DT/16 when Multiprocessor Memory Space Wait State (MMSWS bit in WAIT register) is disabled; when MMSWS is enabled, t_{HRWLI} (min) = 7 + 7DT/16.
[3]See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and dc loads.
[4]t_{DACKAD} is true only if the address and $\overline{SW}$ inputs have setup times (before CLKIN) greater than 10 + DT/8 and less than 19 + 3DT/4. Otherwise ACK is valid 14 + DT/4 (max) after CLKIN.

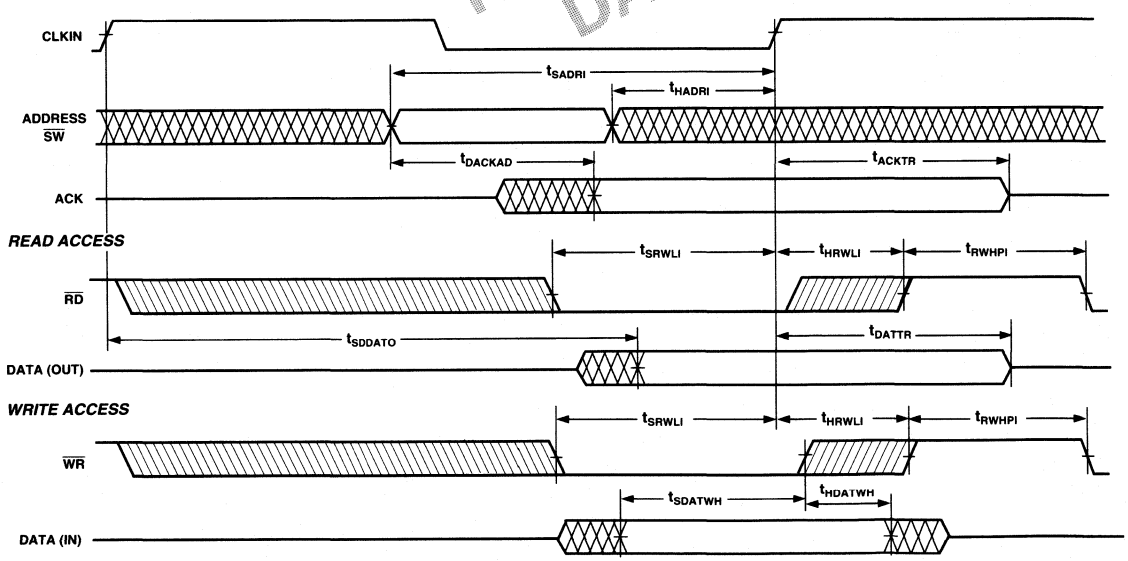


Figure 17. Synchronous Read/Write—Bus Slave

Multiprocessor Bus Request & Host Bus Request
Use these specifications for passing of bus mastership between multiprocessing ADSP-2106xs ($\overline{BR}$x) or asynchronous takeover of the bus by a host processor ($\overline{HBR}$, $\overline{HBG}$).

Parameter		Min	Max	Unit
Timing Requirements:				
$t_{HBGRCSV}$	$\overline{HBG}$ Low to $\overline{RD}$/$\overline{WR}$/$\overline{CS}$ Valid		20 + 5DT/4	ns
t_{SHBRI}	$\overline{HBR}$ Setup before CLKIN[1]	20 + 3DT/4		ns
t_{HHBRI}	$\overline{HBR}$ Hold before CLKIN[1]		15 + 3DT/4	ns
t_{SHBGI}	$\overline{HBG}$ Setup before CLKIN	13 + DT/2		ns
t_{SBRI}	$\overline{BR}$x, $\overline{CPA}$ Setup before CLKIN	13 + DT/2		ns
t_{SRPBAI}	RPBA Setup before CLKIN	18 + 3DT/4		ns
t_{HRPBAI}	RPBA Hold before CLKIN		13 + 3DT/4	ns
Switching Characteristics:				
t_{DHBGO}	$\overline{HBG}$ Delay after CLKIN		6 – DT/8	ns
t_{HHBGO}	$\overline{HBG}$ Hold after CLKIN	0 – DT/8		ns
t_{DBRO}	$\overline{BR}$x Delay after CLKIN		6 – DT/8	ns
t_{HBRO}	$\overline{BR}$x Hold after CLKIN	0 – DT/8		ns
t_{DCPAO}	$\overline{CPA}$ Low Delay after CLKIN		6 – DT/8	ns
t_{TRCPA}	$\overline{CPA}$ Disable after CLKIN	–2 – DT/8	3 – DT/8	ns
t_{DRDYCS}	REDY Low from $\overline{CS}$ and $\overline{HBR}$ Low		8	ns
t_{TRDYHG}	REDY Disable from $\overline{HBG}$	35 + 27DT/16		ns

NOTE: [1]Only required for recognition in the current cycle.

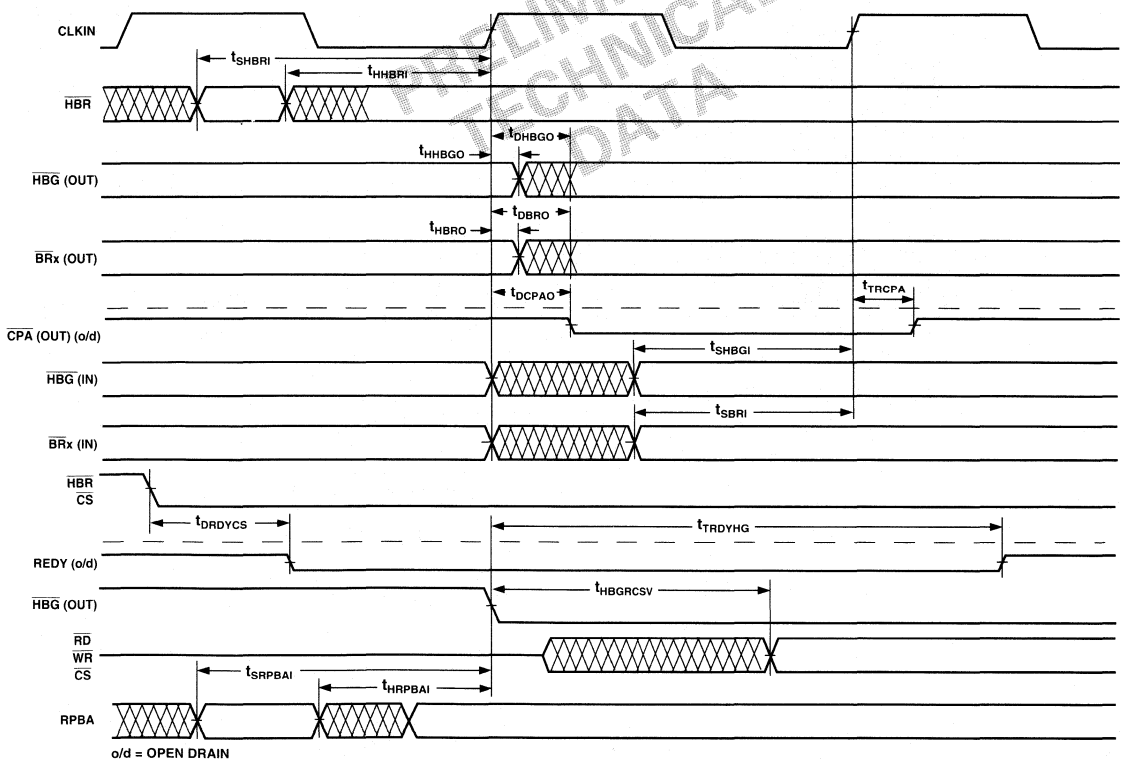


Figure 18. Multiprocessor Bus Request & Host Bus Request

Asynchronous Read/Write–Host to ADSP-2106x
Use these specifications for asynchronous host processor accesses of an ADSP-2106x, after the host has asserted $\overline{CS}$ and $\overline{HBR}$ (low). After $\overline{HBG}$ is returned by the ADSP-2106x, the host can drive the $\overline{RD}$ and $\overline{WR}$ pins to access the ADSP-2106x's internal memory or IOP registers.

Parameter		Min	Max	Unit
Read Cycle				
Timing Requirements:				
t_{SADRDL}	Address Setup before $\overline{RD}/\overline{CS}$ Low	0		ns
t_{HADRDH}	Address Hold after $\overline{RD}/\overline{CS}$ High	0		ns
t_{WRWH}	$\overline{RD}/\overline{WR}/\overline{CS}$ High Width	6		ns
$t_{DRDHRDY}$	$\overline{RD}/\overline{CS}$ High Delay after REDY Disable	0		ns
Switching Characteristics:				
$t_{SDATRDY}$	Data Valid before REDY Disable from Low	2		ns
$t_{DRDYRDL}$	REDY Low Delay after $\overline{RD}/\overline{CS}$ Low		8	ns
t_{RDYPRD}	REDY Low Pulse Width for Read	35 + DT		ns
t_{HDARWH}	Data Hold Delay $\overline{RD}/\overline{CS}$ High	0	7	ns
Write Cycle				
Timing Requirements:				
t_{SADWRH}	Address Setup before $\overline{WR}/\overline{CS}$ High	6		ns
t_{HADWRH}	Address Hold after $\overline{WR}/\overline{CS}$ High	0		ns
t_{WWRL}	$\overline{WR}/\overline{CS}$ Low Width	10		ns
t_{WRWH}	$\overline{RD}/\overline{WR}/\overline{CS}$ High Width	6		ns
$t_{DWRHRDY}$	$\overline{WR}/\overline{CS}$ High Delay after REDY Disable	0		ns
t_{SDATWH}	Data Setup before $\overline{WR}/\overline{CS}$ High	3		ns
t_{HDATWH}	Data Hold after $\overline{WR}/\overline{CS}$ High	0		ns
Switching Characteristics:				
$t_{DRDYWRL}$	REDY Low Delay after $\overline{WR}/\overline{CS}$ Low		8	ns
t_{RDYPWR}	REDY Low Pulse Width for Write	6		ns
t_{SRDYCK}	REDY Disable to CLKIN	3 + 7DT/16	10 + 7DT/16	ns

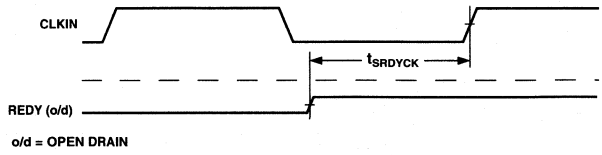


Figure 19a. Synchronous REDY Timing

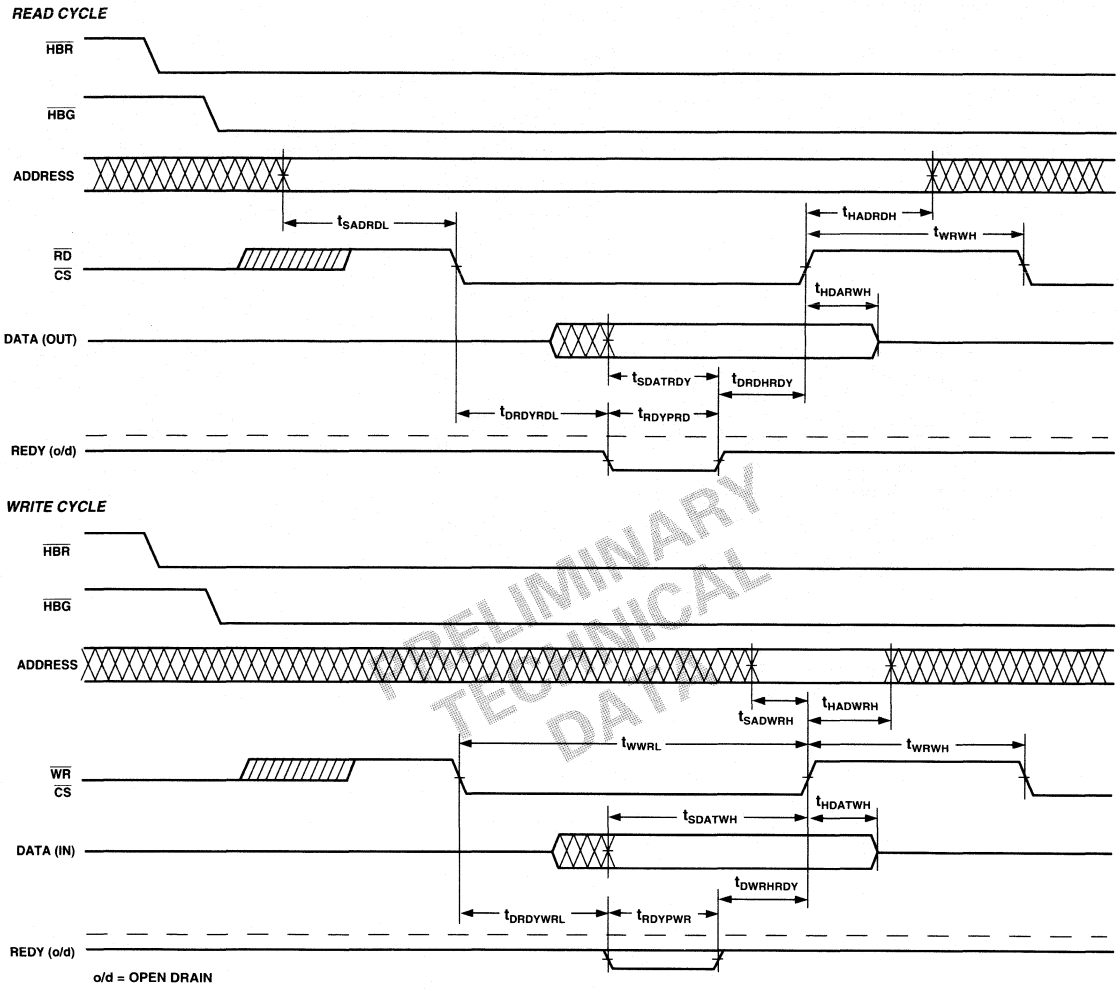


Figure 19b. Asynchronous Read/Write—Host to ADSP-2106x

Three-State Timing —Bus Master, Bus Slave, $\overline{\text{HBR}}$, $\overline{\text{SBTS}}$
These specifications show how the memory interface is disabled (stops driving) or enabled (resumes driving) relative to CLKIN and the $\overline{\text{SBTS}}$ pin. This timing is applicable to bus master transition cycles (BTC) and host transition cycles (HTC) as well as the $\overline{\text{SBTS}}$ pin.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{STSCK}	$\overline{\text{SBTS}}$ Setup before CLKIN	13 + DT/2		ns
t_{HTSCK}	$\overline{\text{SBTS}}$ Hold before CLKIN		6 + DT/2	ns
Switching Characteristics:				
t_{MIEN}	Memory Interface Enable after CLKIN	0 – DT/8		ns
t_{MITR}	Memory Interface Disable after CLKIN		0 – DT/4	ns
t_{DATEN}	Data Enable after CLKIN	16 + 5DT/16		ns
t_{DATTR}	Data Disable after CLKIN	0 – DT/8	7 – DT/8	ns
t_{ACKEN}	ACK Enable after CLKIN	8 + DT/4		ns
t_{ACKTR}	ACK Disable after CLKIN	0 – DT/8	7 – DT/8	ns
t_{ADCEN}	ADRCLK Enable after CLKIN	2 – DT/8		ns
t_{ADCTR}	ADRCLK Disable after CLKIN		0 – DT/4	ns
t_{MTRHBG}	Memory Interface* Disable before $\overline{\text{HBG}}$ Low	0 + DT/8		ns
t_{MENHBG}	Memory Interface* Enable after $\overline{\text{HBG}}$ High	18 + DT		ns

*Memory Interface = Address, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{MS}}$x, $\overline{\text{SW}}$, $\overline{\text{HBG}}$, PAGE, $\overline{\text{DMAG}}$x.

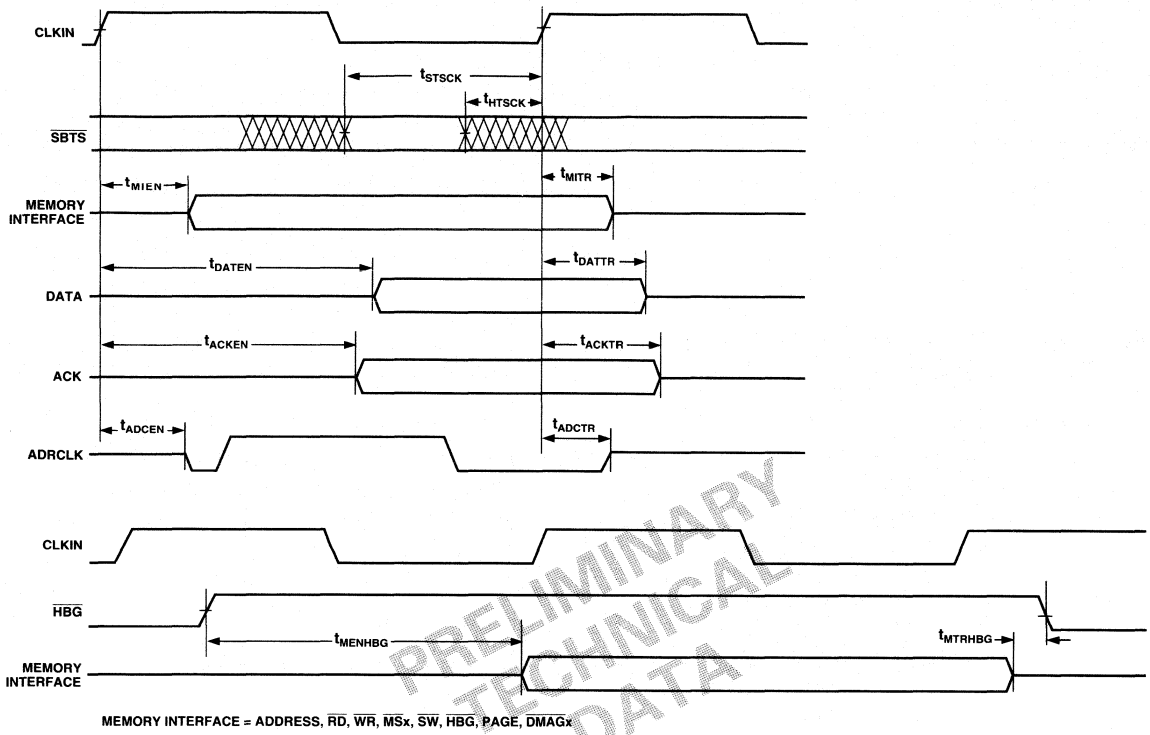


Figure 20. Three-State Timing

DMA Handshake

These specifications show how DMA handshaking uses the $\overline{\text{DMAR}}$x and $\overline{\text{DMAG}}$x signals to control each DMA transfer, word-by-word. DMA handshaking is enabled by the HSHAKE bit of DMA control registers DMAC6–9.

Parameter		Min	Max	Unit
Timing Requirements:				
t_{SDRLC}	$\overline{\text{DMAR}}$x Low Setup before CLKIN[1]	5		ns
t_{SDRHC}	$\overline{\text{DMAR}}$x High Setup before CLKIN[1]	5		ns
t_{WDR}	$\overline{\text{DMAR}}$x Width Low (Nonsynchronous)	6		ns
$t_{SDATDGL}$	Data Setup after $\overline{\text{DMAG}}$x Low[2]		10 + 5DT/8	ns
$t_{HDATIDG}$	Data Hold after $\overline{\text{DMAG}}$x High	0		ns
t_{DATDRH}	Data Valid after $\overline{\text{DMAR}}$x High[2]		16 + 7DT/8	ns
t_{DMARLL}	$\overline{\text{DMAR}}$x Low Edge to Low Edge	23 + 7DT/8		ns
t_{DMARH}	$\overline{\text{DMAR}}$x Width High	6		ns
Switching Characteristics:				
t_{DDGL}	$\overline{\text{DMAG}}$x Low Delay after CLKIN	10 + DT/4	16 + DT/4	ns
t_{WDGH}	$\overline{\text{DMAG}}$x High Width	6 + 3DT/8		ns
t_{WDGL}	$\overline{\text{DMAG}}$x Low Width	12 + 5DT/8		ns
t_{HDGC}	$\overline{\text{DMAG}}$x High Delay after CLKIN	1 – DT/8	7 – DT/8	ns
$t_{VDATDGH}$	Data Valid before $\overline{\text{DMAG}}$x High[3]	8 + 9DT/16		ns
$t_{DATRDGH}$	Data Disable after $\overline{\text{DMAG}}$x High[4]	0	7	ns
t_{DGWRF}	$\overline{\text{WR}}$ Low before $\overline{\text{DMAG}}$x Low	0	2	ns
t_{DGWRH}	$\overline{\text{DMAG}}$x Low before $\overline{\text{WR}}$ High	12 + 5DT/8 + W		ns
t_{DGWRR}	$\overline{\text{WR}}$ High before $\overline{\text{DMAG}}$x High	1 + DT/16	4 + DT/16	ns
t_{DGRDF}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x Low	0	2	ns
t_{DRDGH}	$\overline{\text{RD}}$ Low before $\overline{\text{DMAG}}$x High	13 + 9DT/16 + W		ns
t_{DGRDR}	$\overline{\text{RD}}$ High before $\overline{\text{DMAG}}$x High	0	2	ns

NOTES

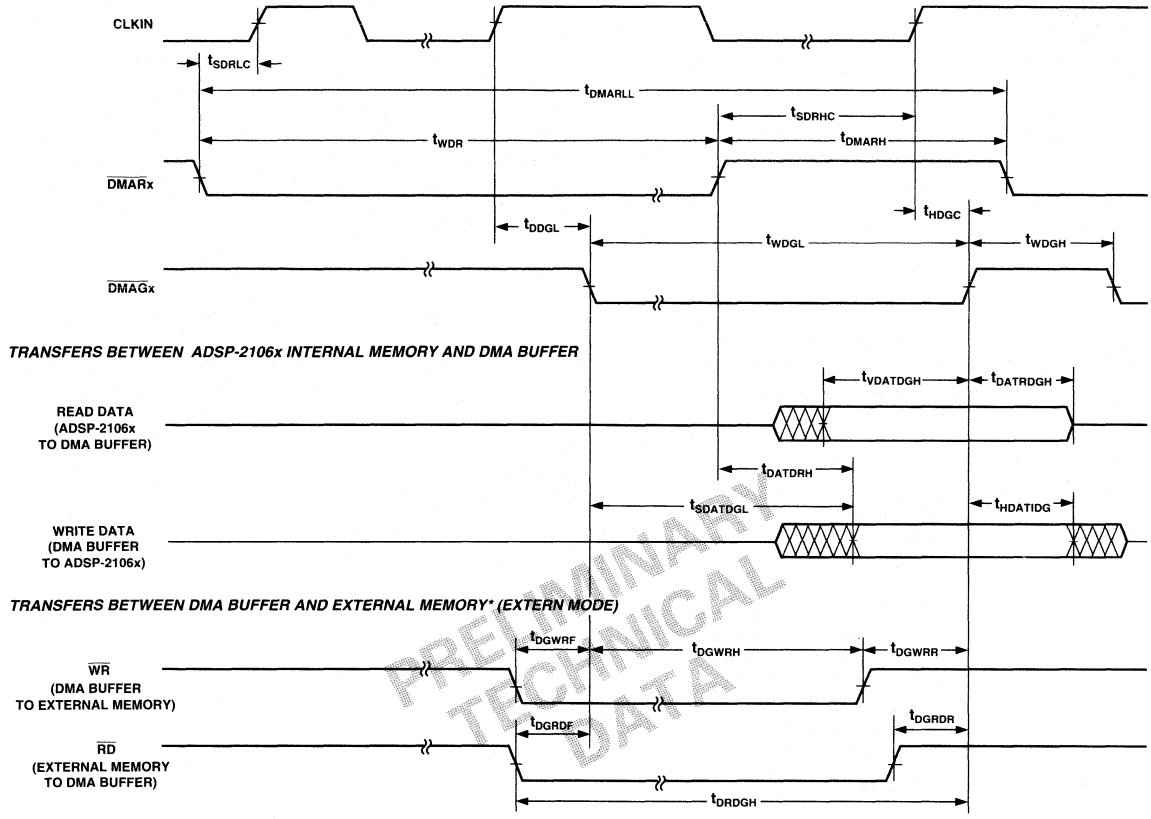
W = (number of wait states specified in WAIT register) × t_{CK}.

[1]Only required for recognition in the current cycle.

[2]$t_{SDATDGL}$ is the data setup requirement if $\overline{\text{DMAR}}$x is not being used to hold off completion of a write. Otherwise, if $\overline{\text{DMAR}}$x low holds off completion of the write, the data can be driven t_{DATDRH} after $\overline{\text{DMAR}}$x is brought high.

[3]$t_{VDATDGH}$ is valid if $\overline{\text{DMAR}}$x is not being used to hold off completion of a read. If $\overline{\text{DMAR}}$x is used to prolong the read, then $t_{VDATDGH}$ = 8 + 9DT/16 + (n • t_{CK}) where n equals the number of extra cycles that the access is prolonged.

[4]See "System Hold Time Calculation" under "Test Conditions" for calculation of hold times given capacitive and dc loads.



* "MEMORY READ–BUS MASTER," "MEMORY WRITE–BUS MASTER," AND "SYNCHRONOUS READ/WRITE–BUS MASTER" TIMING SPECIFICATIONS FOR ADDR31–0, RD, WR, MS3-0 AND ACK ALSO APPLY HERE.

Figure 21. DMA Handshake Timing

Link Ports

Parameter		Min	Max	Unit
Receive				
Timing Requirements:				
t_{SLDCL}	Data Setup before LCLK Low	3		ns
t_{HLDCL}	Data Hold after LCLK Low	2		ns
t_{LCLKIW}	LCLK Period (1x Operation)	t_{CK}		ns
t_{LCLKIW}	LCLK Period (2x Operation)	$t_{CK}/2$		ns
t_{LCLKRW}	LCLK Width	5		ns
Switching Characteristics:				
t_{DLAHCI}	LACK High Delay after CLKIN High	18 + DT/2	27 + DT/2	ns
t_{DLALC}	LACK Low Delay after LCLK High	7	13	ns
t_{ENDLK}	LACK Enable from CLKIN	5 + DT/2		ns
t_{TDLK}	LACK Disable from CLKIN		23 + DT/2	ns
Transmit				
Timing Requirements:				
t_{SLACH}	LACK Setup before LCLK High		13	ns
t_{HLACH}	LACK Hold after LCLK High	7		ns
Switching Characteristics:				
t_{DLCLK}	LCLK Delay after CLKIN (1x Operation)		8	ns
t_{DLCLK}	LCLK Delay after CLKIN (2x Operation)		12	ns
t_{DLDCH}	Data Delay after LCLK High		2	ns
t_{HLDCH}	Data Hold after LCLK High	– 2		ns
t_{LCLKTW}	LCLK Width (1x Operation)	$(t_{CK}/2) - 2$	$(t_{CK}/2) + 2$	ns
t_{LCLKTW}	LCLK Width (2x Operation)	$(t_{CK}/4) - 2$	$(t_{CK}/4) + 2$	ns
t_{DLACLK}	LCLK Low Delay after LACK High	$(t_{LCLKTW}/2) + 11$	$(3 \times t_{LCLKTW}/2) + 11$	ns
Link Port Service Request Interrupts				
Timing Requirements:				
t_{SLCK}	LACK/LCLK Setup before CLKIN Low*	2		ns
t_{HLCK}	LACK/LCLK Hold after CLKIN Low*	6		ns

*Only required for interrupt recognition in the current cycle.

LINK PORT INTERRUPT SETUP TIME

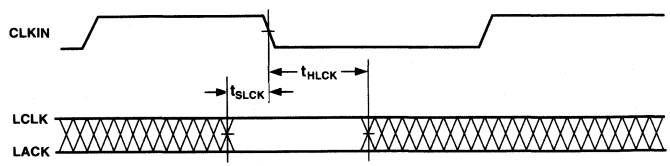
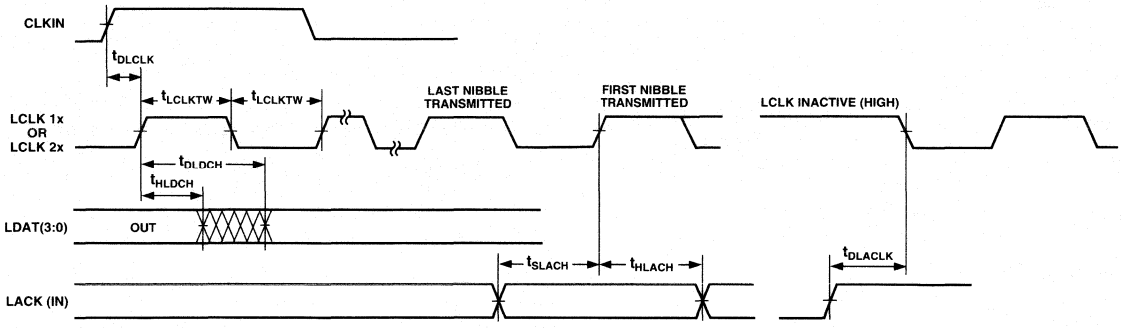


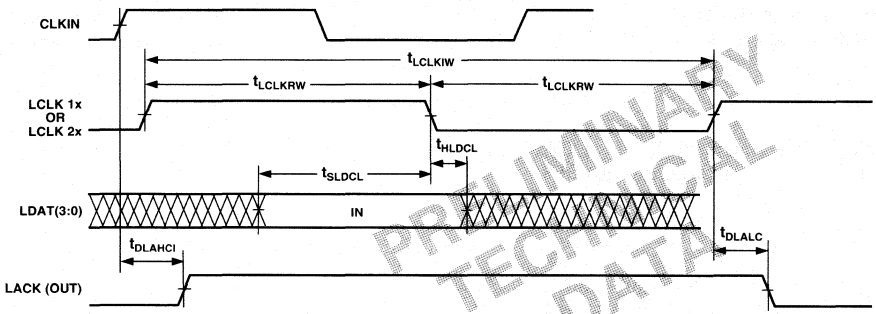
Figure 22a. Link Port Interrupts

TRANSMIT



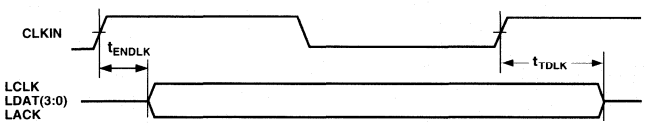
THE t_{SLACH} REQUIREMENT APPLIES TO THE RISING EDGE OF LCLK ONLY FOR THE FIRST NIBBLE TRANSMITTED.

RECEIVE



LACK GOES LOW ONLY AFTER THE SECOND NIBBLE IS RECEIVED.

LINK PORT ENABLE/THREE-STATE DELAY FROM INSTRUCTION



LINK PORT ENABLE OR THREE-STATE TAKES EFFECT 2 CYCLES AFTER A WRITE TO A LINK PORT CONTROL REGISTER.

Figure 22b. Link Ports

Serial Ports

Parameter		Min	Max	Unit
External Clock				
Timing Requirements:				
t_{SFSE}	TFS/RFS Setup before TCLK/RCLK	3		ns
t_{HFSE}	TFS/RFS Hold after TCLK/RCLK		3	ns
t_{SDRE}	Receive Data Setup before RCLK	3		ns
t_{HDRE}	Receive Data Hold after RCLK		3	ns
t_{SCLKW}	TCLK/RCLK Width	10		ns
t_{SCLK}	TCLK/RCLK Period	t_{CK}		ns
Internal Clock				
Timing Requirements:				
t_{SFSI}	TFS Setup before TCLK	7		ns
t_{SFSI}	RFS Setup before RCLK	7		ns
t_{HFSI}	TFS/RFS Hold after TCLK/RCLK		– 3	ns
t_{SDRI}	Receive Data Setup before RCLK	7		ns
t_{HDRI}	Receive Data Hold after RCLK		– 3	ns
External or Internal Clock				
Switching Characteristics:				
t_{DFSE}	RFS Delay after RCLK (Internally Generated RFS)		10	ns
t_{HOFSE}	RFS Hold after RCLK (Internally Generated RFS)	6		ns
External Clock				
Switching Characteristics:				
t_{DFSE}	TFS Delay after TCLK (Internally Generated TFS)		10	ns
t_{HFSE}	TFS Hold after TCLK (Internally Generated TFS)	6		ns
t_{DDTE}	Transmit Data Delay after TCLK		10	ns
t_{HODTE}	Transmit Data Hold after TCLK	6		ns
Internal Clock				
Switching Characteristics:				
t_{DFSI}	TFS Delay after TCLK (Internally Generated TFS)		4	ns
t_{HOFSI}	TFS Hold after TCLK (Internally Generated TFS)	0		ns
t_{DDTI}	Transmit Data Delay after TCLK		4	ns
t_{HDTI}	Transmit Data Hold after TCLK	0		ns
t_{SCLKW}	TCLK/RCLK Width	(SCLK/2) – 3	(SCLK/2) + 3	ns
Enable & Three-State				
Switching Characteristics:				
t_{DDTEN}	DT Enable Delay from Ext. TCLK or "Late" Ext. TFS	5		ns
t_{DDTTE}	DT Disable Delay from External TCLK		12	ns
t_{DDTIN}	DT Enable Delay from Int. TCLK or "Late" Int. TFS	2		ns
t_{DDTTI}	DT Disable Delay from Internal TCLK		5	ns
t_{DCLK}	TCLK/RCLK Delay from CLKIN		10	ns
t_{DPTR}	SPORT Disable after CLKIN		15	ns
Gated SCLK with External TFS (Mesh Multiprocessing)*				
Timing Requirements:				
t_{STFSCK}	TFS Setup before CLKIN	5		ns
t_{HTFSCK}	TFS Hold after CLKIN	$t_{CK}/2$		ns

*Applies only to gated serial clock mode used for serial port system I/O in mesh multiprocessing systems; see User's Manual.

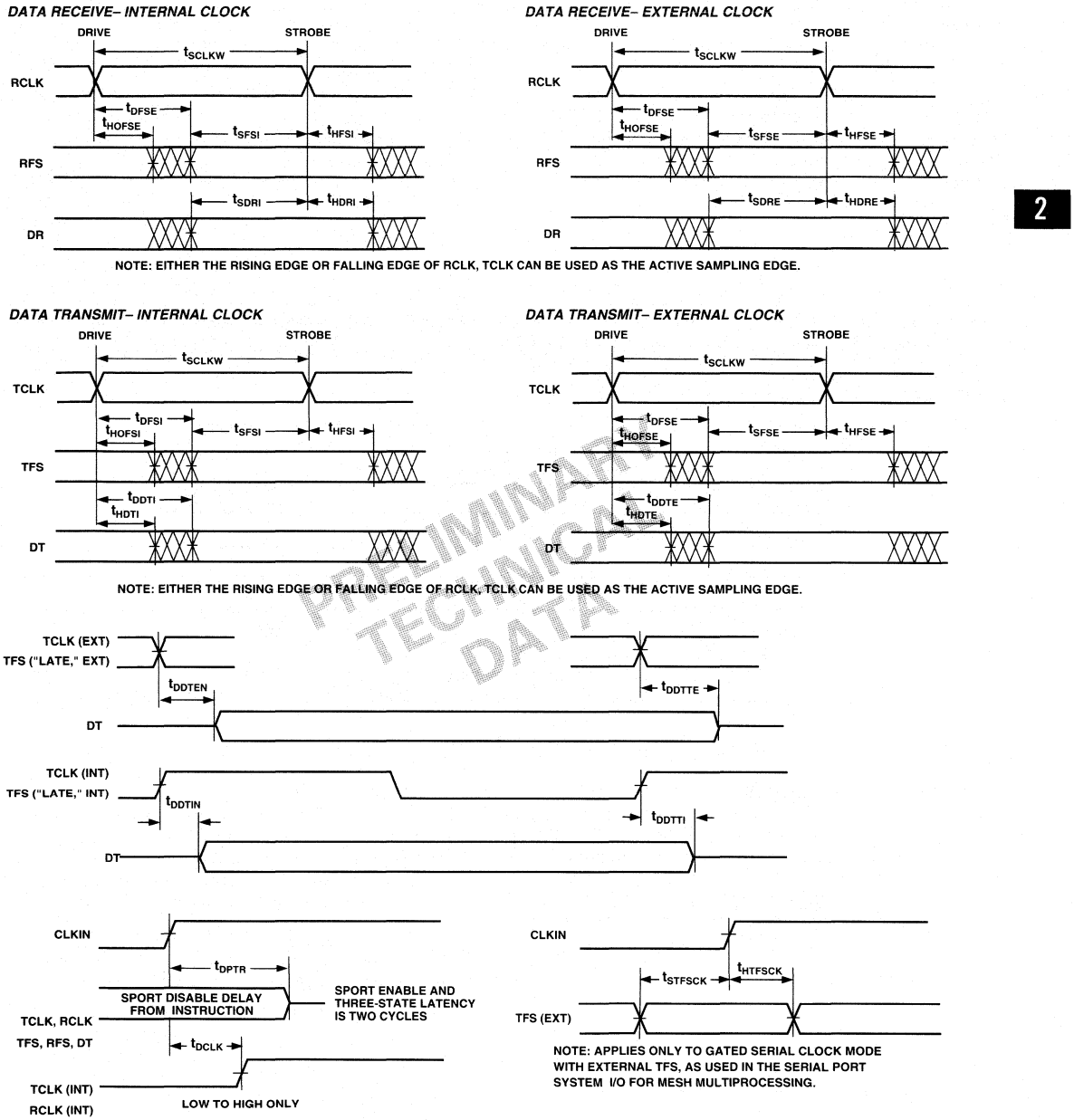


Figure 23. Serial Ports

JTAG Test Access Port & Emulation

Parameter		Min	Max	Unit
Timing Requirements:				
t_{TCK}	TCK Period	t_{CK}		ns
t_{STAP}	TDI, TMS Setup before TCK High	5		ns
t_{HTAP}	TDI, TMS Hold after TCK High	6		ns
t_{SSYS}	System Inputs Setup before TCK High*	7		ns
t_{HSYS}	System Inputs Hold after TCK High*	9		ns
t_{TRSTW}	$\overline{TRST}$ Pulse Width	$4t_{CK}$		ns
Switching Characteristics:				
t_{DTDO}	TDO Delay from TCK Low		10	ns
t_{DSYS}	System Outputs Delay after TCK Low**		18	ns

*System Inputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{RD}$, $\overline{WR}$, ACK, $\overline{SBTS}$, $\overline{SW}$, $\overline{HBR}$, $\overline{HBG}$, $\overline{CS}$, $\overline{DMAR1}$, $\overline{DMAR2}$, $\overline{BR_{6-1}}$, ID_{2-0}, RPBA, $\overline{IRQ_{2-0}}$, $FLAG_{3-0}$, DR0, DR1, TCLK0, TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, EBOOT, LBOOT, $\overline{BMS}$, CLKIN, $\overline{RESET}$.

**System Outputs = $DATA_{47-0}$, $ADDR_{31-0}$, $\overline{MS_{3-0}}$, $\overline{RD}$, $\overline{WR}$, ACK, PAGE, ADRCLK, $\overline{SW}$, $\overline{HBG}$, REDY, $\overline{DMAG1}$, $\overline{DMAG2}$, $\overline{BR_{6-1}}$, $\overline{CPA}$, $FLAG_{3-0}$, TIMEXP, DT0, DT1, TCLK0 TCLK1, RCLK0, RCLK1, TFS0, TFS1, RFS0, RFS1, $LxDAT_{3-0}$, LxCLK, LxACK, $\overline{BMS}$.

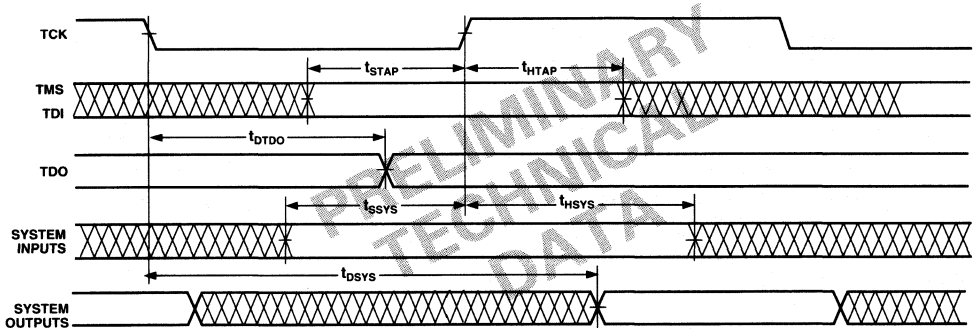


Figure 24. IEEE 1149.1 JTAG Test Access Port

OUTPUT DRIVE CURRENTS

Figure 25 shows typical I-V characteristics for the output drivers of the ADSP-2106x. The curves represent the current drive capability of the output drivers as a function of output voltage.

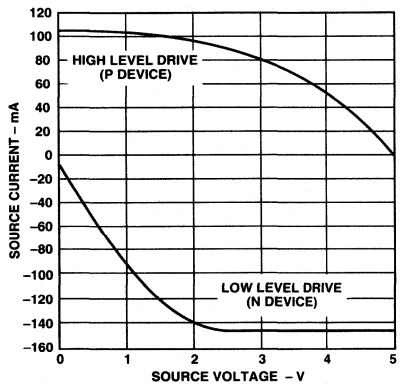


Figure 25. ADSP-2106x Typical Drive Currents

POWER DISSIPATION

Total power dissipation has two components, one due to internal circuitry and one due to the switching of external output drivers. Internal power dissipation is dependent on the instruction execution sequence and the data operands involved. Internal power dissipation is calculated in the following way:

$$P_{INT} = I_{DDIN} \times V_{DD}$$

The external component of total power dissipation is caused by the switching of output pins. Its magnitude depends on:

- the number of output pins that switch during each cycle (O)
- the maximum frequency at which they can switch (f)
- their load capacitance (C)
- their voltage swing (V_{DD})

and it is calculated by:

$$P_{EXT} = O \times C \times V_{DD}^2 \times f$$

The load capacitance should include the processor's package capacitance (C_{IN}). The switching frequency includes driving the load high and then back low. Address and data pins can drive

high and low at a maximum rate of $1/(2t_{CK})$. The write strobe can switch every cycle at a frequency of $1/t_{CK}$. Select pins switch at $1/(2t_{CK})$, but selects can switch on each cycle.

Example:

Estimate P_{EXT} with the following assumptions:

– a system with one bank of external data memory RAM (32-bit)

– four 128K x 8 RAM chips are used, each with a load of 10 pF

– external data memory writes occur every other cycle, a rate of $1/(4t_{CK})$, with 50% of the pins switching

– the instruction cycle rate is 40 MHz (t_{CK} = 25 ns) and V_{DD} = 5.0 V

The P_{EXT} equation is calculated for each class of pins that can drive:

Pin Type	# of Pins	% Switching	× C	× f	× V_{DD}^2	= P_{EXT}
Address	15	50%	× 47 pF	× 10 MHz	× 25 V	= 0.088 W
$\overline{MS0}$	1	0%	× 47 pF	× 10 MHz	× 25 V	= 0.000 W
$\overline{WR}$	1	–	× 47 pF	× 20 MHz	× 25 V	= 0.023 W
Data	32	50%	× 17 pF	× 10 MHz	× 25 V	= 0.068 W

P_{EXT} = 0.179 W

A typical power consumption can now be calculated for these conditions by adding a typical internal power dissipation:

$$P_{TOTAL} = P_{EXT} + (I_{DDIN} \times 5.0\ V)$$

Note that the conditions causing a worst-case P_{EXT} are different from those causing a worst-case P_{INT}. Maximum P_{INT} cannot occur while 100% of the output pins are switching from all ones to all zeros. Also note that it is not common for an application to have 100% or even 50% of the outputs switching simultaneously.

TEST CONDITIONS

Output Disable Time

Output pins are considered to be disabled when they stop driving, go into a high-impedance state, and start to decay from their output high or low voltage. The time for the voltage on the bus to decay by ΔV is dependent on the capacitive load, C_L, and the load current, I_L. This decay time can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \Delta V}{I_L}$$

The output disable time t_{DIS} is the difference between $t_{MEASURED}$ and t_{DECAY} as shown in Figure 26. The time $t_{MEASURED}$ is the interval from when the reference signal switches to when the output voltage decays ΔV from the measured output high or output low voltage. t_{DECAY} is calculated with test loads C_L and I_L, and with ΔV equal to 0.5 V.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time t_{ENA} is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram (Figure 26). If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

Example System Hold Time Calculation

To determine the data output hold time in a particular system, first calculate t_{DECAY} using the equation given above. Choose ΔV to be the difference between the ADSP-2106x's output voltage and the input threshold for the device requiring the hold time. A typical ΔV will be 0.4 V. C_L is the total bus capacitance (per data line), and I_L is the total leakage or tristate current (per data line). The hold time will be t_{DECAY} plus the minimum disable time (i.e., t_{HDWD} for the write cycle).

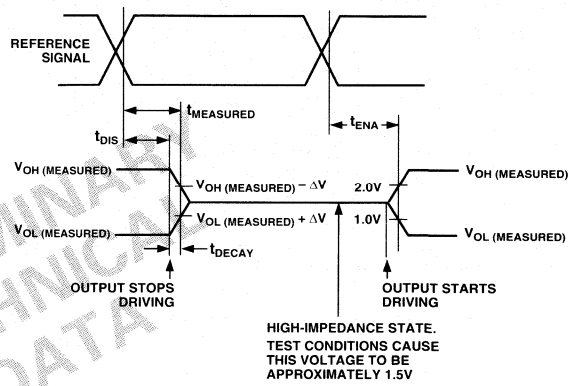


Figure 26. Output Enable/Disable

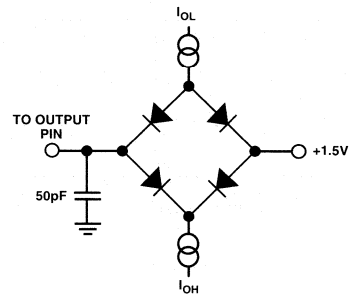


Figure 27. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

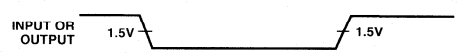


Figure 28. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Capacitive Loading

Output delays are based on standard capacitive loads: 50 pF on all pins (see Figure 27). The delay specifications given should be derated by a factor of 1.5 ns/50 pF for loads other than the nominal value of 50 pF. Figure 29 shows how output rise time varies with capacitance. Figure 30 shows graphically how output delays vary with load capacitance. Note that the graphs may not be linear outside the ranges shown.

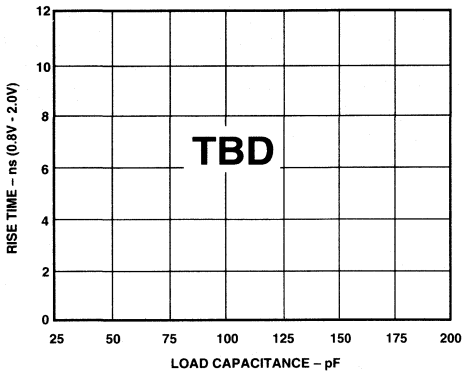


Figure 29. Typical Output Rise Time vs. Load Capacitance (at Maximum Case Temperature)

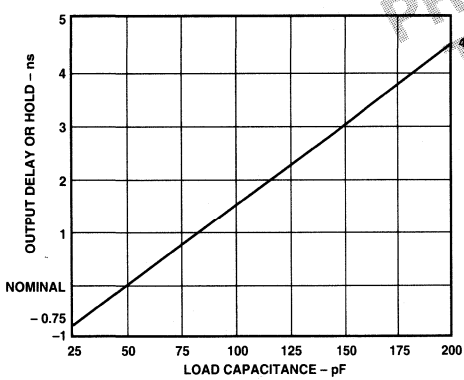


Figure 30. Typical Output Delay or Hold vs. Load Capacitance (at Maximum Case Temperature)

ENVIRONMENTAL CONDITIONS

Thermal Characteristics

The ADSP-2106x is packaged in a 240-lead EDQUAD* (a thermally enhanced PQFP). The top surface of the package contains a copper slug from which most of the die heat is dissipated. The slug is flush with the top surface of the package. Note that the copper slug is internally connected to V_{DD} through the device substrate.

*EDQUAD is a trademark of ASAT, Inc.

The commercial temperature range (K grade) ADSP-2106x is specified for operation at T_{AMB} of 0°C to +70°C. To ensure long-term reliability and package integrity, the maximum recommended junction temperature (T_J) is 130°C. To ensure that T_J does not exceed 130°C, a heat sink and/or air flow source may be used. A heat sink should be attached with a thermal adhesive.

$T_J = T_{AMB} + (PD \times \theta_{JA})$

$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$

T_{CASE} = Case temperature (measured on top surface of package)

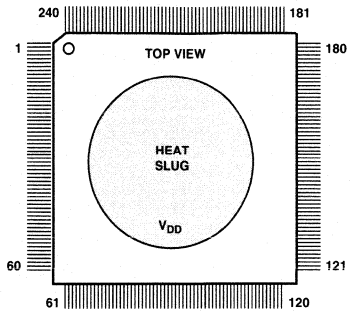
PD = Power dissipation in W (this value depends upon the specific application; a method for calculating PD is shown under "Power Dissipation").

ADSP-2106x Thermal Characteristics

Airflow (Linear Ft./Min.)	0	100	200	300
θ_{JA}*	20°C/W	18°C/W	16°C/W	14°C/W
θ_{JC}	TBD	TBD	TBD	TBD
θ_{CA}	TBD	TBD	TBD	TBD

*NOTE: This is preliminary data based on a similar package.

EDQUAD PIN CONFIGURATIONS



The EDQUAD package contains a copper heat slug flush with its top surface; the slug is internally connected to V_{DD} through the device substrate.

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	TDI	41	ADDR20	81	TCLK0	121	DATA41	161	DATA14	201	L2DAT0
2	TRST	42	ADDR21	82	TFS0	122	DATA40	162	DATA13	202	L2CLK
3	EVDD	43	EGND	83	DR0	123	DATA39	163	DATA12	203	L2ACK
4	TDO	44	ADDR22	84	RCLK0	124	EVDD	164	EGND	204	NC
5	TIMEXP	45	ADDR23	85	RFS0	125	DATA38	165	DATA11	205	EVDD
6	EMU	46	ADDR24	86	EVDD	126	DATA37	166	DATA10	206	L3DAT3
7	ICSA	47	EVDD	87	IVDD	127	DATA36	167	DATA9	207	L3DAT2
8	FLAG3	48	IGND	88	IGND	128	EGND	168	EVDD	208	L3DAT1
9	FLAG2	49	IVDD	89	ADRCLK	129	NC	169	DATA8	209	L3DAT0
10	FLAG1	50	ADDR25	90	REDY	130	DATA35	170	DATA7	210	L3CLK
11	FLAG0	51	ADDR26	91	HBG	131	DATA34	171	DATA6	211	L3ACK
12	EGND	52	ADDR27	92	CS	132	DATA33	172	EGND	212	EGND
13	ADDR0	53	EGND	93	RD	133	EVDD	173	DATA5	213	L4DAT3
14	ADDR1	54	MS3	94	WR	134	IVDD	174	DATA4	214	L4DAT2
15	EVDD	55	MS2	95	EGND	135	IGND	175	DATA3	215	L4DAT1
16	ADDR2	56	MS1	96	IVDD	136	DATA32	176	EVDD	216	L4DAT0
17	ADDR3	57	MS0	97	IGND	137	DATA31	177	DATA2	217	L4CLK
18	ADDR4	58	SW	98	CLKIN	138	DATA30	178	DATA1	218	L4ACK
19	EGND	59	BMS	99	ACK	139	EGND	179	DATA0	219	EVDD
20	ADDR5	60	ADDR28	100	DMAG2	140	DATA29	180	EGND	220	IGND
21	ADDR6	61	IGND	101	DMAG1	141	DATA28	181	EGND	221	IVDD
22	ADDR7	62	IVDD	102	PAGE	142	DATA27	182	L0DAT3	222	L5DAT3
23	EVDD	63	EVDD	103	EVDD	143	EVDD	183	L0DAT2	223	L5DAT2
24	ADDR8	64	ADDR29	104	BR6	144	IVDD	184	L0DAT1	224	L5DAT1
25	ADDR9	65	ADDR30	105	BR5	145	DATA26	185	L0DAT0	225	L5DAT0
26	ADDR10	66	ADDR31	106	BR4	146	DATA25	186	L0CLK	226	L5CLK
27	EGND	67	EGND	107	BR3	147	DATA24	187	L0ACK	227	L5ACK
28	ADDR11	68	SBTS	108	BR2	148	IGND	188	EVDD	228	EGND
29	ADDR12	69	DMAR2	109	BR1	149	DATA23	189	L1DAT3	229	ID2
30	ADDR13	70	DMAR1	110	IGND	150	DATA22	190	L1DAT2	230	ID1
31	IVDD	71	HBR	111	IVDD	151	DATA21	191	L1DAT1	231	ID0
32	ADDR14	72	DT1	112	EGND	152	IVDD	192	L1DAT0	232	LBOOT
33	ADDR15	73	TCLK1	113	DATA47	153	DATA20	193	L1CLK	233	RPBA
34	IGND	74	TFS1	114	DATA46	154	DATA19	194	L1ACK	234	RESET
35	ADDR16	75	DR1	115	DATA45	155	DATA18	195	EGND	235	EBOOT
36	ADDR17	76	RCLK1	116	EVDD	156	EGND	196	IGND	236	IRQ2
37	ADDR18	77	RFS1	117	DATA44	157	DATA17	197	IVDD	237	IRQ1
38	IVDD	78	EGND	118	DATA43	158	DATA16	198	L2DAT3	238	IRQ0
39	EVDD	79	CPA	119	DATA42	159	DATA15	199	L2DAT2	239	TCK
40	ADDR19	80	DT0	120	EGND	160	EVDD	200	L2DAT1	240	TMS

ANALOG DEVICES

ADSP-2100 Family Software and Hardware Development Tools

ADDS-21xx-TOOLS

2

FEATURES

DEVELOPMENT SOFTWARE

SYSTEM BUILDER
Defines Architecture of ADSP-21xx System
Specifies Amount of RAM/ROM Memory

ASSEMBLER
Easy-to-Program, Algebraic Instruction Set Syntax
Supports C Language Constructs
Provides Flexible Macro Processing
Encourages Modular Code Development

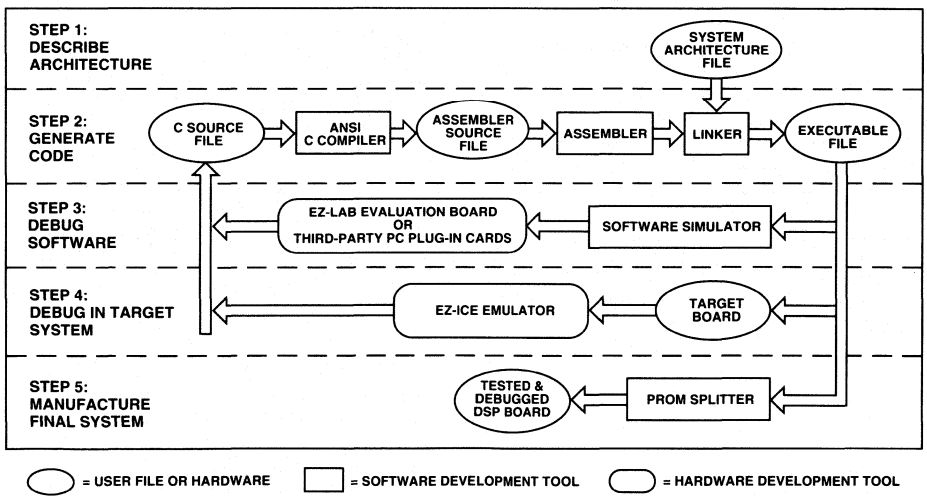
LINKER
Maps Assembler Output to Target System Memory
Supports User-Defined Library Routines
Creates Memory Map Listing

PROM SPLITTER & HIP SPLITTER
Generates PROM Programmer Compatible Files in a Variety of Industry-Standard Formats
Formats Executable File for Programming PROMs or for Host Processor Booting

SIMULATOR
Features Reconfigurable GUI (Graphical User Interface)
Supports Full Symbolic Disassembly and On-Line Assembly
Provides Breakpoint and Single-Step Execution
Includes CBUG™ C Source-Level Debugger as Integrated Tool
Supports Multiple Break Conditions
Provides Full View of All Processor Registers and Memory for Direct Modification of Contents
Profiles Code Execution History
Uses Data Files to Simulate Parallel I/O Ports, Serial Ports, HIPs, and Analog I/O Interface
Plots Data Memory Graphically

CBUG is a trademark of Analog Devices, Inc.

SYSTEM DEVELOPMENT DIAGRAM



ADDS-21xx-TOOLS

G21 OPTIMIZING C COMPILER & C RUNTIME LIBRARY
Compliant with ANSI C Standards
Includes C-Callable Library of ANSI-Standard and DSP Functions
Supports In-Line Assembly Code Using *asm* () Construct
Incorporates Optimizing Algorithms
Generates Reliable and ROM-able Code
Simplifies Interrupt Handling via Library Functions
Provides Support for Heap Memory Management
Supports Switches Used by the ADSP-21000 Family G21K Floating Point C Compiler
Supports Float Type IEEE-Single Precision Math Routines

CBUG C SOURCE-LEVEL DEBUGGER
Supports Single Step Execution
Supports Breakpoints
Integrated with Simulators

EZ-ICE® EMULATOR (ADSP-2101, ADSP-2111, ADSP-21msp50)
Performs Full-Speed, In-Circuit Emulation of ADSP-21xx Target Systems
Contains GUI (Graphical User Interface) for Easier Debugging Control
Plugs Directly Into Processor Socket on Target Board
Single-Step Capability
Stand Alone Operation for Software Debugging
Upload/Download Memory with IBM PC

3-VOLT EMULATION CONVERTER BOARD
Used with the ADSP-2101 EZ-ICE or Full-Featured ICE to Enable Emulation with an ADSP-2103 (3 V) Target System

EZ-LAB® EVALUATION BOARD (ADSP-2101, ADSP-2111, ADSP-21msp50)
Preprogrammed with DSP Demo Programs
Four Channel, 8-Bit DAC (D/A Converter) Port
Contains Voice I/O Port with Microphone Input and Powered Output for Speaker
Full Memory Expansion and I/O from Bus Expansion Connector
Serial Port Interface via SPORT Connector

EZ-KIT STARTER PACKAGES (ADSP-2101, ADSP-2111)
Complete Hardware and Software Development Kit
Includes the ADSP-2101 or ADSP-2111 EZ-LAB Evaluation Board and ADSP-2100 Family Assembler/Linker and Simulator Software for IBM PC
Includes *Digital Signal Processing Applications Using the ADSP-2100 Family* Applications Handbook with Source Code Diskette
Includes *Digital Signal Processing Laboratory Using the ADSP-2101 Microcomputer* Laboratory Workbook with Introductory DSP Experiments

GENERAL DESCRIPTION

The ADSP-2100 Family Development Software, a complete set of software design tools, lets you program applications for this family of DSP microprocessors that includes the ADSP-2100, ADSP-2101, ADSP-2105, ADSP-2111, ADSP-2115, ADSP-21msp50, and the newest member, the ADSP-2171 microcomputer. With these tools, you can quickly and efficiently program your DSP applications.

DSP Software Development Tools

The software development tools include the following programs:

- System Builder
- Assembler
- Linker
- Simulator
- G21 C Compiler
- C Runtime Library
- CBUG C Source-Level Debugger
- PROM Splitter

The System Builder reads your system specification file and then generates an architecture description file that passes information about your target hardware to the linker, simulator, and emulator. Code generation begins after you create assembly language source code modules. These modules are assembled separately by the assembler and then linked together to form an executable program (memory image file).

The highly readable *algebraic syntax* of the ADSP-2100 Family instruction set eases programming in assembly language. Multiply-accumulate instructions are written in the same manner as the actual equation. For example, the algebraic statement `r = r + x*y` is coded in assembly language as

```
MR = MR + MX0*MY0.
```

The simulator configures program and data memory according to the architecture description file and simulates the memory-mapped I/O ports to let you debug your system and analyze its performance. After simulating your system and software, use the emulator with your prototype hardware to test circuitry, timing, and real-time software execution. The PROM Splitter then translates the linker-output executable file into an industry-standard file format for a PROM burner. Once you burn the code into a PROM device and plug in an ADSP-21xx processor to the target board, your prototype is ready to run.

Development software is available for the IBM (or IBM-compatible) PC and Sun4 workstation platforms.

DSP Hardware Development Tools

- EZ-ICE Emulators
- Full-Featured Emulators*
- EZ-LAB Evaluation Boards
- EZ-KIT Development Tools Packages

The ADSP-2100 Family hardware development tools provide a controlled environment for observing, debugging, and testing activities in a full-speed target system. Our ADSP-2100 Family EZ-ICE Emulators provide this control by replacing the target processor. The EZ-ICE, controlled by an IBM PC host computer that runs an interface similar to the ADSP-2100 Family Simulators, lets you examine and modify processor information such as registers and memory. The Full-Featured Emulators* also offer trace capability and complex breakpoints.

*Please refer to the ADDS-21xx-ICE data sheet.

The ADSP-2100 Family EZ-LAB Evaluation Boards let you test coded applications in real time without a host or PC. At reset, the processor on the ADSP-2100 Family EZ-LAB boots code and program memory into its internal program memory from the EPROM, and then executes the code.

EZ-KIT offers a complete development environment: the ADSP-2100 Family Assembler/Linker and Simulator, an ADSP-2100 Family EZ-LAB Evaluation Board, an applications handbook, plus a laboratory textbook and source code diskettes.

SYSTEM BUILDER

The System Builder lets you create systems based on ADSP-21xx Memory Variant processors by allowing any on-chip data memory and program memory configuration; the memory may be specified as RAM or ROM. It also lets you design ADSP-21xx Family systems with paged external data memory, extending the processor's address space for additional data storage.

G21 C COMPILER

The G21 C Compiler is an optimizing ANSI compiler based on the GNU gcc compiler. Applications written in C are compiled, assembled, and linked to create executable ADSP-21xx programs that can be debugged with an ADSP-21xx Simulator or Emulator. It also supports in-line assembly code using the `asm()` construct, which lets you use C expressions.

The G21 C Compiler contains optimization features to increase execution speed of the resultant assembly code. These features include algorithms to perform the following:

- Constant Folding
- Common subexpression elimination
- Loop optimization and strength reduction
- Global and local register allocation
- Parallelization
- Instruction scheduling

C RUNTIME LIBRARY

The C Compiler comes with ANSI-standard functions and a set of C-callable library routines commonly used in digital signal processing to speed up development.

The ADSP-2100 Family C Runtime Library includes the following ANSI-standard and DSP-specific functions:

abs	absolute value
acos	arc cosine
asin	arc sine
atan	arc tangent
atan2	arc tangent of quotient
ceil	ceiling
cos	cosine
cosh	hyperbolic cosine
exp	exponential
fabs	absolute value
fir	finite impulse response (FIR) filter
floor	floor
fmod	floating-point modulus
frexp	separate fraction and exponent
ifftN	N-point inverse fast Fourier transform (IFFT)
iir	infinite impulse response (IIR) filter
interrupt	define interrupt handling
isalpha	detect alphabetic character
isdigit	detect decimal digit
labs	absolute value
ldexp	multiply by power of 2
log	natural logarithm
log10	base 10 logarithm
memcmp	compare objects
memcpy	copy characters from one object to another
memset	set range of memory to a character
modf	separate integral and fractional parts
pow	raise to a power
raise	force a signal
signal	define signal handling
sin	sine
sinh	hyperbolic sine
sqrt	square root
strcat	concatenate strings
strcmp	compare strings
strcpy	copy from one string to another
strlen	string length
strncat	concatenate characters from one string to another
strncmp	compare characters in strings
strncpy	copy characters from one string to another
tan	tangent
tanh	hyperbolic tangent
timer_off	disable ADSP-21020 timer
timer_on	enable ADSP-21020 timer
timer_set	initialize ADSP-21020 timer
va_arg	get next argument in variable list
va_end	reset variable list pointer
va_start	set variable list pointer

Interrupt Handling in C

The C environment supports hardware interrupts —a key feature that facilitates programming. The signal handling functions of the C library, *signal, raise,* and *interrupt,* process ADSP-21xx interrupts such as serial port transmit and receive interrupts, timer interrupts, and external interrupt request signals.

The *signal* and *raise* functions direct execution to a specific C interrupt service routine based on the type of interrupt that occurs. This routing service allows the entire application to be written in C without assembly language code. The signal handling routines save and restore registers, and the overhead is usually minimal compared to overall program execution time. If you choose to write custom interrupt service routines in assembly language, you can use the *signal* and *raise* functions to set up service routines in the C environment.

ASSEMBLER

The Assembler reads source files containing ADSP-2100 Family assembly language and generates a relocatable object file. The Assembler includes a preprocessor that lets you use C preprocessor directives such as `#define`, `#include`, `#if`, `#ifdef`, and `#else` in assembly code.

Assembler directives define code modules, data buffers, data variables, and memory-mapped I/O ports. Either assembler directives or C preprocessor directives define and invoke macros.

LINKER

The Linker processes separately assembled object files to create a single executable program. It assigns memory locations to code and data in accordance with the architecture file defined by the System Builder.

The Linker also generates symbols (variable names and program labels) in the processed files, which the simulator, emulator, and the CBUG C Source-level debugger use to perform symbolic debugging.

PROM SPLITTER AND HIP SPLITTER

The PROM Splitter translates an ADSP-21xx executable program into a file used to program PROM memory devices. The PROM Splitter's output file can be generated in Motorola S Record or Intel Hex Record format. Motorola S2 format is supported for byte stream output.

The HIP Splitter utility generates ADSP-2111, ADSP-2171, and ADSP-21msp5x programs to be downloaded from a host processor through its Host Interface Port (HIP). The HIP Splitter's output file can be generated in Motorola S Record or Intel Hex Record format.

Both the PROM Splitter and the HIP Splitter have a loader option that enables loading of external memory.

SIMULATORS

There is a simulator for each ADSP-2100 Family processor that provides instruction-level simulation of program execution. The Simulator models system memory and I/O according to the contents of the system architecture file, and provides windows to display different portions of the target system hardware (See Figure 1). The Graphical User Interface (GUI) lets system designers interactively observe and alter register and memory contents, providing a powerful debug environment. Simulator commands can be entered from the mouse or keyboard.

Features offered by the ADSP-2100 Family Simulators include the following:

- Program and Data Memory Simulation
- Memory-mapped I/O Port Simulation
- Interrupt Simulation
- Program Booting (from PROM or host processor) Simulation
- Code Execution Pattern Profiling for Program Optimization
- On-Line Help
- Reconfigurable Windows
- Same User Interface as EZ-ICE Emulators

CBUG C SOURCE-LEVEL DEBUGGER

The Simulators are seamlessly integrated with the CBUG C source-level debugger. CBUG supports the following operations:

- Run, Step, Next, and Finish Program Execution Commands
- C Source Code Breakpoints
- Local and Global Variable Display with Auto Refresh Examines Value of Variables at Previously Executed Instructions
- Symbol Look-Up

HARDWARE TOOLS

ADSP-2100 Family EZ-ICE Emulators

ADSP-2100 Family EZ-ICEs are in-circuit probe boards, including the processor being emulated, used for testing and debugging an ADSP-21xx-based system. Its features make it easy to view and manipulate the data needed to debug your DSP applications:

- Up to 32 user breakpoints
- Memory plot
- Program code modification directly in emulator's program memory window
- Symbolic debugging
- On-line help for currently selected window
- View relevant data without switching screens
- Overlay memory

Control and debug features include single-step capabilities, with or without register displays, and multiple breakpoint capability.

At power-up, the host processor automatically resets and performs a diagnostic check to ensure that both host memory and EZ-ICE are functional; it automatically displays any failures found.

ADSP-2101, ADSP-2111, ADSP-21msp50 EZ-ICE Emulators

Connector Requirements

The probe's PGA footprint that protrudes from the bottom of the board fits into a socket in your target system. Note that the socket must accept the ADSP-21xx footprint. You may use an optional umbilical cord (pin extender) to make the emulator-to-target connection when your board prohibits direct connection of the ADSP-2100 Family EZ-ICE to the target socket. (The cord may limit the speed at which the programs run.)

GUI Interface

To increase development productivity, a Graphical User Interface (GUI) makes your data easier to view and manipulate when debugging. In addition, you can view relevant information without switching between screens and can obtain on-line help for the currently selected window. The same user interface comes with the ADSP-2100 Family Simulators.

Clock Speed

EZ-ICE runs at full speed. There is no degradation of processor performance other than $\overline{BR}$, $\overline{BG}$, and $\overline{RESET}$, which are slightly delayed. A jumper is used to select either the target system clock or the EZ-ICE clock. The oscillator socket lets you use other oscillator devices to achieve different clock speeds.

Memory

The ADSP-2101 and ADSP-2111 EZ-ICE each have 8K × 24-bit overlay program memory and 16K × 16-bit overlay data memory. The ADSP-21msp50 EZ-ICE contains 16K × 24-bit overlay program memory and 16 × 16-bit overlay data memory. You can either run programs from target system memory, emulator overlay memory, or from a combination of both. The overlay memory option is jumper-selectable.

Additional Equipment Required
EZ-ICE requires a +5 V dc power supply capable of supplying 1 A of current.

3-Volt Emulation
The 3-Volt Emulation Converter Board may be used with the ADSP-2101 EZ-ICE or Full-Featured ICE to enable emulation of ADSP-2103 (3 V) systems.

Surface Mount Adaptors
ADSP-2101/ADSP-2105/ADSP-2115
Two surface mount adaptors are available for emulation of the ADSP-2101. For the 68-pin PLCC package of the ADSP-2101 and ADSP-2105, a PGA-to-PLCC adaptor is available from the vendors listed in the ordering guide in this data sheet. For the 80-pin PQFP package of the ADSP-2101, a 68-pin PGA to 80-pin PQFP adaptor is available from Analog Devices.

The ADDS-2101-PGA/PQFP, a surface-mountable PGA-to-PQFP adaptor, provides a footprint that exactly matches the 80-pin package. This solution does not require extra space around the adaptor or an extra through hole to the PQFP package to let you use the same PCB in production. The PGA-to-PQFP adaptor is surface mounted in the usual manner, and the PGA connector of the ADSP-2101 EZ-ICE or ICE can be directly plugged in.

ADSP-2100A/ADSP-2111
The ADDS-2100-PGA/PQFP, a surface-mountable 101 PGA to 100 pin PQFP adaptor, matches both the ADSP-2100A and the ADSP-2111 package footprints. This solution does not require extra space around the adaptor, and you can use the same PCB in production. The PGA-to-PQFP adaptor is surface mounted in the usual manner, and the PGA connector of the ADSP-2100A ICE or the ADSP-2111 EZ-ICE or ICE can be directly plugged in.

ADSP-21msp50
The ADDS-msp50-PGA/PQFP, a surface mountable 145-pin PGA to 100-pin PQFP adaptor for use with the ADSP-21msp50 EZ-ICE or ICE, lets you use the 144-pin PGA probe of the EZ-ICE with target boards designed for the 100-pin PQFP package of the ADSP-21msp55 or ADSP-21msp56.

Extra space around the adaptor and extra through holes to the PQFP package are not required to let you use the same PCB in production. The adaptor is surface-mounted in the usual manner, and the PGA connector of the ADSP-21msp50 EZ-ICE probe can be directly plugged in.

ADSP-2100 Family EZ-LAB Evaluation Board
The ADSP-2100 Family EZ-LAB Evaluation Board, a complete DSP system on a 4 1/2" × 6" board, lets you test coded applications in real time without a host or PC. At reset, the processor on the ADSP-2100 Family EZ-LAB boots code and programs memory data into its internal program memory from a 64K × 8-bit EPROM and then executes the code.

Demo Programs
Use the prepared demonstrations on the ADSP-2100 Family EZ-LAB, which includes speech and graphics applications, to familiarize yourself with and evaluate the ADSP-2100 Family processors. The EPROM is mapped into the boot memory space. Upon reset, the processor loads boot page 0 into its internal program memory and begins execution. During program execution, any one of the eight boot pages can be loaded into the processor under software control.

The demonstrations use the microphone and speaker connections for audio input and output. EZ-LAB has four DAC outputs to connect to an oscilloscope for display. In addition to these outputs, EZ-LAB has an expansion connector and a serial port connector for synchronous serial data I/O. The connectors let you access the serial ports, external address bus, external data bus, control signals, interrupt lines, and the host interface port.

The demonstration board operates alone when you attach a +5 V dc @ 1 amp and ±12 V dc power supply with a common power return.

Analog I/O
A codec attaches to the processor's serial port 0 on the ADSP-21xx EZ-LAB. (The ADSP-21msp50 processor contains an on-chip, 16-bit, sigma-delta A/D, D/A converter.) Configure the other serial port for interrupts and flags by changing on-board jumpers. The input signal to the codec can be a microphone, signal generator or any other high impedance source, and the resulting output signal can drive a small speaker.

The ADSP-2101 EZ-LAB and ADSP-2111 EZ-LAB contain socket-mounted 16.384 MHz crystals, and the ADSP-21msp50 EZ-LAB contains a socket-mounted 13.00 MHz crystal. The sockets let you replace the crystals to achieve different clock speeds. Note that Analog Devices' specifications for the ADSP-21msp50 EZ-LAB are not supported for speeds greater than 13.00 MHz.

EZ-LAB provides manual control of several functions. For example, push-buttons activate the IRQ2 interrupt and FLAG IN pins, and an on-board hardware RESET switch resets EZ-LAB.

Using EZ-LAB and EZ-ICE Together
Combine an EZ-LAB and EZ-ICE to form a high speed DSP nvironment with an interactive, window-based debugging interface. Simply remove the processor device from the EZ-LAB and plug in an ADSP-2101, ADSP-2111, or ADSP-21msp50 EZ-ICE. This combination lets you prototype and evaluate your application without initial time investment in hardware design.

ADSP-2105 and ADSP-2115 System Development
The ADSP-2101 EZ Development Tools support the ADSP-2105 and the ADSP-2115 because their architectures are a subset of the ADSP-2101. The ADSP-2105 has one serial port (instead of two), and both the ADSP-2105 and the ADSP-2115 have half the internal memory of the ADSP-2101. Use the ADSP-2101 EZ-LAB to evaluate, and the ADSP-2101 EZ-ICE for emulation and debugging of both the ADSP-2115 and ADSP-2105 target systems.

ADSP-2100 Family Ordering Guide
16-Bit Fixed-Point Family

Model Number	Description	ADSP-2100A	ADSP-2101	ADSP-2103	ADSP-2105	ADSP-2111	ADSP-2115	ADSP-2171	ADSP-21msp50
STARTER PACKAGES									
ADDS-2101-EZ-KIT	Starter Package: Assembler Package and Simulators,* ADSP-2101 EZ-LAB	–	✓	✓	✓	–	✓	–	–
ADDS-2111-EZ-KIT	Starter Package: Assembler Package and Simulators,* ADSP-2111 EZ-LAB	–	–	–	–	✓	–	–	–
SOFTWARE AND HARDWARE									
ADDS-21xx-DSW-PC	Assembler Package and Simulators*	✓	✓	✓	✓	✓	✓	✓	✓
ADDS-21xx-BUN-PC	Assembler Package, Simulators,* and C Tools**	✓	✓	✓	✓	✓	✓	✓	✓
ADDS-21xx-C-UP-PC	Upgrades for Owners of DSW or EZ-KIT to Include C Tools**	✓	✓	✓	✓	✓	✓	✓	✓
ADDS-21xx-BUN-SUN	Assembler Package, Simulators, and C Tools* for Sun4 Platform	✓	✓	✓	✓	✓	✓	✓	✓
ADDS-2101-EZ-LAB	Evaluation Board for Testing Coded DSP Applications	–	✓	✓	✓	–	✓	–	–
ADDS-2101-EZ-ICE	Compact Emulator for Debugging and Testing Code	–	✓	✓	✓	–	✓	–	–
ADDS-2101-ICE	Full-Featured Emulator with Trace	–	✓	–	–	–	–	–	–
ADDS-2101-3V	3-Volt Emulation Converter Board	–	–	✓	–	–	–	–	–
ADDS-2111-EZ-LAB	Evaluation Board for Testing Coded DSP Applications	–	–	–	–	✓	–	–	–
ADDS-2111-EZ-ICE	Compact Emulator for Testing Coded DSP Applications	–	–	–	–	✓	–	–	–
ADDS-2111-ICE	Full-Featured Emulator with Trace	–	–	–	–	✓	–	–	–
ADDS-21msp50-EZ-LAB	Evaluation Board for Testing Coded DSP Applications	–	–	–	–	–	–	–	✓
ADDS-21msp50-EZ-ICE	Compact Emulator for Debugging and Testing Code	–	–	–	–	–	–	–	✓

NOTES
*Assembler, Assembly Library/Librarian, Linker, PROM Splitter, HIP Splitter, and ADSP-21xx Simulators.
**G21 C Compiler, C Runtime Library, and CBUG C Source-Level Debugger.

Model Number	Description	
OPTIONAL ACCESSORIES		
ADDS-2101-UMBIL	ADSP-2101 Probe-to-Target Umbilical Cord (8")	
ADDS-2111-UMBIL	ADSP-2111 Probe-to-Target Umbilical Cord (8")	
ADDS-2101-PGA/PQFP	ADSP-2101 8-Pin PGA to 80-Pin PQFP Adaptor (for ADSP-2101 EZ-ICE)	
ADDS-2100-PGA/PQFP	ADSP-2100/ADSP-2111 100-Pin Surface Mountable PGA-to-PQFP Adaptor (for ADSP-2100A, ADSP-2111 ICE or ADSP-2111 EZ-ICE)	
ADDS-msp50-PGA/PQFP	ADSP-21msp50 144-Pin PGA to ADSP-21msp55 10-Pin PQFP Adaptor (for ADSP-21msp50 EZ-ICE)	
AVAILABLE FROM OTHER VENDORS		
68-Pin PGA-PLCC Adaptor (for ADSP-2101 and ADSP-2105)	Emulation Technology 2344 Walsh Avenue Santa Clara, CA 95051 (408) 982-0660	AP4-68-PGA
	EDI Corporation P.O. Box 366 Patterson, CA 95363 (209) 892-3270	68-PGA/PLCC
	McKenzie Technology 910 Page Avenue Fremont, CA 94538 (510) 651-2700	68-PGA/PLCC
100-Pin PGA-PQFP Adaptor (for the Amp Socket, the ADSP-2100A, or the ADSP-2111 Full-Featured ICE or EZ-ICE)*	Emulation Technology 2344 Walsh Avenue Santa Clara, CA 95051 (408) 982-0660	AS-PGA-QF01A-ADSP-2100
RAM Expansion Card for EZ-LAB: ADSP-2101, ADSP-2111 and ADSP-21msp50 *Available from:* Momentum Data Systems 1520 Nutmeg Place #108 Costa Mesa, CA 92626 (714) 557-6884 (714) 557-6969 fax	The RAM Expansion card expands the amount of program and data RAM available to the maximum amount each DSP can address. The card also provides a user prototype area which includes four (4) fully coded block select lines for addressing the expansion area, and all DSP signals are brought out to an expansion header for easy connection. You may also load a boot program into RAM and then restart the DSP without reprogramming the EPROM.	
PC Interface Card for the EZ-LAB *Available from:* Momentum Data Systems 1520 Nutmeg Place #108 Costa Mesa, CA 92626 (714) 557-6884 (714) 557-6969 fax	The PC Interface card lets you use an IBM compatible computer as a host for DSP and RAM expansion cards. Using the Bus Request and Bus Grant signals, the PC gains access to the RAM and prototype expansion areas. The PC can interrupt the DSP, and the DSP can interrupt the PC via a communication register. This register enables signaling from the DSP to the PC without slowing down the DSP for bus accesses to check status. The card also provides access to the boot section of the expansion card for downloading programs and restarting the DSP so the developer can design and test programs without needing to burn EPROMs.	
ADSP-2101 EZ-LAB Evaluation Board LAB+ *Available from:* Hollis Electronics 5 Northern Boulevard Unit 13 Amherst, NH 03031 (603) 598-4640 (603) 598-3428 fax	The LAB+ Enhancement Board, designed specifically for the ADSP-2101 EZ-LAB, provides a full complement of external program and data RAM. As a low cost alternative to an in-circuit emulator, LAB+ contains a dual UART with RS-232 drivers that enable a Host PC communication link with the DSP ROMulator, an on-board monitor/debugger that runs from boot EPROM. The ROMulator lets the user download executable (*.exe) files, inspect or modify program/data/register RAM, set or clear breakpoints, and single-step and run applications at full speed.	

*For use with the ADSP-2111, please call Analog Devices Customer Support for important installation instructions at (617) 461-3881.

ADSP-21000 Family
Hardware and Software Development Tools

ADDS-210xx-TOOLS

FEATURES

DEVELOPMENT SOFTWARE

ASSEMBLER
Easy-to-Use Algebraic Syntax
Contains an Extensive Set of Directives
Allows Single-Cycle Access to Data from Program and Data Memory

LINKER
Combines Object and Library Files
Generates COFF Executable Files
Creates Memory Map Listing

ASSEMBLY LIBRARY/LIBRARIAN
Includes a Set of Arithmetic and DSP Functions
Incorporates User-Defined Routines

SIMULATOR
Reconfigurable, Windowed User Interface Common to All Analog Devices DSP Development Tools
Full Symbolic Disassembly and On-Line Assembly
Supports Simple Break Conditions
Simulates Memory and Port Configurations
Plots Memory Graphically

PROM SPLITTER
Supports Popular PROM Formats

C COMPILER AND RUNTIME LIBRARY

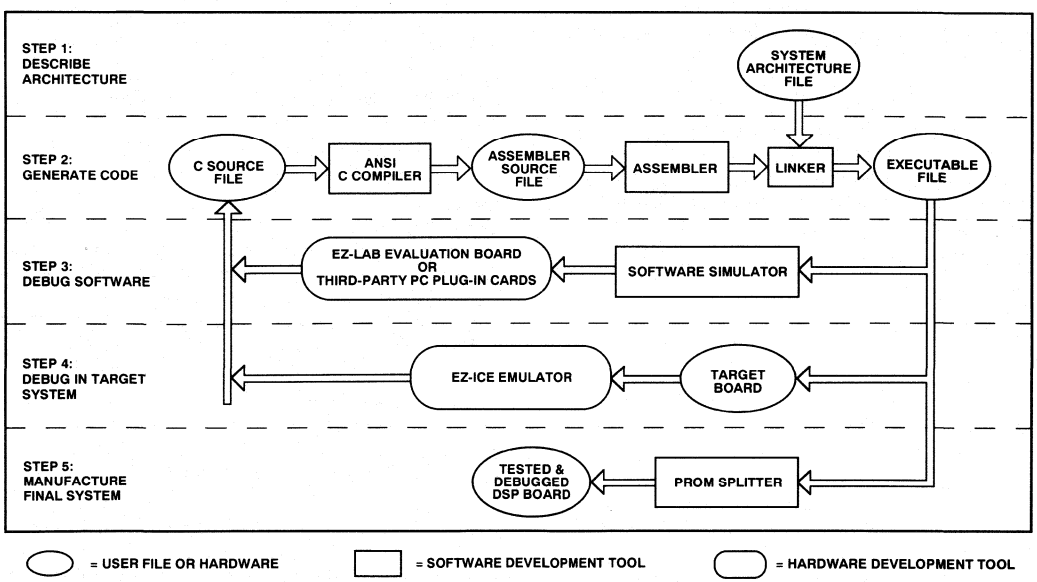
OPTIMIZING G21K ANSI C COMPILER
Supports Numerical C
Based on GNU C Compiler
Includes C-Callable Library of ANSI-Standard and DSP Functions
Supports In-Line Assembly Code

CBUG™ C SOURCE-LEVEL DEBUGGER
Integrated with Simulator and Emulator with Same User Interface
Evaluates ANSI-Standard C Expressions

C RUNTIME LIBRARY
Includes ANSI-Standard and Mathematics Functions
Handles Signals, Variables, and Characters
Includes Standard DSP Functions such as FIR, IIR, and FFT
Contains over 150 Functions and Macros

CBUG is a trademark of Analog Devices, Inc.

SYSTEM DEVELOPMENT DIAGRAM



ADDS-210xx-TOOLS

EZ-LAB® EVALUATION BOARD
Enables Evaluation, Prototyping, and Demonstration of ADSP-21000 Family Systems
Supports PC Host Control via RS-232 Link
Includes ADSP-21020 32-/40-bit Floating-Point DSP, 32K words of both Program Memory RAM and Data Memory RAM, Memory Bus Expansion Connectors, AD1849 SoundPort® Stereo Codec and other Peripherals

EZ-ICE® EMULATOR
Full-Speed, In-Circuit Emulation for ADSP-21020 Target Systems
Consists of IBM PC Plug-in Board with Small In-Circuit Probe (11-Pin JTAG)
ADSP-21020 On-Chip Emulation Features Enable Reliable, Nonintrusive Emulation
Provides PC-based Software Debug Environment with Graphical User Interface of ADSP-21020 Simulator
Upload/Download Programs and Data

EZ-KIT
Includes the EZ-LAB Evaluation Board and ADSP-21000 Family Development Software (Simulator and Assembler/Linker)

EZ-KIT PLUS
Includes the ADSP-21020 EZ-LAB, ADSP-21000 Family Development Software (Simulator and Assembler/Linker), and ADSP-21000 Family C Tools (Optimizing G21K ANSI C Compiler with C Runtime Library and CBUG C Source-Level Debugger)

ICEPAK™ Embeddable In-Circuit Emulator
Incorporates Embedded Emulation Functionality into a Plug-In Target Board

GENERAL DESCRIPTION

The ADSP-21000 Family Development Software Tools let you create and debug programs for the ADSP-21000 Family Floating-Point Processors on IBM PC-compatible or Sun4 platforms. They support your DSP products during all research, design and test stages.

DSP Software Development Tools
- Assembler
- Linker
- Assembly Library/Librarian
- Simulator
- PROM Splitter
- Optimizing G21K ANSI C Compiler with Numerical C
- CBUG C Source-Level Debugger
- C Runtime Library

The assembler translates ADSP-21000 Family assembly language text files into object code. The G21K C Compiler compiles C source code into object code. The Linker then links the multiple object files to form an executable program.

The ADSP-21000 Family Simulator executes programs in software the same way the processor executes programs in hardware, by displaying different portions of the hardware environment through reconfigurable windows.

Minimum PC Requirements
- a 386- or 486-based PC; 640K RAM (2MB total RAM is required)
- EGA or VGA monitor and color video card
- High-density floppy disk drive
- DOS 3.1 or higher

DSP Hardware Development Tools
- EZ-LAB Evaluation Board
- ICEPAK Embeddable In-Circuit Emulator
- EZ-ICE Emulator
- EZ-KIT and EZ-KIT Plus

The ADSP-21020 EZ-LAB, a ready-to-run target system and evaluation platform, lets you download and execute your ADSP-21000 Family programs in real time. EZ-ICE, an in-circuit emulator, provides a controlled environment for observing, debugging, and testing by directly connecting to the target processor through its JTAG interface. The ICEPAK, a small daughter card, incorporates embedded emulation functionality: you can add all the capabilities of the EZ-ICE to your PC plug-in target board. EZ-KIT includes the EZ-LAB Evaluation Board and the ADSP-21000 Family Development Software, and EZ-KIT Plus includes the C Compiler, C Runtime Library, and CBUG Source Level Debugger.

SOFTWARE TOOLS

Assembler
The Assembler reads ADSP-21000 Family assembly language source files and generates a relocatable object file. It includes a preprocessor that lets you use C preprocessor directives, *#define, #include, #if, #ifdef,* and *#else* in assembly code. Assembler directives define code modules, data buffers, data variables, and memory-mapped I/O ports. Both the assembler and C preprocessor have directives to define macros.

Programming in assembly language is eased by the highly readable algebraic syntax of the ADSP-21000 Family instruction set. An add instruction, for example, is written in the same manner as the actual equation: The algebraic statement r = x + y is coded in assembly language as (f0 = f1 + f2).

Linker
The Linker processes separately assembled object and library files to create a single executable program. It assigns memory locations to code and data according to user-defined architecture files—text files that describe the memory configuration of the target system. The Linker generates symbols (variable names and program labels) in the processed files, which are used by the simulator and emulator to perform symbolic debugging.

Assembly Library/Librarian
The Assembly Library contains standard arithmetic and DSP routines accessible through your programs. You can create libraries of your own functions using the librarian tool.

Simulator
The Simulator, a software model of the DSP, provides instruction-level simulation of program execution. It models system memory and I/O according to the contents of the system architecture file, and displays hardware registers and memory in windows (See Figure 1). The Graphical User Interface (GUI) with reconfigurable windows, lets you observe and alter register and memory contents, making a powerful debugging environment. The simulator also reads symbols to perform symbolic debugging.

Features of the ADSP-21000 Family Simulator include the following:

- Display of all Registers, Caches, and Stacks
- Single-Step Execution
- Integration with CBUG C Source-Level Debugger
- Interrupt Simulation
- Plotting Memory
- Break Points and Break Conditions
- Simulation of Program and Data Memory

G21K ANSI C Compiler

Known for its efficiency and reliability, the GNU-based Optimizing G21K C Compiler supports in-line assembly code using the *asm( )* construct, and generates COFF (Common Object Format Files), an industry-standard file format for object, library, and executable files.

For portable code and development platform flexibility, the G21K conforms to ANSI Standard X3J11. Its optimizing features include the following:

- Constant folding
- Common subexpression elimination
- Loop unrolling and strength reduction
- Global and local register allocation
- Flow analysis
- Pattern combining
- Instruction scheduling
- Global and Local register allocation
- Parallelization

NUMERICAL C

Numerical C—extensions to the G21K ANSI C compiler—require fewer lines of code to perform vector and matrix operations. Developed with the ANSI Numerical C Extensions Group (NCEG), a working committee reporting to ANSI X3J11, Numerical C lets the compiler perform more powerful optimizations. These Numerical C extensions have been adapted by the Free Software Foundation for GNU C compilers (version 2.4).

Numerical C supports iterators used for generating one or more loops out of a single statement. This Numerical C code fragment for DSP application:

```
iter i = N;
A[i] = sin (2*PI*i/N);
```

is equivalent to this C Code:

```
int i, __ilimit__I = N;
for (i = 0; i <__ilimit__I; i++)
|
A[i] = sin (2*PI*i/N);
|
```

An FIR filter with k taps on the array of n numbers notated as follows:

$$y_i = \sum_{j=0}^{k} x_{i-j}\, a_j$$

is coded as this equation:

```
iter i = n, j = k;
y[i] = sum (x [i - j] * a [j]);
```

CBUG C Source-Level Debugger

CBUG, a full-featured C source-level debugger, works with the ADSP-21000 Family Simulator and EZ-ICE Emulator without hindering their full capabilities. It performs the following:

- Displays Variables and Expressions (Automatically Updated)
- Evaluates Standard ANSI C Expressions
- Stepping and Various Other Program Execution Commands
- Breakpoints and Conditional Breaks Based on Expression Evaluation
- Displays Symbol Definition and Values
- Displays Function Calling Tree
- Uses Same Friendly User Interface as Simulator

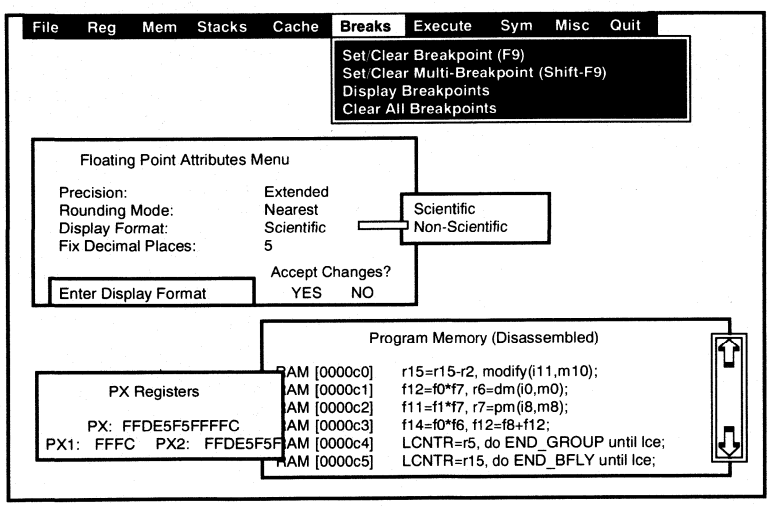


Figure 1. ADSP-21000 Family Simulator

C Runtime Library

The C Compiler has a set of ANSI-standard functions that ease program development. These library routines include ANSI-standard functions commonly used in digital signal processing. The table below contains all the C Runtime Library functions that perform digital signal processing operations.

Table I. ADSP-21000 FAMILY C RUNTIME LIBRARY

a_compress	A-law compression	matadd	matrix addition
a_expand	A-law expansion	matmul	matrix multiplication
abort	abnormal program end	matscalmut	multiply matrix by scalar
abs	absolute value	matsub	matrix subtraction
acos, acosf	arc cosine	mean	computes mean
asin, asinf	arc sine	memchr	find first occurrence of character
atan, atanf	arc tangent	memcmp	compare objects
atan2, atan2f	arc tangent of quotient	memcpy	copy characters from one object to another
atexit	register a function to call at program termination	memmove	copy characters from one object to another
atoi	convert string to integer	memset	set range of memory to a character
atof	convert string to long integer	modf, modff	separate integral and fractional parts
autocoh	autocoherence	mu_compress	μ-law compression
autocorr	autocorrelation	mu_expand	μ-law expansion
bsearch	perform binary search in sorted array	poll_flag_in	test input flag
biquad	biquad filter section	pow, powf	raise to a power
cabs	complex absolute value	raise	force a signal
calloc	allocate and initialize memory	rand	random number generator
ceil, ceilf	ceiling	realloc	change memory allocation
cexpf	complex exponential	rFFtN	N-point fast Fourier transform
cos, cosf	cosine	set_alloc_type	change memory allocation
cosh, coshf	hyperbolic cosine	setjmp	label for external linkage
cot, cotf	cotangent	setlocale	set the current locale
crosscoh	cross-coherence	signal	define signal handling
crosscorr	cross-correlation	sin, sinf	sine
div	division	sinh, sinhf	hyperbolic sine
exit	normal program termination	sqrt, sqrtf	square root
exp, expf	exponential	srand	random number seed
fabs, fabsf	absolute value	strcat	concatenate strings
fir	finite impulse response (FIR) filter	strchr	find first occurrence of character in string
floor, floorf	floor	strcmp	compare strings
fmod, fmodf	floating-point modulus	strcoll	compare strings
free	deallocate memory	strcpy	copy from one string to another
frexp, frexpf	separate fraction and exponent	strcspn	length of character segment in one string but not the other
getenv	get string definition from operating system		
histo	histogram	strerror	get string containing error message
idle	execute ADSP-21020 IDLE instruction	strlen	string length
ifftN	N-point inverse fast Fourier transform (IFFT)	strncat	concatenate characters from one string to another
iir	infinite impulse response (IIR) filter	strncmp	compare characters in strings
interrupt	define interrupt handling	strncpy	copy characters from one string to another
isalnum	detect alphanumeric character	strpbrk	find character match in two strings
isalpha	detect alphabetic character	strrchr	find last occurrence of character in string
iscntrl	detect control character	strspn	length of segment of characters in both strings
isdigit	detect decimal digit	strstr	find string within string
isgraph	detect printable character, not including whitespace	strtok	convert string to tokens
islower	detect lowercase character	strtol	convert string to long integer
isprint	detect printable character	strtoul	convert string to unsigned long integer
ispunct	detect punctuation character	strxfrm	transform string using LC_COLLATE
isspace	detect whitespace character	system	send string to operating system
isupper	detect uppercase character	tan, tanf	tangent
isxdigit	detect hexadecimal digit	tanh, tanhf	hyperbolic tangent
labs	absolute value	timer_off	disable ADSP-21020 timer
ldexp, ldexpf	multiply by power of 2	timer_on	enable ADSP-21020 timer
ldiv	division	timer_set	initialize ADSP-21020 timer
localeconv	get pointer for formatting to current locale	tolower	convert from uppercase to lowercase
log, logf	natural logarithm	toupper	convert from lowercase to uppercase
log10, log10f	base 10 logarithm	var	variance
longjmp	second return from setjmp	zero_cross	count zero crossings
malloc	allocate memory		

The ADSP-21000 Family Runtime Library includes the following ANSI-standard function categories:

- Standard Library
- Mathematics
- Signal, Variable and Character Handling

The library also includes signal processing functions in the following categories developed by Analog Devices:

- DSP Filters
- Fast Fourier Transforms
- Matrix Operations
- Interrupt Servicing

PROM Splitter
The PROM splitter translates an ADSP-21000 Family executable program into one of several formats for different PROM configurations, or downloads to a target system from a microcontroller. The PROM Splitter's output file generates Motorola S Record or Intel Hex Record format.

HARDWARE DEVELOPMENT TOOLS

EZ-LAB Evaluation Board Overview
EZ-LAB lets you control and observe ADSP-21000 Family programs executing in real-time from on-board RAM. The large memory space lets you develop high-performance floating-point DSP applications. Several demonstration programs accompany EZ-LAB for you to familiarize yourself with and evaluate the ADSP-21000 Family of floating-point DSPs.

ADSP-21020 EZ-LAB Evaluation Board Platform Requirements
The ADSP-21020 EZ-LAB requires a power supply that can deliver +5 V dc @ 1 amp and ±12 V dc @ 200 mA.

Memory
The ADSP-21020 EZ-LAB contains 32K × 48-bit words of zero-wait state program memory and 32K × 48-bit words of zero-wait state data memory.

Expansion Connectors
Two expansion connectors let you add additional program memory, data memory, and I/O devices to customize the system. The 96-pin expansion connectors accept standard Eurocard prototyping boards (6U or 3U form factor).

PC Control
A host PC controls the ADSP-21020 EZ-LAB board through an RS-232 link. With this connection, you can download and run ADSP-21000 Family programs using interface software that runs on the PC. Program results may be uploaded from EZ-LAB's on-board memory to the host PC. For code debug, plug the ADSP-21020 EZ-ICE Emulator into the EZ-LAB's JTAG emulation connection.

SoundPort Stereo Codec
The AD1849 SoundPort Stereo Codec enables the development of speech and audio processing applications. A 16-bit sigma-delta audio codec, the AD1849 integrates two sigma-delta DACs, two sigma-delta ADCs, antialiasing filters, digital interpolation filters, attenuators, and analog anti-imaging filters. It handles multiple channels of stereo input and output, and allows sampling rates from 8 kHz to 48 kHz. Figure 2 shows the ADSP-21020 EZ-LAB set up for speech/audio processing applications.

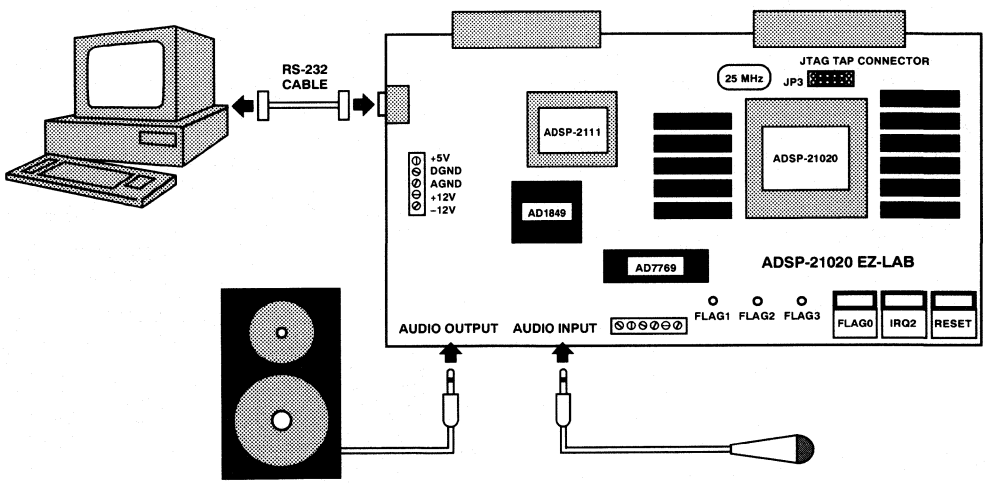


Figure 2. EZ-LAB Setup for Speech/Audio Processing Applications

The input signal to the AD1849 comes from a microphone (for speech processing), a signal generator, or any other high-impedance source. The processed signal outputs to a small speaker through the standard on-board audio amplifier. Line-level I/O is also provided.

AD7769 Analog Interface

The 2-channel, 8-bit AD7769 general purpose analog interface lets the ADSP-21020 Family processor work with sampled analog signals. For example, connect an oscilloscope to display output waveforms, and a joystick to generate input signals.

The AD7769 interfaces to the ADSP-21020 processor through four memory-mapped I/O ports (two for input, two for output).

EZ-ICE EMULATOR

Overview

EZ-ICE provides a controlled environment for observing, debugging and testing activities in a target system by connecting directly to the target processor through its JTAG interface. The emulator monitors system behavior while running at full speed; it lets you examine and alter memory locations, including processor registers and stacks.

Nonintrusive In-Circuit Emulation

The emulator does not affect target loading or timing. Nonintrusive, in-circuit emulation is assured because EZ-ICE controls the target system's processor through its IEEE 1149.1 (JTAG) Test Access Port.

Graphical User Interface

The software provides a graphical user interface identical to the simulator's. The emulator connects to an IBM PC host computer with an ISA bus plug-in board. If you are familiar with the ADSP-21000 Family simulators, operating the emulator requires little additional learning.

System Configuration Requirements

To operate the ADSP-21000 Family EZ-ICEs, you need the following minimum PC configuration:

- 386- or 486-based PC with 2MB RAM (total)
- a hard disk
- graphics card
- DOS 3.1 or higher
- an available slot for a half-size plug-in board
- mouse

Target system boards must have a JTAG connector to accept EZ-ICE's in-circuit probe.

EZ-ICE Target System Requirements

The ADSP-21000 Family EZ-ICE Emulators use the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The ADSP-21020 EZ-ICE probe requires the CLKIN, TMS, TCK, $\overline{\text{TRST}}$, TDI, TDO, and GND signals to be accessible on the target system via a 12-pin connector (pin strip header) such as that shown in Figure 3. The ADSP-21060 EZ-ICE requires an additional signal, $\overline{\text{EMU}}$ and a 14-pin connector such as that shown in Figure 4.*

*ADSP-21060 EZ-ICE. Available in Spring 1994.

The EZ-ICE probes plug directly onto these connectors for chip-on-board emulation. You must add a connector to your target board design if you intend to use one of the EZ-ICEs. Figure 5 shows the dimensions of the ADSP-21020/21010 EZ-ICE probe. Be sure to allow enough room in your system to fit the probe onto the connector.

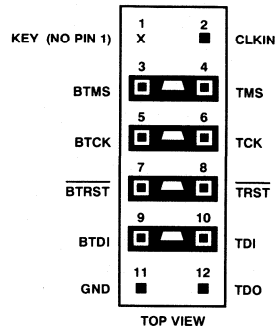


Figure 3. Target Board Connector for ADSP-21020 EZ-ICE (Jumpers in Place)

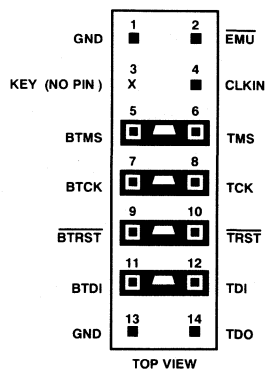


Figure 4. Target Board Connector for ADSP-21060 EZ-ICE (Jumpers in Place)

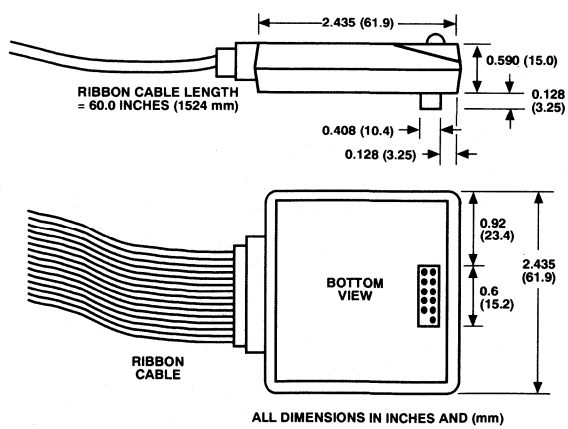


Figure 5. ADSP-21020 EZ-ICE Probe

ADSP-21000 Family Emulator Connector Specifications
The 2-row, 12-pin ADSP-21020 pin strip header is keyed at the Pin 1 location—you must remove Pin 1 from the header. The 14-pin ADSP-21060 pin strip header is keyed at the Pin 3 location—you must remove Pin 3 from the header. The pins must be 0.025 inch square and at least 0.20 inch in length. Pin spacing should be 0.1 × 0.1 inches. The tip of the pins must be at least 0.10 inch higher than the tallest component under the emulator's probe to allow clearance for the bottom of the probe. Pin strip headers are available from vendors such as 3M, McKenzie, and Samtec.

The length of the traces between the EZ-ICE probe connector and the processor's test access port pins should be as short as possible. Note that the EZ-ICE probe adds two TTL loads to the CLKIN pin.

The BMTS, BTCK, $\overline{\text{BTRST}}$, and BTDI signals are provided so that the test access port can also be used for board-level testing. When the connector is not being used for emulation, place jumpers between the BXXX pins and the XXX pins as shown in Figures 3 and 4. If you are not going to use the test access port for board test, tie $\overline{\text{BTRST}}$ to GND and tie or pull up BTCK to V_{DD}. The $\overline{\text{TRST}}$ pin must be asserted (pulsed low) after power up (through $\overline{\text{BTRST}}$ on the connector) or held low for proper operation of the processor.

Using EZ-LAB and EZ-ICE Together
Together, EZ-LAB and EZ-ICE combine to form a high speed DSP workstation with an interactive, window-based debugging interface. This setup lets you develop and test your application without any additional time investment in hardware prototyping.

In this configuration, EZ-LAB becomes the target system for EZ-ICE. From the EZ-ICE, you can download and execute programs, set breakpoints, and observe and change register and memory contents. The "Emulator port" on EZ-LAB lets EZ-ICE control the lab board's processor through the its IEEE 1149.1 (JTAG) interface.

ICEPAK Embeddable In-Circuit Emulator
The ICEPAK, a small (business card size) daughter card that contains emulator-specific hardware, incorporates emulation functionality into a plug-in target board. With ICEPAK, you can execute standard ADSP-21000 Family EZ-ICE software.

The ICEPAK interfaces to the Host with a simple 8-bit data bus, and to the target system through its JTAG test access port. The ICEPAK connector is a superset of the standard EZ-ICE target board connector.

Please call Analog's DSP Applications Assistance line at (617) 461-3672 for specifications on using ICEPAK with your target board.

2

COMBINED SOFTWARE AND HARDWARE PACKAGES

EZ-KIT Packages for the ADSP-21000 Family processors offer complete development tools sets at an affordable price.

EZ-KIT
In addition to the EZ-LAB Evaluation board, EZ-KIT contains ADSP-21000 Family Development Software: Simulator, Assembler, Linker, Librarian, and PROM Splitter. This package creates a complete development environment for programming applications in assembly language.

EZ-KIT Plus
EZ-KIT Plus contains the ADSP-21000 Family Development Software, EZ-LAB Evaluation Board, the G21K ANSI C Compiler, the C Runtime Library, and the CBUG C Source-Level Debugger for a more comprehensive set of tools for developing applications in C or in mixed C and assembly.

ADDS-210xx-TOOLS

ORDERING INFORMATION

The ADSP-21000 Family Development Software is available for IBM-compatible PCs, and SUN4 platforms. Analog Devices offers two sales packages: the DSW package includes the ADSP-21000 Family simulator, systems builder, assembler, linker and PROM splitter. The BUN package includes all the aforementioned plus the C Compiler, C Runtime Library, and CBUG C Source-Level Debugger.

ORDERING GUIDE

ADI Part Number	Description
ADDS-210xx-DSW-PC	Assembler Package and Simulator*
ADDS-210xx-BUN-PC	Assembler Package, Simulator,* and C Tools†
ADDS-210xx-C-UP	Upgrades (for owners of DSW or EZ-KIT Packages) to Include C Tools†
ADDS-210xx-BUN-SUN	Assembler Package, Simulator,* and C Tools† for the Sun4 Platform
ADDS-21020-EZ-LAB	ADSP-21020 EZ-LAB Evaluation Board
ADDS-21020-EZ-ICE	ADSP-21020 EZ-ICE Emulator‡
ADDS-21020-ICEPAK	ADSP-21020 ICEPAK Embeddable In-Circuit Emulator
ADDS-21020-EZ-KIT	ADSP-21020 EZ-LAB, Assembler Package and Simulator*
ADDS-21020-EZ-KIT-PL	ADSP-21020 EZ-LAB, Assembler Package, Simulator,* and C Tools†

NOTES
*Assembler, Assembly Library/Librarian, Linker, PROM Splitter and ADSP-21020 Simulator
†G21K C Compiler, C Runtime Library, and CBUG C Source-Level Debugger
‡EZ-ICE is also available for Japanese NEC workstations.

Sound Processing Products, Computer Audio
Contents

Introduction

Analog Devices is a world leading supplier of IC products designed specifically for adding audio and telephony features to both portable and desktop personal computers. Analog Devices has applied the technology and experience developed through many years of designing data converter products for the professional and consumer audio and communication markets. The computer audio components offered by Analog Devices include both parallel and serial port codecs. These 16-bit devices combine analog-to-digital conversion circuitry, a serial or parallel digital interface, digital-to-analog conversion circuitry, programmable input gain stages, adjustable output level control, digital and analog mixing, and on-chip digital and analog filtering. On a single silicon substrate, Analog Devices has designed codecs to satisfy advanced conversion requirements for computer applications including voice, CD quality music, synthesized music, and telephony.

Analog Devices is applying expertise gained in developing the SamplePort® family of products to the newest generation of codecs. Sample rate conversion technology allows for flexible mixing of ADC and DAC signals of different sample rates and allows the codec to instantaneously change sample rates with a resolution of 1 Hz. These new codecs use variable frequency generators to derive all internal clocks from a single crystal.

The devices are offered in plastic leaded chip carrier packages for desktop applications and thin quad flatpack packages for space constrained applications like portable computers and PCMCIA cards.

Parallel-Port Codecs

Analog Devices offers a growing line of 16-bit sigma-delta stereo codecs. The parallel-port SoundPort® codecs provide a complete single chip audio solution for business audio and multimedia applications. The parallel-port codecs are designed with a direct interface to the ISA and EISA computer buses.

Parallel-Port SoundPort Multimedia Codec Selection Guide

Device	AD1845	AD1846	AD1848K
Resolution (Bits)	16	16	16
Parallel-Bus Interface	ISA/EISA	ISA/EISA	ISA/EISA
Dynamic Range (dB)	80 min	70 min	80 min
ADC Channels	2	2	2
DAC Channels	2	2	2
Play/Capture 16 Sample FIFOs	Yes	–	–
8-Bit DMA Operation	Yes	Yes	Yes
Full Duplex Operation	Yes	Yes	Yes
Sample Rates (kHz)	4–50	5.5–48	5.5–48
Timer	Yes	–	–
Mixer	MPC-2+	MPC-1	MPC-1
Mono In/Out	Yes	–	–
Sample Rate Conversion	Yes	–	–
Digital/Analog Supply (V)	3.3/5 or 5/5	5/5	5/5
Power, typ (mW)	600	600	600
Power-Down Modes	6	1	1
PLCC Package (Pins)	68	68	68
TQFP Package (Pins)	64	NA	64

Serial-Port Codecs

The introduction of business audio has increased the demand for PC-based advanced real-world signal processing. Analog Devices has designed codec IC solutions that satisfy the analog-to-digital and digital-to-analog conversion requirements for audio, data and telephony applications.

Many applications require the use of digital signal processors or application specific signal processors in personal computer communication architectures. Signal processors communicate via a serial port, and consequently these new PC-based designs require codecs with a serial interface. Analog Devices offers a family of serial-port codecs specifically designed to interface to DSPs, dedicated signal processors and bus interface ASICs. These serial-port audio codecs use either a time division multiplexing scheme, or a version of the Concentrated Highway Interface to implement their serial bus interfaces.

In addition to providing audio stereo capture and playback, Analog Devices offers codecs with built-in telephony functionality. A single codec, the AD1843, can provide all A/D and D/A conversion requirements for concurrent audio and telephony modem communications.

Serial-Port SoundPort Multimedia Codec Selection Guide

Device	AD1843	AD1847	AD1849K
Resolution (Bits)	16	16	16
Serial-Bus Interface	DSP	DSP	CHI
Dynamic Range (dB)	80 min	70 min	80 min
Sample Rates (kHz)	4–54	5.5–48	5.5–48
ADC Channels	2	2	2
DAC Channels	4	2	2
Mixer	MPC-2+	MPC-1	MPC-1
PLL	3	–	–
Mono In/Out	Yes	–	–
Headphone Driver	Yes	–	Yes
Mono Speaker Driver	–	–	Yes
Sample Rate Conversion	Yes	–	–
Digital/Analog Supply (V)	3.3/5 or 5/5	5/5	3.3/5 or 5/5
Power, typ (mW)	TBD	500	500
PLCC Package (Pins)	NA	44	44
TQFP Package (Pins)	100	44	44
PQFP Package (Pins)	80	NA	NA

Bulletin Board Service

Analog Devices offers complete codec support for the Microsoft Windows 3.1, Windows NT, Win95, and the IBM OS/2 environments. SoundPort drivers and demonstration applets that control full duplex capture and playback operation, data formatting, and mixing functions are available on the BBS.

To access Analog Devices' DSP Bulletin Board Service, call 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

Serial-Port 16-Bit SoundComm Codec

AD1843

FEATURES

Single Chip Integrated Speech, Audio, Fax and Modem Codec
Highly Configurable Stereo ΣΔ ADCs and Quad ΣΔ DACs
Supports V.34, V.32bis, V.29, V.17 and Fallback Fax and Modem Standards As Well As Voice Over Data
Dual Digital Resamplers with Programmable Input and Output Phase and Frequency
Three On-Chip Phase Lock Loops for Synchronization to External Signals, Including Video
Thirteen Analog Inputs and Seven Analog Outputs
Advanced Analog and Digital Signal Mixing and Digital-to-Digital Sample Rate Conversion
Programmable Gain, Attenuation and Mute
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low Pass
1 Hz Resolution Programmable Sample Rates from 4 kHz to 54 kHz Derived from a Single Clock Input
80-Lead PQFP and 100-Lead TQFP Packages
Operation from +5 V or Mixed +5 V/+3 V Supplies
FIFO-Buffered Serial Digital Interface Compatible with ADSP-21xx Fixed-Point DSPs
Advanced Power Management
VHDL Model of AD1843 Serial Port Available

GENERAL PRODUCT DESCRIPTION

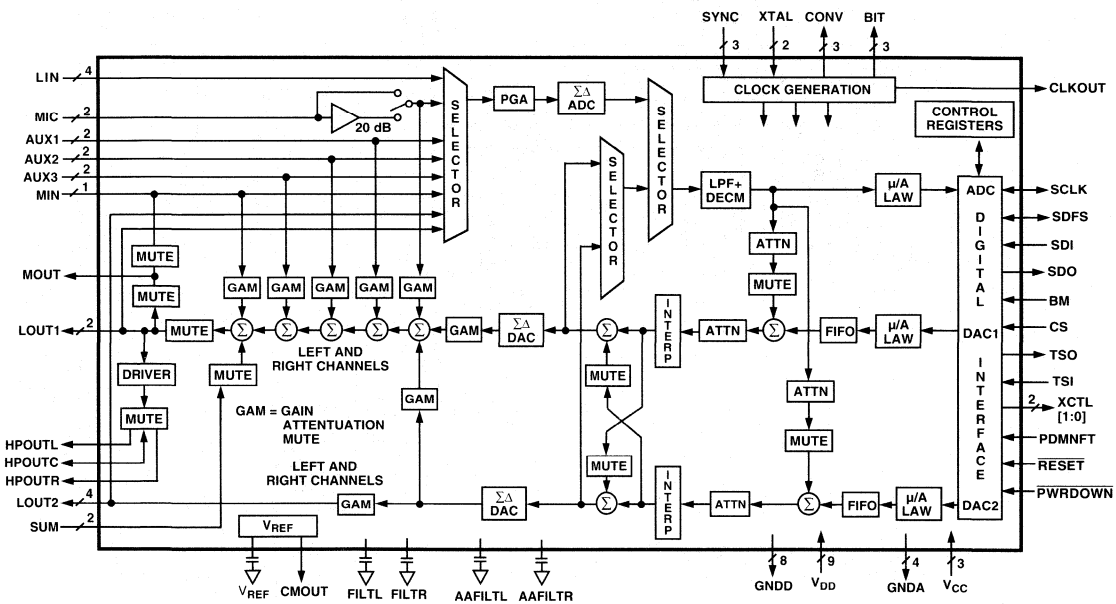
The AD1843 SoundComm™ is a complete analog front end for high performance DSP-based telephony and audio applications. The device integrates the real-world analog I/O requirements for many popular functions thereby reducing size, power consumption, and system complexity.

The main elements of the AD1843 are its extensive input and mixing section, its two channels of sigma-delta (ΣΔ) analog-to-digital conversion, its four channels of ΣΔ digital-to-analog conversion, its digital filters, and the control circuitry for implementing the device's different modes. The AD1843 permits flexible sample-rate selection through programming and external synchronization, many input and output options, and many mixing options.

The versatility of the device is demonstrated by the following examples of functions it can perform:

- Stereo audio input and quad output, simultaneously at different sample rates
- Stereo audio output with simultaneous modem or fax functions
- Mono audio input and output with simultaneous modem receive and transmit for simultaneous voice and data communications
- Dual independent audio input with audio output for full duplex acoustic echo-cancelling speakerphones

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM



This is a preliminary data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

SoundComm is a trademark of Analog Devices, Inc.

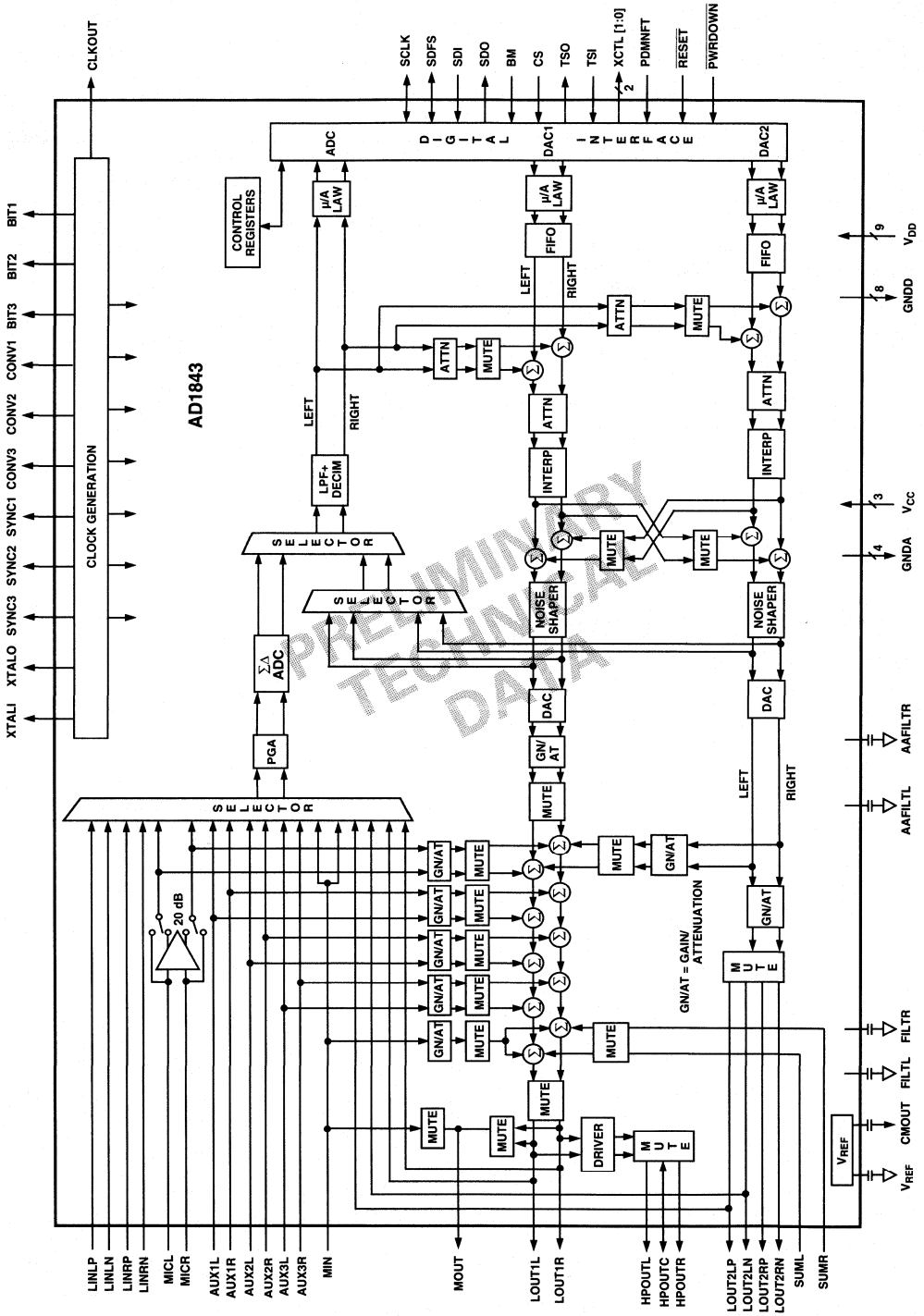


Figure 1. Detailed Functional Block Diagram

Parallel-Port 16-Bit SoundPort Stereo Codec

AD1845

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Supports the Microsoft Windows Sound System*
MPC Level-2+ Compliant Mixing
16 mA Bus Drive Capability
Supports Two DMA Channels for Full Duplex Operation
On-Chip Capture and Playback FIFOs
Advanced Power-Down Modes
Programmable Gain and Attenuation
Sample Rates from 4.0 kHz to 50 kHz Derived from a Single Clock or Crystal Input
68-Lead PLCC, 100-Lead TQFP Packages
Operation from +5 V or Mixed 5 V/3.3 V Supplies
Byte-Wide Parallel Interface to ISA and EISA Buses
Pin Compatible with AD1848, AD1846, CS4248, CS4231

PRODUCT OVERVIEW

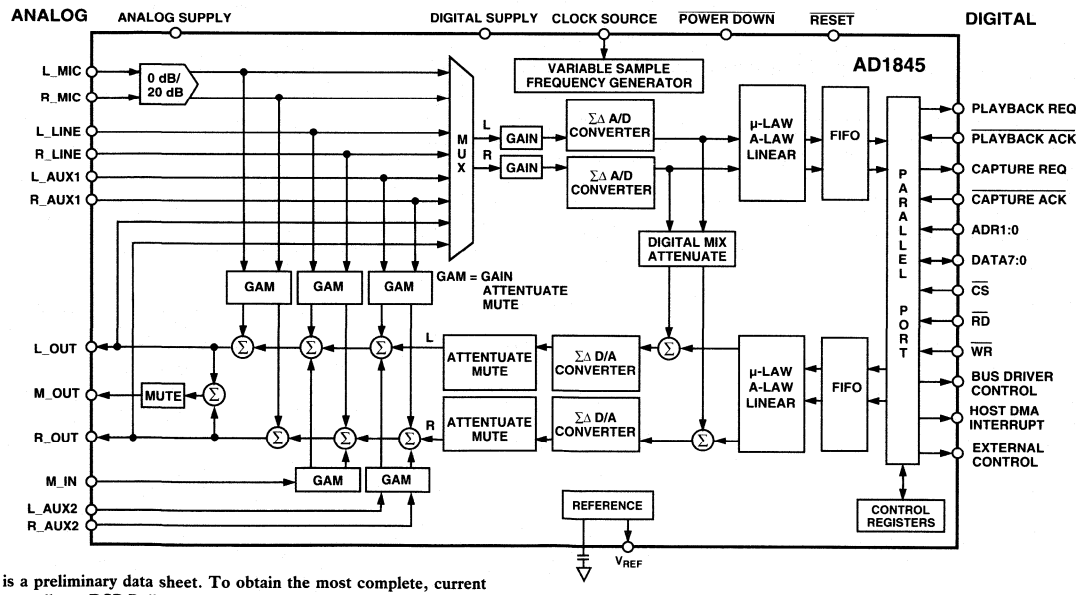
The Parallel Port AD1845 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1845 provides a complete, single chip computer audio solution for business audio and multimedia applications. The codec includes stereo audio converters, complete on-chip filtering, MPC Level-2 compliant analog mixing, programmable gain, attenuation and mute, a variable sample frequency generator, FIFOs, and supports advanced power-down modes. It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card.

The AD1845 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct and indirect addressing of thirty-seven internal control registers over this asynchronous interface. The AD1845 includes dual DMA count registers for full duplex operation enabling the AD1845 to capture data on one DMA channel and play back data on a separate channel. The FIFOs on the AD1845 reduce the risk of losing data when making DMA transfers over the ISA/EISA bus. The FIFOs buffer data transfers and allow for relaxed timing in acknowledging requests for capture and playback data.

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 4 kHz to 50 kHz are supported from a single external crystal or clock source.

*Windows Sound System is a registered trademark of Microsoft Corporation.
SoundPort is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



This is a preliminary data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1845–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Word Rate (F_S)	48	kHz
Input Signal	1008	Hz
Analog Output Passband	20 Hz to 20 kHz	
ADC FFT Size	2048	
DAC FFT Size	2048	
V_{IH}	2.4	V
V_{IL}	0.8	V
V_{OH}	2.4	V
V_{OL}	0.4	V

DAC Output Conditions
Calibrated
–1.0 dB Relative to Full Scale
16-Bit Linear Mode
10 kΩ Output Load
Mute Off, OL = 0

ADC Input Conditions
Calibrated
0 dB Gain
–1.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode

ANALOG INPUT

	Min	Typ	Max	Units
Input Voltage (RMS Values Assume Sine Wave Input)				
Line		1		V rms
	2.66	2.8	2.94	V p-p
MIC with +20 dB Gain (MGE = 1)		0.1		V rms
	0.266	0.28	0.294	V p-p
MIC with 0 dB Gain (MGE = 0)		1		V rms
	2.66	2.8	2.94	V p-p
Input Impedance*	10	17		kΩ
Input Capacitance		15		pF

PROGRAMMABLE GAIN AMPLIFIER–ADC

	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested)	1.3	1.5	1.7	dB
PGA Gain Range Span	21.5	22.5	23.5	dB

AUXILIARY LINE, MONO, AND MICROPHONE INPUT ANALOG GAIN/AMPLIFIERS/ATTENUATORS

	Min	Typ	Max	Units
Step Size (+12 dB to –34.5 dB): AUX1, AUX2, LINE, MIC (All Steps Tested)	1.3	1.5	1.7	dB
Step Size (0 dB to –45 dB): M_IN (All Steps Tested)	2.6	3.0	3.4	dB
Input Gain/Attenuation Range	45.5	46.5	47.5	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	$0.4 \times F_S$	Hz
Passband Ripple		±0.1	dB
Transition Band	$0.4 \times F_S$	$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$15/F_S$	
Group Delay Variation Over Passband		0.0	µs

*Guaranteed not tested.

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	80	86		dB
THD+N (Referenced to Full Scale)			0.022	%
		–77	–73	dB
Signal-to-Intermodulation Distortion*			90	dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		–90	–80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read ADC)		–90	–80	dB
Line to AUX1		–90	–80	dB
Line to AUX2		–90	–80	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±5	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			50	LSBs

3

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (–60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	80	87		dB
THD+N (Referenced to Full Scale)			0.022	%
		–76	–74	dB
Signal-to-Intermodulation Distortion*			90	dB
Gain Error (Full-Scale Span Relative to Nominal Output Voltage)			±5	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			–80	dB
Total Out-of-Band Energy (Measured from $0.6 \times F_S$ to 100 kHz)*			–45	dB
Audible Out-of-Band Energy (Measured from $0.6 \times F_S$ to 20 kHz)*			–70	dB

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to –22.5 dB)	1.3	1.5	1.7	dB
Step Size (–22.5 dB to –94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation Range Span*	93.5	94.5	95.5	dB

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Output Voltage		0.707		V rms
OL = 0	1.85	2.0	2.1	V p-p
OL = 1	2.6	2.8	3.0	V p-p
Output Impedance*			600	Ω
External Load Impedance	10			kΩ
Output Capacitance*			15	pF
External Load Capacitance			100	pF
V_{REF}	2.10	2.25	2.40	V
V_{REF} Current Drive		100		μA
V_{REF} Output Impedance		4		kΩ
Mute Attenuation of 0 dB Fundamental* (L_OUT, R_OUT, M_OUT)			–80	dB
Mute Click (|Muted Output Minus Unmuted Midscale DAC Output|)			5	mV

*Guaranteed not tested.

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
System Frequency Response Ripple (Line In to Line Out)*			1.0	dB
Differential Nonlinearity*			±1	LSB
Phase Linearity Deviation*			5	Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4		V
XTAL1I	2.4		V
Low Level Input Voltage (V_{IL})		0.8	V
High Level Output Voltage (V_{OH})	2.4		V
Low Level Output Voltage (V_{OL})		0.4	V
Input Leakage Current	–10	10	µA
Output Leakage Current	–10	10	µA

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE, $V_{DD} = V_{CC} = 5.0$ V)

	Min	Max	Units
$\overline{WR}/\overline{RD}$ Strobe Width (t_{STW})	90		ns
$\overline{WR}/\overline{RD}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{BWND})	80		ns
Write Data Setup to $\overline{WR}$ Rising (t_{WDSU})	22		ns
$\overline{RD}$ Falling to Valid Read Data (t_{RDDV})	30	70	ns
$\overline{CS}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{CSSU})	10		ns
$\overline{CS}$ Hold from $\overline{WR}/\overline{RD}$ Rising (t_{CSHD})	0		ns
Adr Setup to $\overline{WR}/\overline{RD}$ Falling (t_{ADSU})	10		ns
Adr Hold from $\overline{WR}/\overline{RD}$ Rising (t_{ADHD})	10		ns
$\overline{DAK}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{SUDK1})	60		ns
$\overline{DAK}$ Falling to $\overline{WR}/\overline{RD}$ Rising (t_{SUDK2})	0		ns
$\overline{DAK}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{DKSU})	25		ns
Data Hold from $\overline{RD}$ Rising (t_{DHD1})	0	20	ns
Data Hold from $\overline{WR}$ Rising (t_{DHD2})	15		ns
DRQ Hold from $\overline{WR}/\overline{RD}$ Falling (t_{DRHD})	0	25	ns
$\overline{DAK}$ Hold from $\overline{WR}$ Rising (t_{DKHDa})	20		ns
$\overline{DAK}$ Hold from $\overline{RD}$ Rising (t_{DKHDb})	20		ns
$\overline{DBEN}$/DBDIR Delay from $\overline{WR}/\overline{RD}$ Falling (t_{DBDL})	0	30	ns
$\overline{PWRDWN}$ and $\overline{RESET}$ Low Pulse Width	300		ns

*Guaranteed not tested.

POWER SUPPLY

	Min	Max	Units
Power Supply Range–Digital and Analog	4.75	5.25	V
Power Supply Current–5 V Operating		120	mA
Analog Supply Current–5 V Operating (10 kΩ Load)		65	mA
Digital Supply Current–5 V Operating		55	mA
Power Dissipation–5 V Operating (Current × Nominal Supplies)		600	mW
Total Power Down Supply Current		30	mA
Power Down Supply Current		2	mA
Reset Supply Current		2	mA
Standby Mode Supply Current (ADC and DAC Power Down or ADC and Mixer Power Down)		36	mA
ADC Power Down Supply Current		80	mA
DAC Power Down Supply Current		85	mA
Mixer Power Down Supply Current		70	mA
Mixer Only Supply Current		52	mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, both ADCs and DACs)		TBD	dB

3

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency		33	MHz
Recommended Clock Duty Cycle	10	90	%
Power Up Initialization Time		310	ms

*Guaranteed, not tested.
Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1845JP	0°C to +70°C	68-Lead PLCC	P-68A
AD1845JST	0°C to +70°C	100-Lead TQFP	ST-100

*For outline information see Package Information section.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	–0.3	6.0	V
Analog (V_{CC})	–0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	–0.3	(V_{CC}) +0.3	V
Digital Input Voltage (Signal Pins)	–0.3	(V_{DD}) +0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	–65	+150	°C

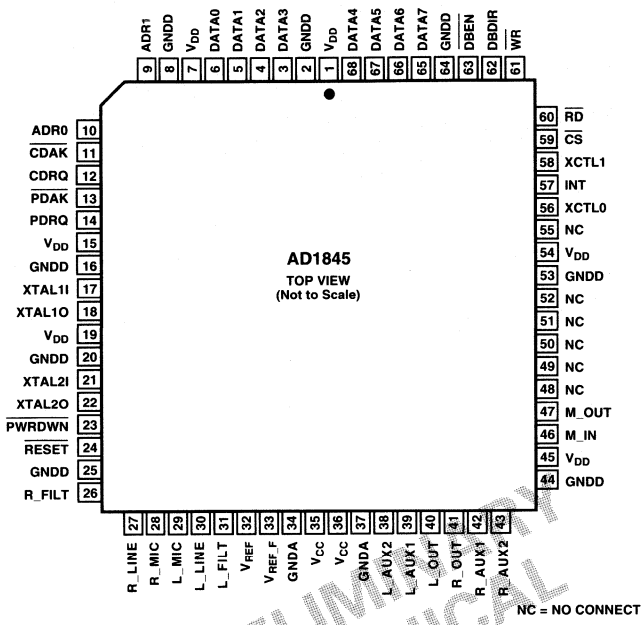
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1845 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

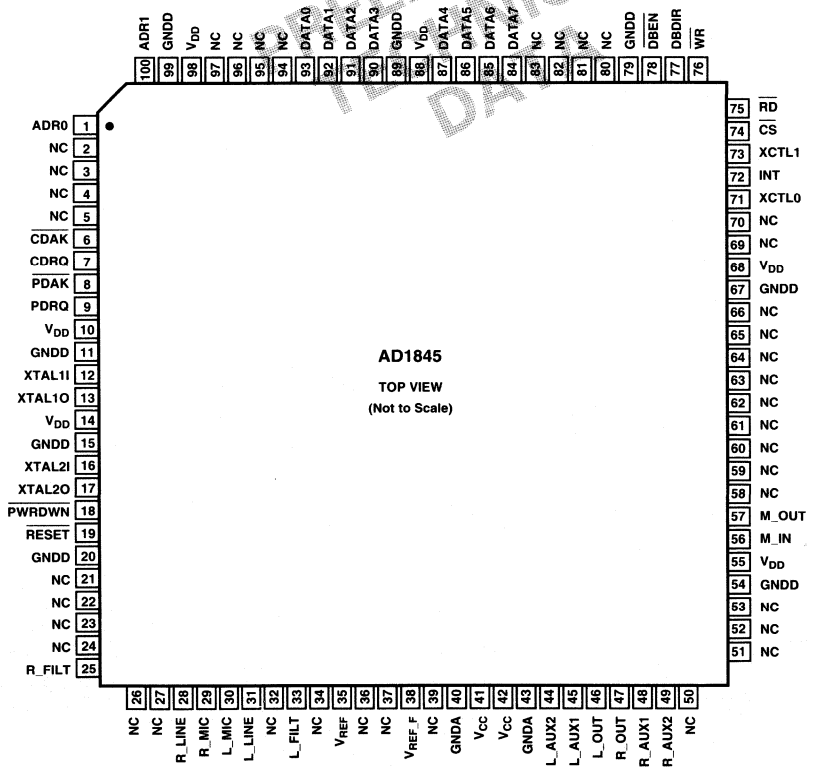
PIN LOCATIONS

68-Lead PLCC



NC = NO CONNECT

100-Lead TQFP



NC = NO CONNECT

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

PIN DESCRIPTION

Parallel Interface

Pin Name	PLCC	TQFP	I/O	Description
CDRQ	12	7	O	Capture Data Request. The assertion of this signal HI indicates that the codec has a captured audio sample from the ADC ready for transfer. This signal will remain asserted until the internal capture FIFO is empty.
$\overline{\text{CDAK}}$	11	6	I	Capture Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.
PDRQ	14	9	O	Playback Data Request. The assertion of this signal HI indicates that the codec is ready for more DAC playback data. The signal will remain asserted until the internal playback FIFO is full.
$\overline{\text{PDAK}}$	13	8	I	Playback Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.
ADR1:0	9 & 10	1 & 100	I	Codec Addresses. These address pins are asserted by the codec interface logic during a control register/PIO access. The state of these address lines determine which direct register is accessed.
$\overline{\text{RD}}$	60	75	I	Read Command Strobe. This active LO signal defines a read cycle from the codec. The cycle may be a read from the control/PIO registers, or the cycles could be a read from the codec's DMA sample registers.
$\overline{\text{WR}}$	61	76	I	Write Command Strobe. This active LO signal indicates a write cycle to the codec. The cycle may be a write to the control/PIO registers, or the cycle could be a write to the codec's DMA sample registers.
$\overline{\text{CS}}$	59	74	I	AD1845 Chip Select. The codec will not respond to any control/PIO cycle accesses unless this active LO signal is LO. This signal is ignored during DMA transfers.
DATA7:0	3–6 & 65–68	84–87 & 90–93	I/O	Data Bus. These pins transfer data and control information between the codec and the host.
$\overline{\text{DBEN}}$	63	78	O	Data Bus Enable. This pin enables the external bus drivers. This signal is normally HI. For control register/PIO cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ *or* $\overline{\text{RD}}$) *and* $\overline{\text{CS}}$ For DMA cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ *or* $\overline{\text{RD}}$) *and* ($\overline{\text{PDAK}}$ *or* $\overline{\text{CDAK}}$).
DBDIR	62	77	O	Data Bus Direction. This pin controls the direction of the data bus transceiver. HI enables writes from the host bus to the AD1845; LO enables reads from the AD1845 to the host bus. This signal is normally HI. For control register/PIO cycles, DBDIR = $\overline{\text{RD}}$ *and* $\overline{\text{CS}}$ For DMA cycles, DBDIR = $\overline{\text{RD}}$ *and* ($\overline{\text{PDAK}}$ *or* $\overline{\text{CDAK}}$).

Analog Signals

Pin Name	PLCC	TQFP	I/O	Description
L_LINE	30	31	I	Left Line Input.
R_LINE	27	28	I	Right Line Input.
L_MIC	29	30	I	Left Microphone Input. This signal can be either line level or –20 dB from line level (using the on-chip 20 dB gain block).
R_MIC	28	29	I	Right Microphone Input. This signal can be either line level or –20 dB from line level (using the on-chip 20 dB gain block).
L_AUX1	39	45	I	Left Auxiliary #1 Line Input.
R_AUX1	42	48	I	Right Auxiliary #1 Line Input.
L_AUX2	38	44	I	Left Auxiliary #2 Line Input.
R_AUX2	43	49	I	Right Auxiliary #2 Line Input.
L_OUT	40	46	O	Left Line Level Output.
R_OUT	41	47	O	Right Line Level Output.
M_IN	46	56	I	Mono Input.
M_OUT	47	57	O	Mono Output.

Miscellaneous

Pin Name	PLCC	TQFP	I/O	Description
XTAL1I	17	12	I	24.576 MHz Crystal #1 Input.
XTAL1O	18	13	O	24.576 MHz Crystal #1 Output.
XTAL2I	21	16		Not used on the AD1845.
XTAL2O	22	17		Not used on the AD1845.
$\overline{\text{PWRDWN}}$	23	18	I	Power Down Signal. Active LO places the AD1845 in its lowest power consumption mode. All sections of the AD1845, including the digital interface, are shut down and consume minimal power.
INT	57	72	O	Host Interrupt Pin. A host interrupt is generated to notify the host that a specified event has occurred.
XCTL1:0	56 & 58	71 & 73	O	External Control. These signals reflect the current status of register bits inside the AD1845. They can be used for signaling or to control external logic.
$\overline{\text{RESET}}$	24	19	I	Reset. Active LO resets all digital registers and filters, and resets all analog filters. Active LO places the AD1845 in the lowest power consumption mode. XTAL1 is required to be running during the minimum low pulse width of the reset signal.
V_{REF}	32	35	O	Voltage Reference. Nominal 2.25 volt reference available for dc-coupling and level-shifting. V_{REF} should not be used to sink or source current.
V_{REF_F}	33	38	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only.
L_FILT	31	33	I	Left Channel Filter. This pin requires a 1.0 µF capacitor to analog ground for proper operation.
R_FILT	26	25	I	Right Channel Filter. This pin requires a 1.0 µF capacitor to analog ground for proper operation.
NC	48–52, 55	2–5, 21–24 26, 27, 32, 34, 36, 37, 39, 51–53, 58–66, 69, 70, 80–83, 94–97		No connect. Do not connect.

Power Supplies

Pin Name	PLCC	TQFP	I/O	Description
V_{CC}	35 & 36	41 & 42	I	Analog Supply Voltage (+5 V).
GNDA	34 & 37	40 & 43	I	Analog Ground.
V_{DD}	1, 7, 15, 19, 45, 54	10, 14, 55, 68, 88, 98	I	Digital Supply Voltage (+5 V/3.3 V).
GNDD	2, 8, 16, 20, 25, 44, 53, 64	11, 15, 20, 54, 67, 79, 89, 99	I	Digital Ground.

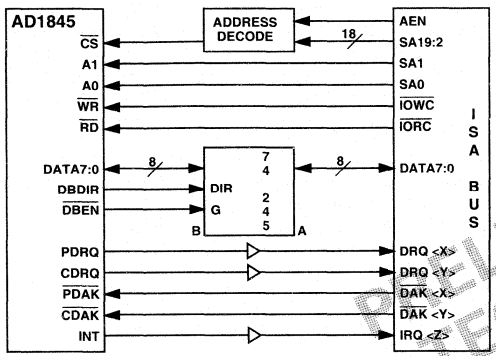


Figure 1. AD1845 Interface to ISA Bus

The AD1845 has built-in 16 mA bus drivers. If 24 mA drive capability is required, the AD1845 generates enable and direction controls for IC bus buffers such as the 74_245.

The codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. The AD1845 mixer surpasses MPC Level-2 recommendations. Inputs to the ADC can be selected from four stereo pairs of analog signals: line (LINE), microphone (MIC), auxiliary line #1 (AUX1), and post-mixed DAC output. In addition, the analog mixer allows the mono input (M_IN), MIC, AUX1, LINE and auxiliary line #2 (AUX2) signals to be mixed with the DACs' output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1845 can accept and generate 16-bit twos complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantized noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters.

The AD1845 supports multiple low power and power-down modes to support notebook and portable computing multimedia applications. The ADC, DAC, and mixer paths can be suspended independently allowing the AD1845 to be used for capture only or playback only, lessening power consumption and extending battery life.

The AD1845 includes a variable sample frequency generator, that allows the codec to instantaneously change sample rates with a resolution of 1 Hz. This feature allows the codec to instantaneously change sample rates with a resolution of 1 Hz, glitchlessly. Additionally, ΣΔ quantization noise is kept out of the 20 kHz audio band regardless of the chosen sample rate. The codec uses the variable sample frequency generator to derive all internal clocks from a single external crystal or clock source.

Expanded Mode (MODE2)

MODE1 is the initial state of the AD1845. In this state the AD1845 appears as an AD1848 compatible device. To access the expanded modes of operation on the AD1845, the MODE2 bit should be set in the Miscellaneous Information Control Register. When this bit is set to one, 16 additional indirect registers can be addressed allowing the user to access the AD1845's expanded features. The AD1845 can return to MODE1 operation by clearing the MODE2 bit.

The additional MODE2 functions are:

1. Full-Duplex DMA support.
2. MIC input mixer, mute and volume control.
3. Mono output with mute control.
4. Mono input with mixer volume control.
5. Software controlled advanced power-down modes.
6. Programmable sample rates from 4 kHz to 50 kHz in 1 Hz increments.
7. Capture/Playback FIFO enable/disable.

FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1845 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs
The AD1845 SoundPort Stereo Codec accepts stereo line-level and MIC-level inputs. The LINE, MIC, AUX1, and post-mixed DAC output are available to the ADC multiplexer. The DAC output can be mixed with LINE, MIC, AUX1, AUX2 and M_IN. Each channel of the MIC inputs can be amplified by +20 dB prior to the PGA to compensate for the voltage swing difference between line levels and typical condenser microphone levels.

Analog Mixing
The M_IN mono input signal, MIC, LINE, AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary, line or MIC analog input can be independently gained/attenuated from +12 dB to –34.5 dB in 1.5 dB steps or completely muted. The mono input signal, M_IN, can be gain/attenuated from 0 dB to –45 dB in 3 dB steps or muted. The post-mixed DAC output is available on L_OUT and R_OUT externally and also to the ADC input multiplexer.

Even if the AD1845 is not playing back data from its DACs, the analog mix function can still be active.

M_IN allows the analog signal intended for the PC speaker to be passed through, attenuated or mixed with the other analog inputs and the DAC output of the AD1845. M_IN can also be used to accept other mono input sources.

Analog-to-Digital Datapath
The PGA following the input multiplexer allows independent selectable gains for each channel from 0 dB to 22.5 dB in +1.5 dB steps. The codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

The AD1845 ΣΔ ADCs incorporate a fourth-order modulator. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high over-sampling ratio. The ADCs include linear-phase digital decimation filters that low-pass filter the input to $0.4 \times F_S$. ("F_S" is the word rate or "sampling frequency.") ADC input overrange conditions will cause bits to be set that can be read.

Digital-to-Analog Datapath
The ΣΔ DACs are preceded by a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter oversamples and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to –94.5 dB in –1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output. No external components are required.

Changes in DAC output attenuation take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise on playback. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48 milliseconds at an 8 kHz sampling rate. (Time-out [ms] ≈ $384 \div F_S$ [kHz].)

Digital Mixing
Stereo digital output from the ADCs can be mixed digitally with the input to the DACs. Digital output from the ADCs going out of the data port is unaffected by the digital mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the digital mix datapath data are attenuated by the same amount. (Note that internally the AD1845 always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixty-four steps of –1.5 dB attenuation are supported to –94.5 dB. The digital mix datapath can also be completely muted. Note that the level of the mixed signal is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators.

In case the AD1845 is capturing data but ADC output data is not removed in time ("ADC overrun"), then the last sample captured before overrun will be used for the digital mix. In case the AD1845 is playing back data but input digital DAC data fails to arrive in time ("DAC underrun"), then a midscale zero will be added to the digital mix data when the DACZ control bit is set to 0, otherwise, the DAC will output the previous valid sample in an underrun condition.

Analog Outputs
A stereo line-level output is available at external pins. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near V_{REF}, the midscale reference voltage. The output is selectable for 2.0 V peak-to-peak or 2.8 V peak-to-peak.

Digital Data Types
The AD1845 supports four global data types: 16-bit twos complement linear PCM, 8-bit unsigned linear PCM, companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. All data formats that are less than 16-bits are properly aligned to insure the utilization of full system resolution.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large-amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

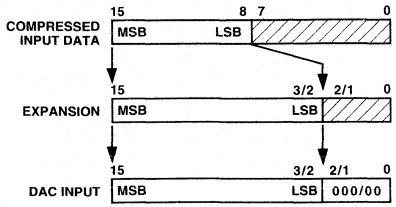


Figure 2. μ-Law or A-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified.

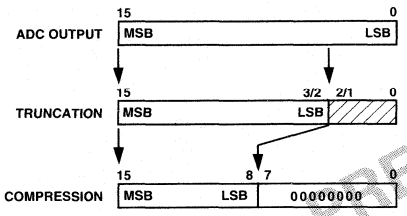


Figure 3. μ-Law or A-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1845 always uses 16-bit linear PCM representations to maintain maximum precision.

Timer Registers

The timer registers are provided for system level synchronization, and for periodic interrupt generation. The 16-bit timer time base is determined by the frequency of the connected input clock source.

The timer is enabled by setting the Timer Enable bit, TE, in the Alternate Feature Enable register. To set the timer, load the Upper and Lower Timer Bits Registers. The timer value will then be loaded into an internal count register with a value of approximately 10 μs (the exact timer value is listed in the register descriptions). The internal count register will decrement until it reaches zero, then the Timer Interrupt bit, TI, is set and an interrupt will be sent to the host. The next timer clock will load the internal count register with the value of the Timer Register, and the timer will be reinitialized. To clear the interrupt, write to the Status Register or write a "0" to TI.

Interrupts

The INT bit, located in the Status Register, is set when the AD1845 cannot respond to parallel bus cycle. The INT sticky bit indicates the status of the AD1845's internal interrupt logic. This bit is cleared by any host write of any value to the Status Register. The IEN bit of the Pin Control Register determines whether the interrupt pin responds to an interrupt condition and reflects the interrupt state on INT. The AD1845 supports interrupt conditions generated by DMA playback count expiration, DMA capture count expiration, or timer expiration. The INT bit will remain set, HI, until a write has been completed to the Status Register or by clearing the TI, CI, or PI bit (depending on the existing condition) in the Capture Playback Timer Register.

Power Supplies and Voltage Reference

The AD1845 operates from a +5 V power supply. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single-supply systems. A voltage reference is included on the codec and its 2.25 V buffered output is available on an external pin (V_{REF}). The reference output can be used for biasing op amps used in dc coupling. The internal reference is externally bypassed to analog ground at the V_{REF_F} pin.

Clocks and Sample Rates

The AD1845 operates from a single external crystal or clock source. From a single input, a wide range of sample rates can be generated. The AD1845 default frequency source is a 24.576 MHz input. The AD1845 can also be driven from a 14.31818 MHz (OSC), 24.00 MHz, 25 MHz or 33 MHz input frequency source. In MODE1, the input drives the internal variable sample frequency generator to derive the following AD1848 compatible sample rates: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz. In MODE2, the AD1845 can be programmed to generate any sample frequency between 4 kHz and 50 kHz with 1 Hz resolution. Note that it is no longer required to enter Mode Change Enable (MCE) to change the sample rate. This feature allows the user to change the AD1845's sample rate "on the fly."

CONTROL REGISTERS

Control Register Architecture

The AD1845 SoundPort Stereo Codec accepts both data and control information through its byte-wide parallel port. Indirect addressing minimizes the number of external pins required to access all 37 of its byte-wide internal registers. Only two external address pins, ADR1:0, are required to accomplish all data and control transfers. These pins select one of five direct registers. (ADR1:0 = 3 addresses two registers, depending on whether the transfer for a playback or capture.)

ADR1:0	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Registers

Figure 4. AD1845 Direct Register Map

A write to or a read from the Indexed Data Register will access the Indirect Register which is indexed by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 32 Indirect Registers indexes are shown in Figure 5:

Index	Register Name	Reset/Default State	
0	Left Input Control	000x	0000
1	Right Input Control	000x	0000
2	Left Aux #1 Input Control	1xx0	1000
3	Right Aux #1 Input Control	1xx0	1000
4	Left Aux #2 Input Control	1xx0	1000
5	Right Aux #2 Input Control	1xx0	1000
6	Left Output Control	1xx0	0000
7	Right Output Control	1xx0	0000
8	Clock and Data Format	x000	0000
9	Interface Configuration	00xx	1000
10	Pin Control	00xx	xx00
11	Test and Initialization	0000	0000
12	Miscellaneous Information	1000	1010
13	Digital Mix/Attenuation	0000	00x0
14	Upper Base Count	0000	0000
15	Lower Base Count	0000	0000
16	Alternate Feature Enable/Left MIC Input Control	0001	0001
17	MIC Mix Enable/Right MIC Input Control	0001	000x
18	Left Line Gain, Attenuate, Mute, Mix	1xx0	1000
19	Right Line Gain, Attenuate, Mute, Mix	0000	0000
20	Lower Timer	0000	0000
21	Upper Timer	0000	0000
22	Upper Frequency Select	0001	1111
23	Lower Frequency Select	0100	0000
24	Capture Playback Timer	x000	x000
25	Revision ID		
26	Mono Control	00xx	0011
27	Power-Down Control	000x	0xxx
28	Capture Data Format Control	x000	xxxx
29	Crystal Clock Select/Total Power-Down	000x	xxx0
30	Capture Upper Base Count	0000	0000
31	Capture Lower Base Count	0000	0000

"X" indicates reserved bit.

Figure 5. AD1845 Indirect Register Map and Default States

Low Cost Parallel-Port 16-Bit SoundPort Stereo Codec

AD1846

FEATURES

Low Cost, Pin- and Register-Compatible Alternative to AD1848
Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Supports the Microsoft Windows Sound System*
Multiple Channels of Stereo Input and Output
Analog and Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
68-Lead PLCC Package
Operation from +5 V Supply
Byte-Wide Parallel Interface to ISA and EISA Buses
Supports One or Two DMA Channels and Programmed I/O

PRODUCT OVERVIEW

The Parallel-Port AD1846 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1846 is intended to provide a complete, single-chip audio solution for business audio and multimedia applications requiring operation from a single +5 V supply.

*Windows Sound System is a trademark of Microsoft Corp.
SoundPort is a registered trademark of Analog Devices, Inc.

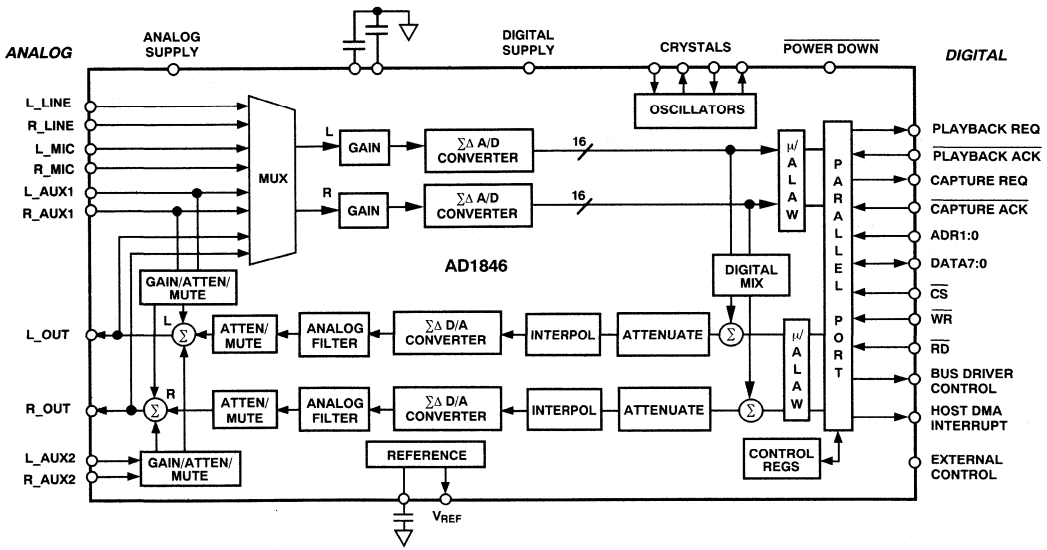
It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card. The AD1846 generates enable and direction controls for IC buffers such as the 74_245.

The AD1846 SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct and indirect addressing of twenty-one internal control registers over this asynchronous interface.

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. DAC dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Inputs to the ADC can be selected from four stereo pairs of analog signals: line, microphone ("mic"), auxiliary ("aux") line #1, and post-mixed DAC output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1846—SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Word Rate (F_S)	48	kHz
Input Signal	1007	Hz
Analog Output Passband	20 Hz to 20 kHz	
FFT Size	4096	
V_{IH}	2.4	V
V_{IL}	0.8	V
V_{OH}	2.4	V
V_{OL}	0.4	V

DAC Output Conditions
Post-Autocalibrated
0 dB Attenuation
Full Scale (0 dB)
16-Bit Linear Mode
No Output Load
Mute Off

ADC Input Conditions
Post-Autocalibrated
0 dB Gain
−1.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode
Inputs Driven with Low Impedance (≈ 50 Ω) Source

ANALOG INPUT

	Min	Typ	Max	Units
Full Scale Input Voltage (RMS Values Assume Sine Wave Input)				
Line		1		V rms
	2.5	2.8	3.1	V p-p
Mic		1		V rms
MGE = 0	2.5	2.8	3.1	V p-p
MGE = 1	0.29	0.36	0.43	V p-p
Input Impedance	100			kΩ
Input Capacitance			15	pF

PROGRAMMABLE GAIN AMPLIFIER—ADC

	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested)	1.0	1.5	2.0	dB
PGA Gain Range Span	21.0	22.5	24.0	dB

AUXILIARY INPUT ANALOG AMPLIFIERS/ATTENUATORS

	Min	Typ	Max	Units
Step Size (+12 dB to −28.5 dB, Referenced to DAC Full Scale)	1.3	1.5	1.7	dB
(−30 dB to −34.5 dB, Referenced to DAC Full Scale)	1.0	1.5	2.0	dB
Auxiliary Gain/Attenuation Range Span	45.5	46.5	47.5	dB
Auxiliary Input Impedance*	10			kΩ

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	$0.4 \times F_S$	Hz
Passband Ripple		±0.1	dB
Transition Band	$0.4 \times F_S$	$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$30/F_S$	
Group Delay Variation Over Passband		0.0	μs

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	70	75		dB
THD+N (Referenced to Full Scale)			0.02	%
		−72	−70	dB
Signal-to-Intermodulation Distortion		83		dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)			−80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read Both Channels)			−80	dB
Line to AUX1			−80	dB
Line to AUX2			−80	dB
Gain Error (Full-Scale Span Relative to Nominal Input Voltage)			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			12	mV

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale, A-Weighted)	80	83		dB
THD+N (Referenced to Full Scale)			0.02	%
		−73	−70	dB
Signal-to-Intermodulation Distortion		86		dB
Gain Error (Full-Scale Span Relative to Nominal Output Voltage)			±10	%
Interchannel Gain Mismatch (Difference of L and R Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			−80	dB
Total Out-of-Band Energy* (Measured from $0.6 \times F_S$ to 96 kHz)			−50	dB
Audible Out-of-Band Energy* (Measured from $0.6 \times F_S$ to 20 kHz, Tested at 5.5 kHz)			−70	dB

*Guaranteed Not Tested.
Specifications subject to change without notice.

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to −60 dB) (Tested at Steps 0 dB, −19.5 dB and −60 dB)	1.3	1.5	1.7	dB
Step Size (−60 dB to −94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation Range Span*	93.5	94.5	95.5	dB

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Output Voltage		0.707		V rms
	1.8	2.0	2.2	V p-p
Output Impedance*			600	Ω
External Load Impedance	10			kΩ
Output Capacitance*			15	pF
External Load Capacitance			100	pF
V_{REF}	2.00	2.25	2.50	V
V_{REF} Current Drive		100		μA
V_{REF} Output Impedance		4		kΩ
Mute Attenuation of 0 dB Fundamental* (OUT)			−80	dB
Mute Click (|Muted Output Minus Unmuted Midscale DAC Output|)			5	mV

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
Peak-to-Peak Frequency Response Ripple* (Line In to Line Out)			1.0	dB
Differential Nonlinearity*			±1	Bit
Phase Linearity Deviation*			5	Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4	(V_{DD}) + 0.3	V
XTAL1/2I	2.4	(V_{DD}) + 0.3	V
Low Level Input Voltage (V_{IL})	−0.3	0.8	V
High Level Output Voltage (V_{OH}) at I_{OH} = −2 mA	2.4		V
Low Level Output Voltage (V_{OL}) at I_{OL} = 2 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	−10	10	μA
Output Leakage Current (GO/NOGO Tested)	−10	10	μA

DIGITAL MIX ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to −94 dB) (Tested at Steps 0 dB, −19.5 dB)	1.0	1.5	2.0	dB
Output Attenuation Range Span*	−93.5		95.5	dB

*Guaranteed, not tested.

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE)

	Min	Max	Units
$\overline{WR}/\overline{RD}$ Strobe Width (t_{STW})	130		ns
$\overline{WR}/\overline{RD}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{BWND})	140		ns
Write Data Setup to $\overline{WR}$ Rising (t_{WDSU})	10		ns
$\overline{RD}$ Falling to Valid Read Data (t_{RDDV})	20	40	ns
$\overline{CS}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{CSSU})	10		ns
$\overline{CS}$ Hold from $\overline{WR}/\overline{RD}$ Rising (t_{CSHD})	0		ns
Adr Setup to $\overline{WR}/\overline{RD}$ Falling (t_{ADSU})	10		ns
Adr Hold from $\overline{WR}/\overline{RD}$ Rising (t_{ADHD})	10		ns
$\overline{DAK}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{SUDK1})	60		ns
$\overline{DAK}$ Falling to $\overline{WR}/\overline{RD}$ Rising (t_{SUDK2})	0		ns
$\overline{DAK}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{DKSU})	25		ns
Data Hold from $\overline{RD}$ Rising (t_{DHD1})	0	20	ns
Data Hold from $\overline{WR}$ Rising (t_{DHD2})	15		ns
DRQ Hold from $\overline{WR}/\overline{RD}$ Falling (t_{DRHD})	0	30	ns
$\overline{DAK}$ Hold from $\overline{WR}$ Rising (t_{DKHDa})	10		ns
$\overline{DAK}$ Hold from $\overline{RD}$ Rising (t_{DKHDb})	10		ns
$\overline{DBEN}$/DBDIR Delay from $\overline{WR}/\overline{RD}$ Falling (t_{DBDL})	0	20	ns

POWER SUPPLY

	Min	Max	Units
Power Supply Range – Analog	4.75	5.25	V
Power Supply Range – 5 V Digital	4.75	5.25	V
Power Supply Current – 5 V Operating (5 V Supplies)		120	mA
Analog Supply Current – 5 V Operating		65	mA
Digital Supply Current – 5 V Operating		55	mA
Digital Power Supply Current – Power Down		0.5	mA
Analog Power Supply Current – Power Down		0.5	mA
Power Dissipation – 5 V Operating (Current • Nominal Supplies)		600	mW
Power Dissipation – Power Down (Current • Nominal Supplies)		5	mW
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40		dB

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency		27	MHz
Recommended Clock Duty Cycle Tolerance		±10	%
Initialization Time			
16.9344 MHz Crystal Selected		70	ms
24.576 MHz Crystal Selected		90	ms

*Guaranteed, not tested

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	−0.3	6.0	V
Analog (V_{CC})	−0.3	6.0	V
Input Current			
(Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.3	(V_{CC}) + 0.3	V
Digital Input Voltage (Signal Pins)	−0.3	(V_{DD}) + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	−65	+150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

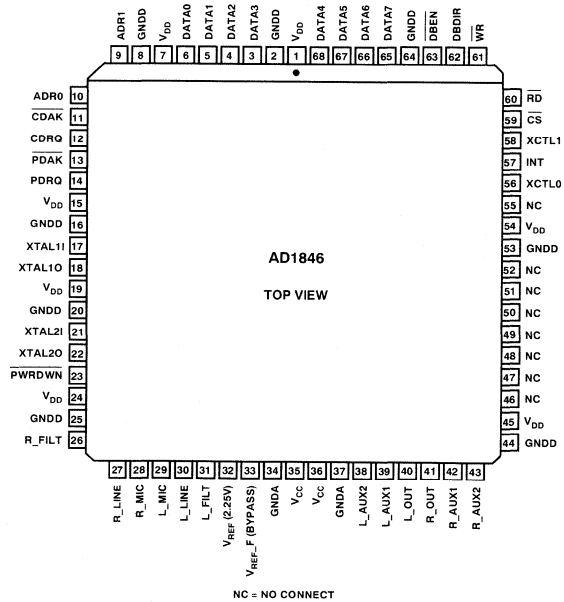
Model	Temperature Range	Package Description	Package Option*
AD1846JP	0°C to +70°C	68-Lead PLCC	P-68A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1846 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

68-Lead Plastic Leaded Chip Carrier Pinout



NC = NO CONNECT

PIN DESCRIPTION

Parallel Interface

Pin Name	PLCC	I/O	Description
CDRQ	12	O	Capture Data Request. The assertion of this signal indicates that the Codec has a captured audio sample from the ADC ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.
$\overline{\text{CDAK}}$	11	I	Capture Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.
PDRQ	14	O	Playback Data Request. The assertion of this signal indicates that the Codec is ready for more DAC playback data. The signal will remain asserted until all the bytes needed for a playback sample have been transferred.
$\overline{\text{PDAK}}$	13	I	Playback Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.
ADR1:0	9 & 10	I	Codec Addresses. These address pins are asserted by the Codec interface logic during a control register/PIO access. The state of these address lines determine which register is accessed.
$\overline{\text{RD}}$	60	I	Read Command Strobe. This active LO signal defines a read cycle from the Codec. The cycle may be a read from the control/PIO registers, or the cycles could be a read from the Codec's DMA sample registers.
$\overline{\text{WR}}$	61	I	Write Command Strobe. This active LO signal indicates a write cycle to the Codec. The cycle may be a write to the control/PIO registers, or the cycle could be a write to the Codec's DMA sample registers.
$\overline{\text{CS}}$	59	I	AD1846 Chip Select. The Codec will not respond to any control/PIO cycle accesses unless this active LO signal is LO. This signal is ignored during DMA transfers.
DATA7:0	3–6 & 65–68	I/O	Data Bus. These pins transfer data and control information between the Codec and the host.
$\overline{\text{DBEN}}$	63	O	Data Bus Enable. This pin enables the external bus drivers. This signal is normally HI. For control register/PIO cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ OR $\overline{\text{RD}}$) AND $\overline{\text{CS}}$ For DMA cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ OR $\overline{\text{RD}}$) AND ($\overline{\text{PDAK}}$ OR $\overline{\text{CDAK}}$)
DBDIR	62	O	Data Bus Direction. This pin controls the direction of the data bus transceiver. HI enables writes from the host to the AD1846; LO enables reads from the AD1846 to the host bus. This signal is normally HI. For control register/PIO cycles, DBDIR = $\overline{\text{RD}}$ AND $\overline{\text{CS}}$ For DMA cycles, DBDIR = $\overline{\text{RD}}$ AND ($\overline{\text{PDAK}}$ OR $\overline{\text{CDAK}}$)

Analog Signals

Pin Name	PLCC	I/O	Description
L_LINE	30	I	Left Line Input. Line level input for the left channel.
R_LINE	27	I	Right Line Input. Line level input for the right channel.
L_MIC	29	I	Left Microphone Input. Microphone input for the left channel. This signal can be either line level or −20 dB from line level.
R_MIC	28	I	Right Microphone Input. Microphone input for the right channel. This signal can be either line level or −20 dB from line level.
L_AUX1	39	I	Left Auxiliary #1 Line Input
R_AUX1	42	I	Right Auxiliary #1 Line Input
L_AUX2	38	I	Left Auxiliary #2 Line Input
R_AUX2	43	I	Right Auxiliary #2 Line Input
L_OUT	40	O	Left Line Level Output
R_OUT	41	O	Right Line Level Output

Miscellaneous

Pin Name	PLCC	I/O	Description
XTAL1I	17	I	24.576 MHz Crystal #1 Input
XTAL1O	18	O	24.576 MHz Crystal #1 Output
XTAL2I	21	I	16.9344 MHz Crystal #2 Input
XTAL2O	22	O	16.9344 MHz Crystal #2 Output
$\overline{\text{PWRDWN}}$	23	I	Power-Down Signal. Active LO control places AD1846 in its lowest power consumption mode. All sections of the AD1846, including the digital interface, are shut down and consume minimal power.
INT	57	O	Host Interrupt Pin. This signal is used to notify the host that the DMA Current Count Register has underflowed.
XCTL1:O	56 & 58	O	External Control. These signals reflect the current status of register bits inside the AD1846. They can be used for signaling or to control external logic. XLTL1 and XLTL0 are open-drain outputs.
V_{REF}	32	O	Voltage Reference. Nominal 2.25 volt reference available externally for dc-coupling and level-shifting. V_{REF} should not be used where it will sink or source current.
V_{REF}_F	33	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only.
L_FILT	31	I	Left Channel Filter Input. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
R_FILT	26	I	Right Channel Filter Input. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
NC	46–52, 55		No Connect. Do not connect.

Power Supplies

Pin Name	PLCC	I/O	Description
V_{CC}	35 & 36	I	Analog Supply Voltage (+5 V)
GNDA	34 & 37	I	Analog Ground
V_{DD}	1, 7, 15, 19, 24, 45, 54	I	Digital Supply Voltage (+5 V)
GNDD	2, 8, 16, 20, 25, 44, 53, 64	I	Digital Ground

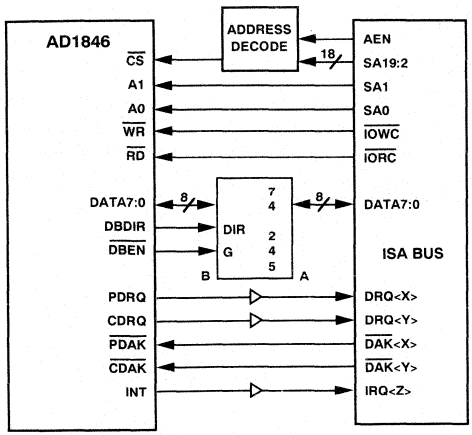


Figure 1. Interface to ISA Bus

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1846 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1846 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1846 SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. LINE, MIC, and AUX1 inputs and post-mixed DAC output analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently gained/attenuated from +12 dB to −34.5 dB in −1.5 dB steps or completely muted. The post mixed DAC output is available on OUT externally and as an input to the ADCs.

Even if the AD1846 is not playing back data from its DACs, the analog mix function can still be active.

Analog-to-Digital Datapath

The AD1846 ΣΔ ADCs incorporate a fourth order modulator. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include linear phase digital decimation filters that low-pass filter the input to $0.4 \times F_S$. ("F_S" is the word rate or "sampling frequency"). ADC input overrange conditions will cause bits to be set that can be read.

Each channel of the mic inputs can be amplified digitally by +18 dB to compensate for the voltage swing differences between line levels and typical condenser microphone levels. This +18 dB digital gain is enabled with the same control bits (LMGE and RMGE) as the +20 dB analog gain in the AD1848.

Digital-to-Analog Datapath

The ΣΔ DACs contain a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter oversamples by 64 and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to −94.5 dB in 1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample by 64 and convert the signal to a single bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output. No external components are required. Phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Changes in DAC output attenuation take effect only on zero crossings, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48 milliseconds at an 8 kHz sampling rate. (Time out [ms] $\approx 384/F_S$ [kHz].)

Digital Mixing

Stereo digital output from the ADCs can be mixed digitally with the input to the DACs. Digital output from the ADCs going out of the data port is unaffected by the digital mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1846 always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixty-four steps of −1.5 dB attenuation are supported to −94.5 dB. The digital mix datapath can also be completely muted, preventing any mixing of the analog input with the digital input. Note that the level of the mixed signal is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators.

In case the AD1846 is capturing data but ADC output data is not removed in time ("ADC overrun"), then the last sample captured before overrun will be used for the digital mix. In case the AD1846 is playing back data but input digital DAC data fails to arrive in time ("DAC underrun"), then a midscale zero will be added to the digital mix data.

Analog Outputs

A stereo line level output is available at external pins. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near V_{REF}, the midscale reference voltage.

Digital Data Types

The AD1846 supports four data types: 16-bit twos-complement linear PCM, eight-bit unsigned linear PCM, companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. Stereo data is always transferred in the left-right order. All data formats that are less than 16 bits are properly aligned to insure the utilization of full system resolution.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

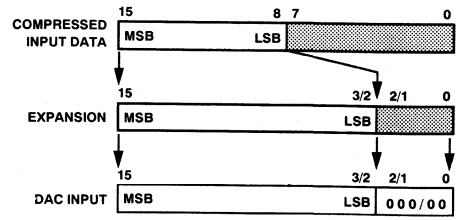


Figure 2. A-Law or μ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified.

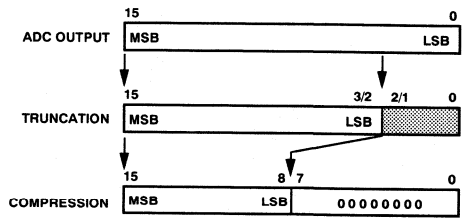


Figure 3. A-Law or μ-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1846 always uses 16-bit linear PCM representations to maintain maximum precision.

Power Supplies and Voltage Reference

The AD1846 operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (V_{REF}). The reference output can be used for biasing op amps used in dc coupling. The internal reference must be externally bypassed to analog ground at the V_{REF}–F pin.

Clocks and Sample Rates

The AD1846 operates from external crystals. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1846, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates are divided down: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz.

CONTROL REGISTERS

Control Register Architecture

The AD1846 SoundPort Stereo Codec accepts both data and control information through its byte-wide parallel port. Indirect addressing minimizes the number of external pins required to access all 21 of its byte-wide internal registers. Only two external address pins, ADR1:0, are required to accomplish all data and control transfers. These pins select one of five direct registers. (ADR1:0 = 3 addresses two registers, depending on whether the transfer is a playback or a capture.)

ADR1:0	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Registers

Figure 4. Direct Register Map

A write to or a read from the Indexed Data Register will access the indirect register which is indexed by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 16 indirect registers are indexed in Figure 5.

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Clock and Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Miscellaneous Information
13	Digital Mix
14	Upper Base Count
15	Lower Base Count

Figure 5. Indirect Register Map

A detailed map of all direct and indirect register contents is summarized for reference as follows:

Direct Registers:

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8	res	FMT	C/L	S/M	CFS2	CFS1	CFS0	CSS
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	res	res	res	res	IEN	res
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	res	res	res	res	ID3	ID2	ID1	ID0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Figure 6. Register Summary

Note that the only sticky bit in any of the AD1846 control registers is the interrupt (INT) bit. All other bits change with every sample period.

Direct Control Register Definitions

Index Register (ADR1:0 = 0)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0

IXA3:0 Index Address. These bits define the address of the AD1846 register accessed by the Indexed Data Register. These bits are read/write.

res Reserved for future expansion. Always write a zero to this bit.

TRD Transfer Request Disable. This bit, when set, causes all data transfers to cease when the Interrupt Status (INT) bit of the Status Register is set.

0 Transfers Enabled During Interrupt. PDRQ and CDRQ pin outputs are generated uninhibited by interrupts. DMA Current Counter Register decrements with every sample period when either PEN or CEN are enabled.

1 Transfers Disabled By Interrupt. PDRQ and CDRQ pin outputs are generated only if INT bit is 0 (when either PEN or CEN, respectively, are enabled). Any pending playback or capture requests are allowed to complete at the time when TRD is set. After pending requests complete, midscale inputs will be internally generated for the DACs, and the ADC output buffer will contain the last valid output. Clearing the sticky INT bit (or the TRD bit) will cause the resumption of playback and/or capture requests (presuming PEN and/or CEN are enabled). The DMA Current Counter Register will not decrement while both the TRD bit is set and the INT bit is a one.

MCE Mode Change Enable. This bit must be set whenever the current functional mode of the AD1846 is changed. Specifically, the Clock and Data Format and Interface Configuration registers cannot be changed unless this bit is set. The exceptions are CEN and PEN in the Interface Configuration which can be changed "on-the-fly." MCE should be cleared at the completion of the desired register changes. The DAC outputs are automatically muted when the MCE bit is set. After MCE is cleared, the DAC outputs will be restored to the state specified by the LDM and RDM mute bits.

Both ADCs and DACs are automatically muted for approximately 128 sample cycles after exiting the MCE state to allow the reference and all filters to settle. The ADCs will produce midscale values; the DACs' analog output will be muted. All converters are internally operating during these ≈128 sample cycles, and the AD1846 will expect playback data and will generate (midscale) capture data. Note that the autocalibrate-in-process (ACI) bit will be set on exit from the MCE state regardless of whether or not ACAL was set. ACI will remain HI for these ≈128 sample cycles; system software should poll this bit rather than count cycles.

Special sequences must be followed if autocalibrate (ACAL) is set or sample rates are changed (CFS2:0 and or CSS) during mode change enable. See the "Autocalibration" and "Changing Sample Rates" sections below.

INIT AD1846 Initialization. This bit is set when the AD1846 is in a state which cannot respond to parallel bus cycles. This bit is read only.

Immediately after reset and once the AD1846 has left the INIT state, the initial value of this register will be "0100 0000 (40h)." During AD1846 initialization, this register cannot be written to and will always read "100x 0000 (80h)."

Indexed Data Register (ADR1:0 = 1)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0

IXD7:0 Indexed Register Data. These bits contain the contents of the AD1846 register referenced by the Indexed Data Register.

During AD1846 initialization, this register cannot be written to and will always read as "1000 0000 (80h)."

Status Register (ADR1:0 = 2)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT

INT Interrupt Status. This sticky bit (the only one) indicates the status of the interrupt logic of the AD1846. This bit is cleared by any host write of any value to this register. The IEN bit of the Pin Control Register determines whether the state of this bit is reflected on the INT pin of the AD1846. The only interrupt condition supported by the AD1846 is generated by the underflow of the DMA Current Count Register.

0 Interrupt pin inactive

1 Interrupt pin active

PRDY Playback Data Register Ready. The PIO Playback Data Register is ready for more data. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 DAC data is still valid. Do not overwrite.

1 DAC data is stale. Ready for next host data write value.

PL/R Playback Left/Right Sample. This bit indicates whether the PIO playback data needed is for the right channel DAC or left channel DAC. This bit is read only.

0 Right channel needed

1 Left channel or mono

PU/L Playback Upper/Lower Byte. This bit indicates whether the PIO playback data needed is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte needed

1 Upper byte needed or any 8-bit mode

SOUR Sample Over/Underrun. This bit indicates that the most recent sample was not serviced in time and therefore either a capture overrun (COR) or playback underrun (PUR) has occurred. The bit indicates an overrun for ADC capture and an underrun for DAC playback. If both capture and playback are enabled, the source which set this bit can be determined by reading COR and PUR. This bit changes on a sample-by-sample basis. This bit is read only.

CRDY Capture Data Ready. The PIO Capture Data Register contains data ready for reading by the host. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 ADC data is stale. Do not reread the information.

1 ADC data is fresh. Ready for next host data read.

CL/R Capture Left/Right Sample. This bit indicates whether the PIO capture data waiting is for the right channel ADC or left channel ADC. This bit is read only.

0 Right channel

1 Left channel or mono

CU/L Capture Upper/Lower Byte. This bit indicates whether the PIO capture data ready is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte ready

1 Upper byte ready or any 8-bit mode

The PRDY, CRDY, and INT bits of this status register can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value just as these bits are changing, for example. A "1" value would not be read until the next host access.

This registers's initial state after reset is "1100 1100."

PIO Data Registers (ADR1:0 = 3)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The PIO Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During AD1846 initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000 (80h)."

CD7:0 PIO Capture Data Register. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

PD7:0 PIO Playback Data Register. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Indirect Control Register Definitions

The following control registers are accessed by writing index values to IXA3:0 in the Index Address Register (ADR1:0 = 0) followed by a read/write to the Indexed Data Register (ADR1:0 = 1).

Left Input Control (IXA3:0 = 0)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3:0 Left input gain select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LMGE Left Input Microphone Gain Enable. Setting this bit will enable the +18 dB digital gain of the left mic input signal.

LSS1:0 Left Input Source Select. These bits select the input source for the left gain stage preceding the left ADC.

0 Left Line Source Selected
1 Left Auxiliary 1 Source Selected
2 Left Microphone Source Selected
3 Left Line Post-Mixed DAC Output Source Selected

This register's initial state after reset is "000x 0000."

Right Input Control (IXA3:0 = 1)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3:0 Right Input Gain Select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RMGE Right Input Microphone Gain Enable. Setting this bit will enable the +18 dB digital gain of the right mic input signal.

RSS1:0 Right Input Source Select. These bits select the input source for the right channel gain stage preceding the right ADC.

0 Right Line Source Selected
1 Right Auxiliary 1 Source Selected
2 Right Microphone Source Selected
3 Right Post-Mixed DAC Output Source Selected

This register's initial state after reset is "000x 0000."

Left Auxiliary #1 Input Control (IXA3:0 = 2)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0

LX1A4:0 Left Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. LX1A4:0 = 0 produces a +12 dB gain. LX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX1 Left Auxiliary #1 Mute. This bit, when set, will mute the left channel of the Auxiliary #1 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Right Auxiliary #1 Input Control (IXA3:0 = 3)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0

RX1A4:0 Right Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. RX1A4:0 = 0 produces a +12 dB gain. RX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX1 Right Auxiliary #1 Mute. This bit, when set, will mute the right channel of the Auxiliary #1 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Left Auxiliary #2 Input Control (IXA3:0 = 4)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0

LX2A4:0 Left Auxiliary Input #2 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. LX2A4:0 = 0 produces a +12 dB gain. LX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX2 Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Right Auxiliary #2 Input Control (IXA3:0 = 5)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0

RX2A4:0 Right Auxiliary Input #2 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. RX2A4:0 = 0 produces a +12 dB gain. RX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX2 Right Auxiliary #2 Mute. This bit, when set, will mute the right channel of the Auxiliary #2 input source. This bit is set to "1" after reset.

This register's initial state after reset is "1xx0 0000."

Left DAC Control (IXA3:0 = 6)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5:0 Left DAC Attenuate Select. The least significant bit of this attenuate select represents −1.5 dB. LDA5:0 = 0 produces a 0 dB attenuation. Maximum attenuation is −94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LDM Left DAC Mute. This bit, when set to 1, will mute the left DAC output. Auxiliary inputs are muted independently with the Left Auxiliary Input Control Registers. This bit is set to "1" after reset.

This register's initial state after reset is "1x00 0000."

Right DAC Control (IXA3:0 = 7)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5:0 Right DAC Attenuate Select. The least significant bit of this attenuate select represents −1.5 dB. RDA5:0 = 0 produces 0 dB attenuation. Maximum attenuation is −94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RDM Right DAC Mute. This bit, when set to 1, will mute the right DAC output. Auxiliary inputs are muted independently with the Right Auxiliary Input Control Registers. This bit is set to "1" after reset.

This register's initial state after reset is "1x00 0000."

Clock and Data Format Register (IXA3:0 = 8)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
8	res	FMT	C/L	S/M	CFS2	CFS1	CFS0	CSS

The contents of the Clock and Data Format Register cannot be changed except when the AD1846 is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1846 is not in the MCE state will not be successful.

CSS Clock Source Select. These bits select the crystal clock source which will be used for the audio sample rates.

0 XTAL1 (24.576 MHz)

1 XTAL2 (16.9344 MHz)

CFS2:0 Clock Frequency Divide Select. These bits select the audio sample rate frequency. The actual audio sample rate depends on which crystal clock source is selected and the frequency of that source.

CFS	Divide Factor	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0	3072	8.0 kHz	5.5125 kHz
1	1536	16.0 kHz	11.025 kHz
2	896	27.42857 kHz	18.9 kHz
3	768	32.0 kHz	22.05 kHz
4	448	Not Supported	37.8 kHz
5	384	Not Supported	44.1 kHz
6	512	48.0 kHz	33.075 kHz
7	2560	9.6 kHz	6.615 kHz

Note that the AD1846's internal oscillators can be driven by external clock sources at the crystal input pins. If an external clock source is applied, it will be divided down by the selected Divide Factor. It need not be at the recommended crystal frequencies.

S/M Stereo/Mono Select. This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 Mono

1 Stereo

C/L Companded/Linear Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all input and output data. The type of linear PCM or the type of companded format is defined by the FMT bits.

0 Linear PCM

1 Companded

FMT Format Select. This bit defines the format for all digital audio input and outputs based on the state of the C/L bit.

	Linear PCM (C/L = 0)	Companded (C/L = 1)
0	8-bit Unsigned PCM	8-bit μ-law Companded
1	16-bit Twos-Complement PCM	8-bit A-law Companded

res Reserved for future expansion. Always write a zero to this bit.

This register's initial state after reset is "x000 0000."

Interface Configuration Register (IXA3:0 = 9)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

The contents of the Interface Configuration Register cannot be changed except when the AD1846 is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1846 is not in the MCE state will not be successful. PEN and CEN are exceptions; these bits may always be written.

PEN Playback Enable. This bit will enable the playback of data in the format selected. The AD1846 will generate PDRQ and respond to $\overline{\text{PDAK}}$ signals when this bit is enabled and PPIO = 0. If PPIO = 1, this bit enables Programmed I/O (PIO) playback mode. PEN may be set and reset without setting the MCE bit.

0 Playback disabled (PDRQ and PIO Playback Data Register inactive)

1 Playback enabled

CEN Capture Enable. This bit will enable the capture of data in the format selected. The AD1846 will generate CDRQ and respond to $\overline{\text{CDAK}}$ signals when this bit is enabled and CPIO = 0. If CPIO = 1, this bit enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 Capture disabled (CDRQ and PIO Capture Data Register inactive)

1 Capture enabled

SDC Single DMA Channel. This bit will force both capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be LO. This bit will allow the AD1846 to be used with only one DMA channel. Simultaneous capture and playback cannot occur in this mode. Should both capture and playback be enabled (CEN = PEN = 1) in the mode, only playback will occur. See "Data and Control Transfers" for further explanation.

0 Dual DMA channel mode

1 Single DMA channel mode

ACAL Autocalibrate Enable. This bit determines whether the AD1846 performs an autocalibrate whenever the $\overline{\text{PWRDWN}}$ pin is deasserted or from the Mode Change Enable (MCE) bit being reset. ACAL is normally set. See "Autocalibration" below for a description of a complete autocalibration sequence.

0 No autocalibration

1 Autocalibration after power down/reset or mode change

res Reserved for future expansion. Always write zeros to these bits.

PPIO Playback PIO Enable. This bit determines whether the playback data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

CPIO Capture PIO Enable. This bit determines whether the capture data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

This register's initial state after reset is "00xx 1000."

Pin Control Register (IXA3:0 = 10)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
10	XCTL1	XCTL0	res	res	res	res	IEN	res

res Reserved for future expansion. Always write zeros to these bits.

IEN Interrupt Enable. This bit enables the interrupt pin. The Interrupt Pin will go active HI when the number of samples programmed in the Base Count Register is reached.

0 Interrupt disabled

1 Interrupt enabled

XCTL1:0 External Control. The state of these independent bits is reflected on the respective XCTL1:0 pins of the AD1846.

0 TTL Logic LO on XCTL1:0 pins

1 TTL Logic HI on XCTL1:0 pins

This register's initial state after reset is "00xx xx0x."

Test and Initialization Register (IXA3:0 = 11)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1:0 Overrange Left Detect. These bits indicate the overrange on the left input channel. This bit changes on a sample-by-sample basis. This bit is read only.

0 Less than −1 dB underrange

1 Between −1 dB and 0 dB underrange

2 Between 0 dB and +1 dB overrange

3 Greater than +1 dB overrange

ORR1:0 Overrange Right Detect. These bits indicate the overrange on the right input channel. This bit changes on a sample-by-sample basis. This bit is read only.

0 Less than −1 dB underrange

1 Between −1 dB and 0 dB underrange

2 Between 0 dB and +1 dB overrange

3 Greater than +1 dB overrange

DRS Data Request Status. This bit indicates the current status of the PDRQ and CDRQ pins of the AD1846.

0 CDRQ and PDRQ are presently inactive (LO)

1 CDRQ or PDRQ are presently active (HI)

ACI Autocalibrate-In-Progress. This bit indicates the state of autocalibration or a recent exit from Mode Change Enable (MCE). This bit is read only.

0 Autocalibration is not in progress

1 Autocalibration is in progress or MCE was exited within approximately the last 128 sample periods

PUR Playback Underrun. This bit is set when playback data has not arrived from the host in time to be played. As a result, a midscale value will be sent to the DACs. This bit changes on a sample by sample basis.

COR Capture Overrun. This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit changes on a sample by sample basis.

The occurrence of a PUR and/or COR is designated in the Status Register's Sample Overrun/Underrun (SOUR) bit. The SOUR bit is the logical OR of the COR and PUR bits. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.

This register's initial state after reset is "0000 0000."

Miscellaneous Control Register (IXA3:0 = 12)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
12	res	res	res	res	ID3	ID2	ID1	ID0

res Reserved for future expansion. The bits are read only. Do not write to these bits.

ID3:0 AD1846 Revision ID. These four bits define the revision level of the AD1846. The AD1846 is designated ID = "1010." Revisions increment by one LSB. These bits are read only.

This register's initial state after reset is "xxxx RRRR" where RRRR = Revision ID of the silicon in use.

Digital Mix Control Register (IXA3:0 = 13)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME

DME Digital Mix Enable. This bit will enable the digital mix of the ADCs' output with the DACs' input. When enabled, the data from the ADCs are digitally mixed with other data being delivered to the DACs (regardless of whether or not playback [PEN] is enabled, i.e., set). If capture is enabled (CEN set) and there is a capture overrun (COR), then the last sample captured before overrun will be used for the digital mix. If playback is enabled (PEN set) and there is a playback underrun (PUR), then a midscale zero will be added to the digital mix data.

0 Digital mix disabled (muted)

1 Digital mix enabled

res Reserved for future expansion. Always write a zero to this bit.

DMA5:0 Digital Mix Attenuation. These bits determine the attenuation of the ADC data in mixing with the DAC input. Each attenuate step is −1.5 dB ranging to −94.5 dB.

This register's initial state after reset is "0000 00x0."

DMA Base Count Registers (IXA3:0 = 14 & 15)

The DMA Base Count Registers in the AD1846 simplify integration of the AD1846 in ISA systems. The ISA DMA controller requires an external count mechanism to notify the host CPU via interrupt of a full DMA buffer. The programmable DMA Base Count Registers will allow such interrupts to occur.

The Base Count Registers contain the number of sample periods which will occur before an interrupt is generated on the interrupt (INT) pin. To load, first write a value to the Lower Base Count Register. Writing a value to the Upper Base Register will cause both Base Count Registers to load into the Current Count Register. Once AD1846 transfers are enabled, each sample period the Current Count Register will decrement until zero count is reached. The next sample period after zero will generate the interrupt and reload the Current Count Register with the values in the Base Count Registers. The interrupt is cleared by a write to the Status Register.

The Host Interrupt Pin (INT) will go HI during the sample period in which the Current Count Register underflows when Interrupt Enable (IEN) is set. The Host Interrupt Pin (INT) will go LO when the Interrupt Status Bit (INT) is cleared. [Note that both the Host Interrupt Pin and the Interrupt Status Bit have the same name (INT)].

The Current Count Register is decremented every sample period when either the PEN or CEN bit is enabled and also either the Transfer Request Disable (TRD) bit or the Interrupt Status (INT) bit are zero. Note that the internal INT bit will become one on counter underflow even if the external interrupt pin is not enabled, i.e., IEN is zero. The Current Count Register is decremented in both PIO and DMA data transfer modes.

Upper Base Count Register (IXA3:0 = 14)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7:0 Upper Base Count. This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters can not be read.

This register's initial state after reset is "0000 0000."

Lower Upper Base Count Register (IXA3:0 = 15)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7:0 Lower Base Count. This byte is the lower byte of the base count register containing the eight least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters cannot be read.

This register's initial state after reset is "0000 0000."

Serial-Port 16-Bit SoundPort Stereo Codec

AD1847

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Supports the Microsoft Windows Sound System*
Multiple Channels of Stereo Input
Analog and Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
44-Lead PLCC and TQFP Packages
Operation from +5 V Supplies
Serial Digital Interface Compatible with ADSP-21xx Fixed-Point DSP

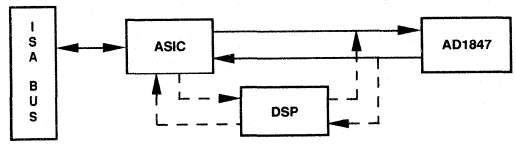


Figure 1. Example System Diagram

3

PRODUCT OVERVIEW

The AD1847 SoundPort® Stereo Codec integrates key audio data conversion and control functions into a single integrated circuit. The AD1847 is intended to provide a complete, low cost, single-chip solution for business, game audio and multimedia applications requiring operation from a single +5 V supply. It provides a serial interface for implementation on a computer motherboard, add-in or PCMCIA card. See Figure 1 for an example system diagram.

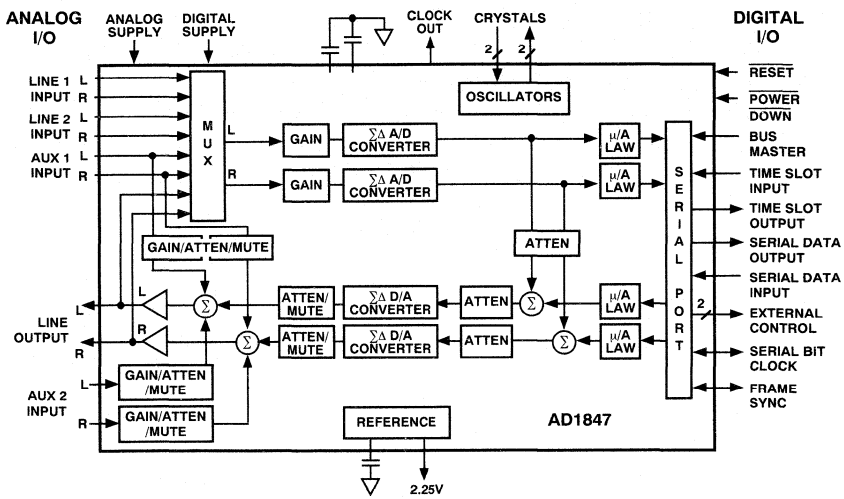
External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 70 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters (ADCs) and a stereo pair of ΣΔ digital-to-analog converters (DACs). Inputs to the ADC can be selected from four stereo pairs of analog signals: line 1, line 2, auxiliary ("aux") line #1, and post-mixed DAC output. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The pair of 16-bit outputs from the ADCs is available over a serial interface that also supports 16-bit digital input to the DACs and control/status information. The AD1847 can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

*Windows Sound System is a registered trademark of Microsoft Corporation.
SoundPort is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1847–SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Word Rate (F_S)	48	kHz
Input Signal	1007	Hz
Analog Output Passband	20	Hz to 20 kHz
FFT Size	4096	
V_{IH}	2.4	V
V_{IL}	0.8	V
V_{OH}	2.4	V
V_{OL}	0.4	V

DAC Input Conditions
0 dB Attenuation
Full-Scale Digital Inputs
16-Bit Linear Mode
No Output Load
Mute Off

ADC Input Conditions
0 dB Gain
−3.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode

ANALOG INPUT

	Min	Typ	Max	Units
Full-Scale Input Voltage (RMS Values Assume Sine Wave Input)				
Line1, Line2, AUX1, AUX2		1		V rms
	2.54	2.8	3.10	V p-p
Input Impedance				
Line1, Line2, AUX1, AUX2†	10			kΩ
Input Capacitance†		15		pF

PROGRAMMABLE GAIN AMPLIFIER–ADC

	Min	Typ	Max	Units
Step Size (All Steps Tested, −30 dB Input)	1.10	1.5	1.90	dB
PGA Gain Range Span†	21.0		24.0	dB

AUXILIARY INPUT ANALOG AMPLIFIERS/ATTENUATORS

	Min	Typ	Max	Units
Step Size (+12 dB to −28.5 dB, Referenced to DAC Full Scale)	1.3	1.5	1.7	dB
Step Size (−30 dB to −34.5 dB, Referenced to DAC Full Scale)	1.1	1.5	1.9	dB
Input Gain/Attenuation Range Span†	45.5		47.5	dB
AUX Input Impedance†	10			kΩ

DIGITAL DECIMATION AND INTERPOLATION FILTERS†

	Min	Max	Units
Passband	0	$0.4 \times F_S$	Hz
Passband Ripple	−0.1	+0.1	dB
Transition Band	$0.4 \times F_S$	$0.6 \times F_S$	Hz
Stopband	$0.6 \times F_S$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$30/F_S$	
Group Delay Variation Over Passband		0	μs

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale, A Weighted)	70			dB
THD+N (Referenced to Full Scale)			0.040	%
			−68	dB
Signal-to-Intermodulation Distortion†		83		dB
ADC Crosstalk†				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)			−80	dB
Line1 to Line2 (Input Line1, Ground and Select Line2, Read Both Channels)			−80	dB
Line to AUX1			−80	dB
Line to AUX2			−80	dB
Line to DAC			−80	dB
Gain Error (Full-Scale Span Relative to V_{REFI})			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.2	dB
DC Offset			±55	LSB

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale, A Weighted)	76			dB
THD+N (Referenced to Full Scale)			0.025	%
			−72	dB
Signal-to-Intermodulation Distortion†		86		dB
Gain Error (Full-Scale Span Relative to V_{REFI})			±10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.2	dB
DAC Crosstalk† (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			−80	dB
Total Out-of-Band Energy (Measured from 0.6 × F_S to 100 kHz)†			−50	dB
Audible Out-of-Band Energy (Measured from 0.6 × F_S to 22 kHz, Tested at F_S = 5.5 kHz)			−55	dB

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to −22.5 dB) (Tested at Steps 0, −19.5)	1.3	1.5	1.7	dB
Step Size (−24.0 dB to −94 dB)	1.0	1.5	2.0	dB
Output Attenuation Range Span†	−93		95	dB

DIGITAL MIX ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to −22.5 dB) (Tested at Steps 0, −19.5)	1.3	1.5	1.7	dB
Step Size (−24.0 dB to −94 dB)	1.0	1.5	2.0	dB
Output Attenuation Range Span†	−93.5		95.5	dB

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Line Output Voltage		0.707		V rms
V_{REFI} = 2.35*	1.80	2	2.20	V p-p
Line Output Impedance†			600	Ω
External Load Impedance	10			kΩ
Output Capacitance†			15	pF
External Load Capacitance			100	pF
V_{REF} (Clock Running)	2.00		2.50	V
V_{REF} Current Drive		100		µA
V_{REFI}		2.35		V
Mute Attenuation of 0 dB Fundamental† (LOUT)			−80	dB
Mute Click† (|Muted Output Minus Unmuted Midscale DAC Output|)			8	mV

*Full-scale line output voltage scales with V_{REF} (e.g., V_{OUT} (typ) − 2.0V × (V_{REF}/2.35)).
†Guaranteed, not tested.

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
System Frequency Response† (Line In to Line Out, 20 Hz to 20 kHz)		±0.3		dB
Differential Nonlinearity†			±1/2	Bit
Phase Linearity Deviation†		1		Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.0		V
XTAL1/2I	2.4		V
Low Level Input Voltage (V_{IL})		0.8	V
High Level Output Voltage (V_{OH}) I_{OH} = 1 mA	2.4	V_{DD}	V
Low Level Output Voltage (V_{OL}) I_{OL} = 4 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	−10	+10	µA
Output Leakage Current (GO/NOGO Tested)	−10	+10	µA

TIMING PARAMETERS (Guaranteed Over Operating Temperature Range)

	Min	Typ	Max	Units
Serial Frame Sync Period (t_1)		1/0.5 F_S		µs
Clock to Frame Sync [SDFS] Propagation Delay (t_{PD1})			20	ns
Data Input Setup Time (t_S)	15			ns
Data Input Hold Time (t_H)	15			ns
Clock to Output Data Valid (t_{DV})	25			ns
Clock to Output Three-State [High-Z] (t_{HZ})			20	ns
Clock to Time Slot Output [TSO] Propagation Delay (t_{PD2})			20	ns
$\overline{\text{RESET}}$ and $\overline{\text{PWRDOWN}}$ LO Pulse Width (t_{RPWL})	100			ns

POWER SUPPLY

	Min	Max	Units
Power Supply Range – Digital & Analog	4.75	5.25	V
Power Supply Current – Operating (10 kΩ Line Out Load)		140	mA
Analog Supply Current – Operating (10 kΩ Line Out Load)		70	mA
Digital Supply Current – Operating (10 kΩ Line Out Load)		70	mA
Analog Power Supply Current – Power Down		400	µA
Digital Power Supply Current – Power Down		400	µA
Power Dissipation – Operating (Current × Nominal Supply)		750	mW
Power Dissipation – Power Down (Current × Nominal Supply)		4	mW
Power Supply Rejection (@ 1 kHz)†			
(At Both Analog and Digital Supply Pins, ADCs)	45		dB
(At Both Analog and Digital Supply Pins, DACs)	55		dB

CLOCK SPECIFICATIONS†

	Min	Max	Units
Input Clock Frequency		25	MHz
Recommended Clock Duty Cycle		±10	%
Initialization/Sample Rate Change Time			
16.9344 MHz Crystal Selected at Power-Up		171	ms
24.576 MHz Crystal Selected at Power-Up		171	ms
16.9344 MHz Crystal Selected Subsequently		6	ms
24.576 MHz Crystal Selected Subsequently		6	ms

†Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	−0.3	6.0	V
Analog (V_{CC})	−0.3	6.0	V
Input Current			
(Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.3	(VA+) +0.3	V
Digital Input Voltage (Signal Pins)	−0.3	(VD+) +0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	−65	+150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1847JP	0°C to +70°C	44-Lead PLCC	P-44A
AD1847JST	0°C to +70°C	44-Lead TQFP	ST-44

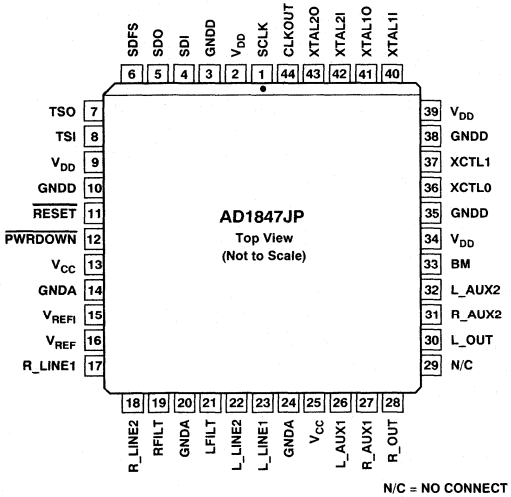
*For outline information see Package Information section.

CAUTION

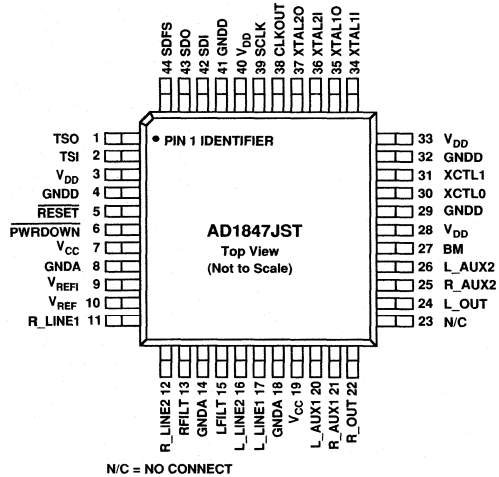
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1847 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

3

44-Lead PLCC



44-Lead TQFP



PIN DESCRIPTION

Serial Interface

Pin Name	PLCC	TQFP	I/O	Description
SCLK	1	39	I/O	Serial Clock. SCLK is a bidirectional signal that supplies the clock as an output to the serial bus when the Bus Master (BM) pin is driven HI and accepts the clock as an input when the BM pin is driven LO. The serial clock output is fixed at 12.288 MHz when XTAL1 is selected, and 11.2896 MHz when XTAL2 is selected. SCLK runs continuously. An AD1847 should always be configured as the serial bus master unless it is a slave in a daisy-chained multiple codec system.
SDFS	6	44	I/O	Serial Data Frame Sync. SDFS is a bidirectional signal that supplies the frame synchronization signal as an output to the serial bus when the Bus Master (BM) pin is driven HI and accepts the frame synchronization signal as an input when the BM pin is driven LO. The SDFS frequency powers up at one half of the AD1847 sample rate (i.e., FRS bit = 0) with two samples per frame and can be programmed to match the sample rate (i.e., FRS bit = 1) with one sample per frame. An AD1847 should always be configured as the serial bus master unless it is a slave in a daisy-chained multiple codec system.
SDI	4	42	I	Serial Data Input. SDI is used by peripheral devices such as the host CPU or a DSP to supply control and playback data information to the AD1847. All control and playback transfers are 16 bits long, MSB first.
SDO	5	43	O	Serial Data Output. SDO is used to supply status/index readback and capture data information to peripheral devices such as the host CPU or a DSP. All status/index readback and capture data transfers are 16 bits long, MSB first. Three-state output driver.
$\overline{\text{RESET}}$	11	5	I	Reset. The $\overline{\text{RESET}}$ signal is active LO. The assertion of this signal will initialize the on-chip registers to their default values. See the "Control Register Definitions" section for a description of the contents of the control registers after $\overline{\text{RESET}}$ is deasserted.
$\overline{\text{PWRDOWN}}$	12	6	I	Powerdown. The $\overline{\text{PWRDOWN}}$ signal is active LO. The assertion of this signal will reset the on-chip control registers (identically to the $\overline{\text{RESET}}$ signal) and will also place the AD1847 in a low power consumption mode. V_{REF} and all analog circuitry are disabled.
BM	33	27	I	Bus Master. The assertion (HI) of this signal indicates that the AD1847 is the serial bus master. The AD1847 will then supply the serial clock (SCLK) and the frame sync (SDFS) signals for the serial bus. One and only one AD1847 should always be configured as the serial bus master. If BM is connected to logic LO, the AD1847 is configured as a bus slave, and will accept the SCLK and SDFS signals as inputs. An AD1847 should only be configured as a serial bus slave when an AD1847 serial bus master already exists, in daisy-chained multiple codec systems.
TSO	7	1	O	Time Slot Output. This signal is asserted HI by the AD1847 coincidentally with the LSB of the last time slot used by the AD1847. Used in daisy-chained multiple codec systems.
TSI	8	2	I	Time Slot Input. The assertion of this signal indicates that the AD1847 should immediately use the next three time slots (TSSEL = 1) or the next six time slots (TSSEL = 0) and then activate the TSO pin to enable the next device down the TDM chain. TSI should be driven LO when the AD1847 is the bus master or in single codec systems. Used in daisy-chained multiple codec systems.
CLKOUT	44	38	O	Clock Output. This signal is the buffered version of the crystal clock output and the frequency is dependent on which crystal is selected. This pin can be three-stated by driving the BM pin LO or by programming the CLKTS bit in the Pin Control Register. See the "Control Registers" section for more details. The CLKOUT frequency is 12.288 MHz when XTAL1 is selected and 16.9344 MHz when XTAL2 is selected.

Analog Signals

Pin Name	PLCC	TQFP	I/O	Description
L_LINE1	23	17	I	Left Line Input #1. Line level input for the #1 left channel.
R_LINE1	17	11	I	Right Line Input #1. Line level input for the #1 right channel.
L_LINE2	22	16	I	Left Line Input #2. Line level input for the #2 left channel.
R_LINE2	18	12	I	Right Line Input #2. Line level input for the #2 right channel.
L_AUX1	26	20	I	Left Auxiliary Input #1. Line level input for the AUX1 left channel.
R_AUX1	27	21	I	Right Auxiliary Input #1. Line level input for the AUX1 right channel.
L_AUX2	32	26	I	Left Auxiliary Input #2. Line level input for the AUX2 left channel.
R_AUX2	31	25	I	Right Auxiliary Input #2. Line level input for the AUX2 right channel.
L_OUT	30	24	O	Left Line Output. Line level output for the left channel.
R_OUT	28	22	O	Right Line Output. Line level output for the right channel.

Miscellaneous

Pin Name	PLCC	TQFP	I/O	Description
XTAL1I	40	34	I	24.576 MHz Crystal #1 Input.
XTAL1O	41	35	O	24.576 MHz Crystal #1 Output.
XTAL2I	42	36	I	16.9344 MHz Crystal #2 Input.
XTAL2O	43	37	O	16.9344 MHz Crystal #2 Output.
XCTL1:O	37 & 36	31 & 30	O	External Control. These TTL signals reflect the current status of register bits inside the AD1847. They can be used for signaling or to control external logic.
V_{REF}	16	10	O	Voltage Reference. Nominal 2.25 volt reference available externally as a voltage datum for dc-coupling and level-shifting. V_{REF} should not have any signal dependent load.
V_{REFI}	15	9	I	Voltage Reference Internal. Voltage reference filter point for external bypassing only.
LFILT	21	15	I	Left Channel Filter Capacitor. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
RFILT	19	13	I	Right Channel Filter Capacitor. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
N/C	29	23		No Connect. Do not connect.

Power Supplies

Pin Name	PLCC	TQFP	I/O	Description
V_{CC}	13 & 25	7 & 19	I	Analog Supply Voltage (+5 V).
GNDA	14, 20, 24	8, 14, 18	I	Analog Ground.
V_{DD}	2, 9, 34, 39	40, 3, 28, 33	I	Digital Supply Voltage (+5 V).
GNDD	3, 10, 35, 38	41, 4, 29, 32	I	Digital Ground.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

The AD1847 serial data interface uses a Time Division Multiplex (TDM) scheme that is compatible with DSP serial ports configured in Multi-Channel Mode with 32 16-bit time slots (i.e., SPORT0 on the ADSP-2101, ADSP-2115, etc.).

AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1847 and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1847 SoundPort Stereo Codec accepts stereo line-level inputs. All inputs should be capacitively coupled (ac-coupled) to the AD1847. LINE1, LINE2, AUX1, and post-mixed DAC output analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently gained/attenuated from +12 dB to −34.5 dB in −1.5 dB steps or completely muted. The post-mixed DAC output is available on L_OUT and R_OUT externally and as an input to the ADCs.

Even if the AD1847 is not playing back data from its DACs, the analog mix function can still be active.

Analog-to-Digital Datapath

The ΣΔ ADCs incorporate a proprietary fourth-order modulator. A single pole of passive filtering is all that is required for antialiasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include digital decimation filters that low-pass filter the input to $0.40 \times F_S$. ("F_S" is the word rate or "sampling frequency.") ADC input overrange conditions will cause status bits to be set that can be read.

Digital-to-Analog Datapath

The ΣΔ DACs contain a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter oversamples and digitally filters the higher frequency images. The attenuator allows independent control of each DAC channel from 0 dB to −94.5 dB in 1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. These filters remove the very high frequency components of the DAC bitstream output. No external components are required.

Changes in DAC output attenuation take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise on playback. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48

milliseconds at an 8 kHz sampling rate. (Time-out [ms] ≈ 384 ÷ F_S [kHz]).

Digital Mixing

Stereo digital output from the ADCs can be mixed digitally with the input to the DACs. Digital output from the ADCs going out of the serial data port is unaffected by the digital mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1847 always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixty-four steps of −1.5 dB attenuation are supported to −94.5 dB. The digital mix datapath can also be completely muted, preventing any mixing of the digital input with the digital output. Note that the level of the mixed signal is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators.

Analog Outputs

A stereo line-level output is available at external pins. Other output types such as headphone and speaker must be implemented in external circuitry. The stereo line-level outputs should be capacitively coupled (ac-coupled) to the external circuitry. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near V_{REF}, the midscale reference voltage.

Digital Data Types

The AD1847 supports four global data types: 16-bit twos-complement linear PCM, 8-bit unsigned linear PCM, companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. Eight-bit data is always left-justified in 16-bit fields; in other words, the MSBs of all data types are always aligned; in yet other words, full-scale representations in all four formats correspond to equivalent full-scale signals. The eight least-significant bit positions of 8-bit data in 16-bit fields are ignored on digital input and zeroed on digital output (i.e., truncated).

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large-amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

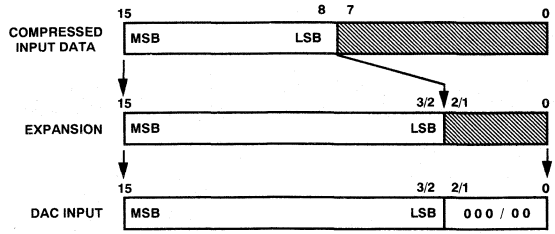


Figure 2. A-Law or μ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified.

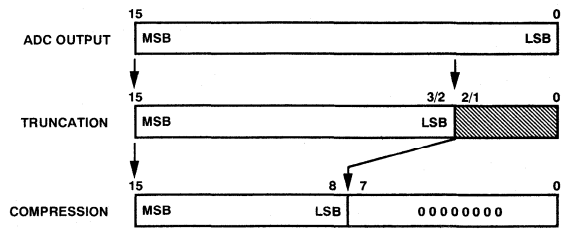


Figure 3. A-Law or μ-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1847 always uses 16-bit linear PCM representations to maintain maximum precision.

Power Supplies and Voltage Reference

The AD1847 operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single-supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (V_{REF}). The reference output can be used for biasing op amps used in dc coupling. The internal reference is externally bypassed to analog ground at the V_{REFI} pin, and must not be used to bias external circuitry.

Clocks and Sample Rates

The AD1847 operates from two external crystals, XTAL1 and XTAL2. The two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1847, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. At a minimum, XTAL1 must be provided since it is selected as the reset default. If XTAL2 is not used, the XTAL2 input pin should be connected to ground. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them, the following sample rates can be selected: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz.

CONTROL REGISTERS

Control Register Mapping

The AD1847 has six 16-bit and thirteen 8-bit on-chip user-accessible control registers. Control information is sent to the AD1847 in the 16-bit Control Word. Status information is sent from the AD1847 in the 16-bit Status Word. Playback Data and Capture Data each have two 16-bit registers for the right and left channels. Additional 8-bit Index Registers are accessed via indirect addressing in the AD1847 Control Word. [Index Registers are reached with indirect addressing.] The contents of an indirect addressed Index Register may be readback by the host CPU or DSP (during the Status Word/Index Readback time slot) by setting the Read Request (RREQ) bit in the Control Word. Note that each 16-bit register is assigned its own time slot, so that the AD1847 always consumes six 16-bit time slots. Figure 4 shows the mapping of the Control Word, Status Word/Index Readback and Data registers to time slots when TSSEL = 0. TSSEL = 0 is used when the SDI and SDO pins are tied together (i.e., "1-wire" system). This configuration is efficient in terms of component interconnect (one bidirectional wire for serial data input and output), but inefficient in terms of time slot usage (six slots consumed on single bidirectional Time Division Multiplexed [TDM] serial bus). When TSSEL = 0, serial data input to the AD1847 occurs sequentially with serial data output from the AD1847 (i.e., Control Word, Left Playback and Right Playback data is received on the SDI pin, then the Status Word/Index Readback, Left Capture and Right Capture data is transmitted on the SDO pin).

Slot	Register Name (16-Bit)
0	Control Word Input
1	Left Playback Data Input
2	Right Playback Data Input
3	Status Word/Index Readback Output
4	Left Capture Data Output
5	Right Capture Data Output

Figure 4. Control Register Mapping with TSSEL = 0

Figure 5 shows the mapping of the Control Word, Status Word/Index Readback and Data registers to time slots when TSSEL = 1. Note that the six 16-bit registers "share" three time slots. TSSEL = 1 is used when the SDI and SDO pins are independent inputs and output (i.e., "2-wire" system). This configuration is inefficient in terms of component interconnect (two unidirectional wires for serial data input and output), but efficient in terms of time slot usage (three slots consumed on each of two unidirectional TDM serial buses). When TSSEL = 1, serial data input to the AD1847 occurs concurrently with serial data output from the AD1847 (i.e., Control Word reception on the SDI pin occurs simultaneously with Status Word/Index Readback transmission on the SDO pin).

Slot	Register Name (16-Bit)
0	Control Word Input
1	Left Playback Data Input
2	Right Playback Data Input
0	Status Word/Index Readback Output
1	Left Capture Data Output
2	Right Capture Data Output

Figure 5. Control Register Mapping with TSSEL = 1

An Index Register readback request to an invalid index address (11, 14 and 15) will return the contents of the Status Word. Attempts to write to an invalid index address (11, 14 and 15) will have no effect on the AD1847. As mentioned above, the RREQ bit of the Control Word is used to request Status Word output or Index Register readback output during either time slot 3 (TSSEL = 0) or time slot 0 (TSSEL = 1). RREQ is set for Index Register readback output, and reset for Status Word output. When Index Register readback is requested, the Index Readback bit format is the same as the Control Word bit format. All status bits are updated by the AD1847 before a new Control Word is received (i.e., at frame boundaries). Thus, if TSSEL = 0 and the Control Word written at slot 0 causes some status bits to change, the change will show up in the Status Word transmitted at slot 3 of the same sample.

Control Word (16-Bit)

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
CLOR	MCE	RREQ	res	IA3	IA2	IA1	IA0
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA7:0 — Index Register Data. These bits are the data for the desired AD1847 Index Register referenced by the Index Address. Written by the host CPU or DSP to the AD1847.

IA3:0 — Index Register Address. These bits define the indirect address of the desired AD1847 Index Register. Written by the host CPU or DSP to the AD1847.

RREQ — Read Request. Setting this bit indicates that the current transfer is a request by the host CPU or DSP for readback of the contents of the indirect addressed Index Register. When this bit is set (RREQ = HI), the AD1847 will not transmit its Status Word in the following Status Word/Index readback slot, but will instead transmit the data in the Index Register specified by the Index Address. Although the Index Readback is transmitted in the following Status Word/Index Readback time slot, the format of the Control Word is used (i.e., CLOR, MCE, RREQ and the Index Register Address in the most significant byte, and the readback Index Register Data in the least significant byte). When this bit is reset (RREQ = LO), the AD1847 will transmit its Status Word in the following Status Word/Index Readback time slot.

A read request is serviced in the next available Index Readback time slot. If TSSEL = 0, the Index Register readback data is transmitted in slot 3 of the same sample. If TSSEL = 1, Index Register readback data is transmitted in slot 0 of the next sample. If TSSEL changes from 0 to 1, Index Register readback will occur twice, in slot 3 of the current sample, and slot 0 of the next. If TSSEL changes from 1 to 0, the last read request is lost.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

MCE — Mode Change Enable. This bit must be set (MCE = HI) whenever protected control register bits of the AD1847 are changed. The Data Format register, the Miscellaneous Information register, and the ACAL bit of the Interface Configuration register can NOT be changed unless this bit is set. The DAC outputs will be muted when MCE is set. The user must mute the AUX1 and AUX2 channels when this bit is set (no audio activity should occur). Written by the host CPU or DSP to the AD1847. This bit is HI after reset.

CLOR — Clear Overrange. When this bit is set (CLOR = HI), the overrange bits in the Status Word are updated every sample. When this bit is reset (CLOR = LO), the overrange bits in the Status Word will record the largest overrange value. The largest overrange value is sticky until the CLOR bit is set. Written by the host CPU or DSP to the AD1847. Since there can be up to 2 samples in the data pipeline, a change to CLOR may take up to 2 samples periods to take effect. This bit is HI after reset.

Immediately after reset, the contents of this register is: 1100 0000 0000 0000 (C000h).

Left/Right Playback/Capture Data (16-Bit)

The data formats for Left Playback, Right Playback, Left Capture and Right Capture are all identical.

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
DATA15	DATA14	DATA13	DATA12	DATA11	DATA10	DATA9	DATA8
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA15:0 — Data Bits. These registers contain the 16-bit, MSB first data for capture and playback. The host CPU or DSP reads the capture data from the AD1847. The host CPU or DSP writes the playback data to the AD1847. For 8-bit linear or 8-bit companded modes, only DATA15:8 contain valid data; DATA7:0 are ignored during capture, and are zeroed during playback. Mono mode plays back the same audio sample on both left and right channels. Mono capture only captures data from the left audio channel. See "Serial Data Format" Timing Diagram.

Immediately after reset, the content of these registers is: 0000 0000 0000 0000 (0000h).

Status Word (16-Bit)

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
res	res	RREQ	res	ID3	ID2	ID1	ID0
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
res	res	ORR1	ORR0	ORL1	ORL0	ACI	INIT

INIT — Initialization. This bit is an indication to the host that frame syncs will stop and the serial bus will be shut down. INIT is set HI on the last valid frame. It is reset LO for all other frames. Read by the host CPU or DSP from the AD1847.

The INIT bit is set HI on the last sample before the serial interface is inactivated. The only condition under which the INIT bit is set is when a different sample rate is programmed. If FRS = 0 (32 slots per frame, two samples per frame) and the sample rate is changed in the first sample of the 32 slot frame (i.e., during slots 0 through 15), the INIT bit will be set on the second sample of that frame (i.e., during slots 16 through 31). If FRS = 0 and the sample rate is changed in the second sample of the 32 slot frame, the INIT bit will be set on the second sample of the following frame.

ACI — Autocalibrate In-Progress. This bit indicates that autocalibration is in progress or the Mode Change Enable (MCE) state has been recently exited. When exiting the MCE state with the ACAL bit set, the ACI bit will be set HI for 384 sample periods. When exiting the MCE state with the ACAL bit reset, the ACAL bit will be set HI for 128 sample periods, indicating that offset and filter values are being restored. Read by the host CPU or DSP from the AD1847.

0 – Autocalibration not in progress
1 – Autocalibration is in progress

ACI clear (i.e., reset or LO) should be recognized by first polling for a HI on the sample after the MCE bit is reset, and then polling for a LO. Note that it is important not to start polling until one sample after MCE is reset, because if MCE is set while ACI is HI, an ACI LO on the following sample will suggest a false clear of ACI.

ORL1:0 — Overrange Left Detect. These bits indicate the overrange on the left input channel. Read by the host CPU or DSP from the AD1847.

0 – Greater than −1.0 dB underrange
1 – Between −1.0 dB and 0 dB underrange
2 – Between 0 dB and 1.0 dB overrange
3 – Greater than 1.0 dB overrange

ORR1:0 — Overrange Right Detect. These bits indicate the overrange on the right input channel. Read by the host CPU or DSP from the AD1847.

0 – Greater than −1.0 dB underrange
1 – Between −1.0 dB and 0 dB underrange
2 – Between 0 dB and 1.0 dB overrange
3 – Greater than 1.0 dB overrange

ID3:0 — AD1847 Revision ID. These four bits define the revision level of the AD1847. The first version of the AD1847 is designated ID = 0001. Read by the host CPU or DSP from the AD1847.

RREQ — This bit is reset LO for the Status Word, echoing the RREQ state written by the host CPU or DSP in the previous Control Word. Read by the host CPU or DSP from the AD1847.

res — Reserved for future expansion. All reserved bits read zero (LO).

Immediately after reset, the contents of this register is: 0000 0001 0000 0000 (0100h).

Index Readback (16-Bit)

Data 15	Data 14	Data 13	Data 12	Data 11	Data 10	Data 9	Data 8
CLOR	MCE	RREQ	res	IA3	IA2	IA1	IA0
Data 7	**Data 6**	**Data 5**	**Data 4**	**Data 3**	**Data 2**	**Data 1**	**Data 0**
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

DATA7:0 Index Register Data. These bits are the readback data from the desired AD1847 Index Register referenced by the Index Address from the previous Control Word (with the RREQ bit set). Read by the host CPU or DSP from the AD1847

IA3:0 Index Register Address. These bits echo the indirect address (written during the previous Control Word (with the RREQ bit set)) of the desired AD1847 Index Register to be readback. Read by the host CPU or DSP from the AD1847.

RREQ Read Request. This bit is set HI for Index Readback, echoing the RREQ state written by the host CPU or DSP in the previous Control Word. Read by the host CPU or DSP from the AD1847.

res Reserved for future expansion. All reserved bits read zero (LO).

MCE Mode Change Enable. This bit echoes the MCE state written by the host CPU or DSP during the previous Control Word (with the RREQ bit set). Read by the host CPU or DSP from the AD1847.

CLOR Clear Overrange. This bit echoes the CLOR state written by the host CPU or DSP during the previous Control Word (with the RREQ bit set). Read by the host CPU or DSP from the AD1847.

Immediately after reset, the contents of this register is: 1110 0000 0000 0000 (E000h).

Indirect Mapped Registers

Following in Figure 6 is a table defining the mapping of AD1847 8-bit Index Registers to Index Address. These registers are accessed by writing the appropriate 4-bit Index Address in the Control Word.

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left DAC Control
7	Right DAC Control
8	Data Format
9	Interface Configuration
10	Pin Control
11	Invalid Address
12	Miscellaneous Information
13	Digital Mix Control
14	Invalid Address
15	Invalid Address

Figure 6. Index Register Mapping

A detailed description of each of the Index Registers is given below.

Left Input Control Register (Index Address 0)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0000	LSS1	LSS0	res	res	LIG3	LIG2	LIG1	LIG0

LIG3:0 Left Input Gain Select. The least significant bit of this 16-level gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Write zeros (LO) to all reserved bits.

LSS1:0 Left Input Source Select. These bits select the input source for the left gain stage preceding the left ADC.

0 – Left Line 1 Source Selected
1 – Left Auxiliary 1 Source Selected
2 – Left Line 2 Source Selected
3 – Left Line 1 Post-Mixed Output Loopback Source Selected

This register's initial state after reset is: 0000 0000 (00h).

Right Input Control Register (Index Address 1)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0001	RSS1	RSS0	res	res	RIG3	RIG2	RIG1	RIG0

RIG3:0 Right Input Gain Select. The least significant bit of this 16-level gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Write zeros (LO) to all reserved bits.

RSS1:0 Right Input Source Select. These bits select the input source for the right gain stage preceding the right ADC.

0 – Right Line 1 Source Selected
1 – Right Auxiliary 1 Source Selected
2 – Right Line 2 Source Selected
3 – Right Line 1 Post-Mixed Output Loopback Source Selected

This register's initial state after reset is: 0000 0000 (00h).

Left Auxiliary #1 Input Control Register (Index Address 2)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0010	LMX1	res	res	LX1G4	LX1G3	LX1G2	LX1G1	LX1G0

LX1G4:0 Left Auxiliary Input #1 Gain Select. The least significant bit of this 32-level gain/attenuate select represents −1.5 dB. LX1G4:0 = 0 produces a +12 dB gain. LX1G4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB. Gains referred to 2.0 V p-p full-scale output level.

res Reserved for future expansion. Write zeros (LO) to all reserved bits.

LMX1 Left Auxiliary #1 Mute. This bit, when set HI, will mute the left channel of the auxiliary #1 input source. This bit is HI after reset.

This register's initial state after reset is: 1000 0000 (80h).

Right Auxiliary #1 Input Control Register (Index Address 3)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0011	RMX1	res	res	RX1G4	RX1G3	RX1G2	RX1G1	RX1G0

RX1G4:0 Right Auxiliary Input #1 Gain Select. The least significant bit of this 32-level gain/attenuate select represents −1.5 dB. RX1G4:0 = 0 produces a +12 dB gain. RX1G4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB. Gains referred to 2.0 V p-p full-scale output level.

res Reserved for future expansion. Write zeros (LO) to all reserved bits.

RMX1 Right Auxiliary #1 Mute. This bit, when set to HI, will mute the right channel of the auxiliary #1 input source. This bit is HI after reset.

This register's initial state after reset is: 1000 0000 (80h).

Left Auxiliary #2 Input Control Register (Index Address 4)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0100	LMX2	res	res	LX2G4	LX2G3	LX2G2	LX2G1	LX2G0

LX2G4:0 — Left Auxiliary #2 Gain Select. The least significant bit of this 32-level gain/attenuate select represents −1.5 dB. LX2G4:0 = 0 produces a +12 dB gain. LX2G4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB. Gains referred to 2.0 V p-p full-scale output level.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

LMX2 — Left Auxiliary #2 Mute. This bit, when set HI, will mute the left channel of the auxiliary #2 input source. This bit is HI after reset.

This register's initial state after reset is: 1000 0000 (80h).

Right Auxiliary #2 Input Control Register (Index Address 5)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0101	RMX2	res	res	RX2G4	RX2G3	RX2G2	RX2G1	RX2G0

RX2G4:0 — Right Auxiliary #2 Gain Select. The least significant bit of this 32-level gain/attenuate select represents −1.5 dB. RX2G4:0 = 0 produces a +12 dB gain. RX2G4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB. Gains referred to 2.0 V p-p full-scale output level.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

RMX2 — Right Auxiliary #2 Mute. This bit, when set HI, will mute the right channel of the auxiliary #2 input source. This bit is HI after reset.

This register's initial state after reset is: 1000 0000 (80h).

Left DAC Control Register (Index Address 6)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0110	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5:0 — Left DAC Attenuate Select. The least significant bit of this 64-level attenuate select represents −1.5 dB. LDA5:0 = 0 produces a 0 dB attenuation. Maximum attenuation is −94.5 dB.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

LDM — Left DAC Mute. This bit, when set HI, will mute the left channel output Auxiliary inputs are muted independently with the Left Auxiliary Input Control registers. This bit is HI after reset.

This register's initial state after reset is: 1000 000 (80h).

Right DAC Control Register (Index Address 7)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0111	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5:0 — Right DAC Attenuate Select. The least significant bit of this 64-level attenuate select represents −1.5 dB. RDA5:0 = 0 produces a 0 dB attenuation. Maximum attenuation must be at least −94.5 dB.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

RDM — Right DAC Mute. This bit, when set HI, will mute the right DAC output. Auxiliary inputs are muted independently with the Right Auxiliary Input Control registers. This bit is HI after reset.

This register's initial state after reset is: 1000 000 (80h).

Data Format Register (Index Address 8)

Note: The contents of this register can NOT be changed except when the AD1847 is in the Mode Change Enable (MCE) state (i.e., the MCE bit in the Control Word is HI). Write attempts to this register when the AD1847 is not in the MCE state will not be successful.

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1000	res	FMT	C/L	S/M	CFS2	CFS1	CFS0	CSL

CSL — Clock Source Select. This bit selects the clock source to be used for the audio sample rate.
0 – XTAL1 24.576 MHz
1 – XTAL2 16.9344 MHz

CFS2:0 — Clock Frequency Divide Select. These bits select the audio sample frequency. The audio sample rate depends on which clock source is selected and the frequency of the clock source.

CFS2:0	Divide Factor	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0 –	3072	8.0 kHz	5.5125 kHz
1 –	1536	16.0 kHz	11.025 kHz
2 –	896	27.42857 kHz	18.9 kHz
3 –	768	32.0 kHz	22.05 kHz
4 –	448	Not Supported	37.8 kHz
5 –	384	Not Supported	44.1 kHz
6 –	512	48.0 kHz	33.075 kHz
7 –	2560	9.6 kHz	6.615 kHz

Note that the AD1847's internal oscillators can be overdriven by external clock sources at the crystal inputs. This is the configuration used by serial bus slave codecs in daisy-chained multiple codec systems. If an external clock source is applied, it will be divided down by the selected Divide Factor. The external clock need not be at the recommended crystal frequencies.

S/M — Stereo/Mono Select. This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.
0 – Mono
1 – Stereo

C/L — Companded/Linear Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all input and output data. The type of linear PCM or the type of companded format is defined by the FMT bits.
0 – Linear PCM
1 – Companded

FMT — Format Select. This bit defines the format for all digital audio input and output based on the state of the C/L bit.

Linear PCM (C/L = 0)	Companded (C/L = 1)
0 – 8-bit unsigned linear PCM	0 – 8-bit μ-law companded
1 – 16-bit signed linear PCM	1 – 8-bit A-law companded

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

This register's initial state after reset is: 0000 0000 (00h).

Interface Configuration Register (Index Address 9)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1001	res	res	res	res	ACAL	res	res	PEN

PEN — Playback Enable. This bit will enable the playback of data in the format selected. PEN may be set and reset without setting the MCE bit.

0 – Playback Disabled
1 – Playback Enabled

ACAL — Autocalibrate Enable. This bit determines whether the AD1847 performs an autocalibration when exiting from the Mode Change Enable (MCE) state. If the ACAL bit is not set, the previous autocalibration values are used when returning from the Mode Change Enable (MCE) state and no autocalibration takes place. Autocalibration must be performed after initial power-up for proper operation. This bit is HI after reset.

0 – No autocalibration
1 – Autocalibration allowed

NOTE: The ACAL bit can only be changed when the AD1847 is in the Mode Change Enable (MCE) state.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

This register's initial state after reset is: 0000 1000 (08h).

Pin Control Register (Index Address 10)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1010	XCTL1	XCTL0	CLKTS	res	res	res	res	res

CLKTS — Clockout Three-State. If the BM bit is HI, and the CLKTS bit is HI, then the CLKOUT pin will be three-stated. If the BM bit is HI, and the bit CLKTS is LO, then the CLKOUT pin is not three-stated. If the BM bit is LO, then the CLKOUT pin is always three-stated.

XCTL1:0 — External Control. The state of these independent bits is reflected on the respective XCTL1 and XCTL0 pins of the AD1847.

0 – TTL logic LO on XCTL1, XCTL0 pins
1 – TTL logic HI on XCTL1, XCTL0 pins

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

This register's initial state after reset is: 0000 0000 (00h).

Invalid Address (Index Address 11)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1011	inval	inval	inval	inval	inval	inval	inval	inval

inval — Writes to this index address are ignored. Index readback of this index address will return the Status Word.

Miscellaneous Information Register (Index Address 12)

NOTE: The Miscellaneous Information Register can only be changed when the AD1847 is in the Mode Change Enable (MCE) state. Changes to this register are updated at the next Serial Data Frame Sync (SDFS) boundary. If FRS is LO (i.e., 32 slots per frame), and either TSSEL or FRS change in the first sample of a frame, the change is not updated at the second sample of the same frame, but at the first sample of the next frame.

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1100	FRS	TSSEL	res	res	res	res	res	res

TSSEL — Transmit Slot Select. This bit determines which TDM time slots the AD1847 should transmit on.

0 – Transmit on time slots 3, 4 and 5. Used when SDI and SDO are tied together (i.e., "1-wire" system).
1 – Transmit on slots 0, 1 and 2. Used when SDI and SDO are independent inputs and outputs (i.e., "2-wire" system).

FRS — Frame Size. This bit selects the number of time slots per frame.

0 – Selects 32 slots per frame (two samples per frame sync or frame sync at half the sample rate).
1 – Selects 16 slots per frame (one sample per frame sync or frame sync at the sample rate).

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

This register's initial state after reset is 0000 0000 (00h).

Digital Mix Control Register (Index Address 13)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1101	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME

DME — Digital Mix Enable. This bit enables the digital mix of the ADCs' output with the DACs' input. When enabled, the data from the ADCs is digitally mixed with other data being delivered to the DACs (regardless of whether or not playback [PEN] is enabled, i.e., set). If there is a capture overrun, then the last sample captured before overrun will be used for the digital mix. If playback is enabled (PEN set) and there is a playback underrun, then a midscale zero will be added to the digital mix data.

0 – Digital mix disabled (muted)
1 – Digital mix enabled

DMA5:0 — Digital Mix Attenuation. These bits determine the attenuation of the ADC output data mixed with the DAC input data. The least significant bit of this 64-level attenuate select represents −1.5 dB. Maximum attenuation is −94.5 dB.

res — Reserved for future expansion. Write zeros (LO) to all reserved bits.

This register's initial state after reset is: 0000 0000 (00h).

Invalid Address (Index Address 14)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1110	inval	inval	inval	inval	inval	inval	inval	inval

inval — Writes to this index address are ignored. Index readback of this index address will return the Status Word.

Invalid Address (Index Address 15)

IA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1111	inval	inval	inval	inval	inval	inval	inval	inval

inval — Writes to this index address are ignored. Index readback of this index address will return the Status Word.

ANALOG DEVICES

Parallel-Port 16-Bit SoundPort Stereo Codec

AD1848K

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Supports the Microsoft Windows Sound System*
Multiple Channels of Stereo Input
Analog and Digital Signal Mixing
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
68-Lead PLCC and 64-Lead TQFP Packages
Operation from +5 V Supplies
Byte-Wide Parallel Interface to ISA and EISA Buses
Supports One or Two DMA Channels and Programmed I/O

PRODUCT OVERVIEW

The Parallel-Port AD1848K SoundPort® Stereo Codec integrates the key audio data conversion and control functions into a single integrated circuit. The AD1848K is intended to provide a complete, single-chip audio solution for business audio and multimedia applications requiring operation from a single +5 V supply. It provides a direct, byte-wide interface to both ISA ("AT") and EISA computer buses for simplified implementation on a computer motherboard or add-in card. The AD1848K generates enable and direction controls for IC buffers such as 74_245.

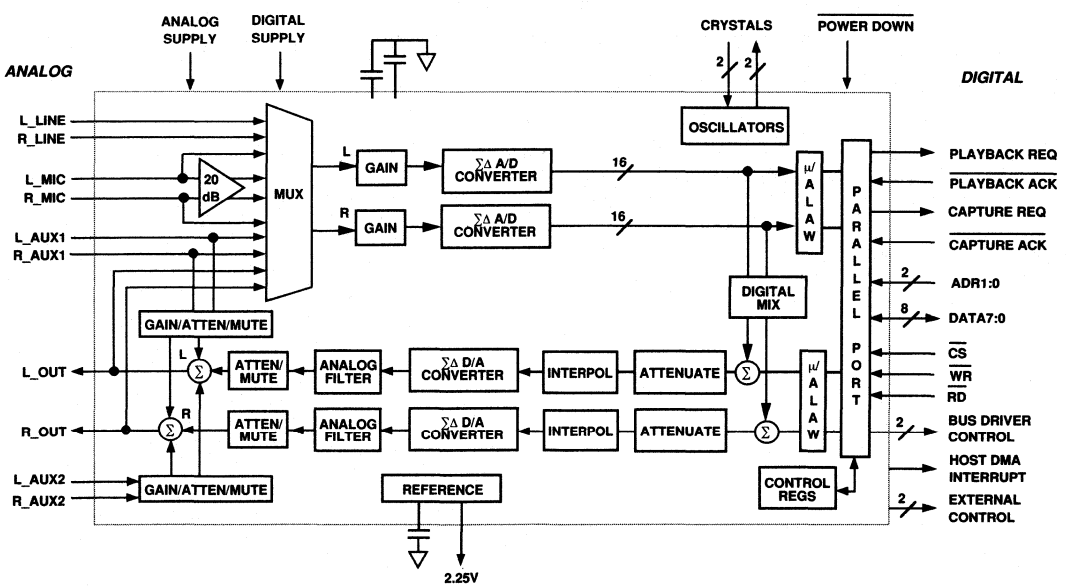
The AD1848K SoundPort Stereo Codec supports a DMA request/grant architecture for transferring data with the host computer bus. One or two DMA channels can be supported. Programmed I/O (PIO) mode is also supported for control register accesses and for applications lacking DMA control. Two input control lines support mixed direct and indirect addressing of twenty-one internal control registers over this asynchronous interface.

External circuit requirements are limited to a minimal number of low cost support components. Anti-imaging DAC output filters are incorporated on-chip. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals.

The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Inputs to the ADC can be selected from four stereo pairs of analog signals: line, microphone ("mic"), auxiliary ("aux") #1, and post-mixed DAC output. The microphone inputs can pass through optional 20 dB gain blocks. A software-controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

*Windows Sound System is a trademark of Microsoft Corp.
SoundPort is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1848K—SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Word Rate (F_S)	48	kHz
Input Signal	1008	Hz
Analog Output Passband	20 Hz to 20 kHz	
ADC FFT Size	2048	
DAC FFT Size	8192	
V_{IH}	2.4	V
V_{IL}	0.8	V
V_{OH}	2.4	V
V_{OL}	0.4	V

DAC Input Conditions
Post-Autocalibrated
0 dB Attenuation
−2.0 dB Relative to Full Scale
16-Bit Linear Mode
No Output Load
Mute Off

ADC Input Conditions
Post-Autocalibrated
0 dB Gain
−3.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode

ANALOG INPUT

	Min	Typ	Max	Units
Input Voltage (RMS Values Assume Sine Wave Input)				
Line		1		V rms
	2.6	2.8	3.0	V p-p
Mic with +20 dB Gain (MGE = 1)		0.1		V rms
	0.26	0.28	0.3	V p-p
Mic with 0 dB Gain (MGE = 0)		1		V rms
	2.6	2.8	3.0	V p-p
Input Impedance	20			kΩ
Input Capacitance			15	pF

PROGRAMMABLE GAIN AMPLIFIER—ADC

	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested, −30 dB Input)	1.3	1.5	1.7	dB
PGA Gain Range Span*	21.5	22.5	23.5	dB

AUXILIARY INPUT ANALOG AMPLIFIERS/ATTENUATORS

	Min	Typ	Max	Units
Step Size (+12.0 dB to −33.0 dB) (All Steps Tested, −14.5 dB Input)	1.3	1.5	1.7	dB
Auxiliary Gain/Attenuation Range Span*	45.5	46.5	47.5	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	$0.45 \times F_S$	Hz
Passband Ripple		±0.1	dB
Transition Band	$0.45 \times F_S$	$0.55 \times F_S$	Hz
Stopband	$0.55 \times F_S$	∞	Hz
Stopband Rejection	74		dB
Group Delay		$30/F_S$	
Group Delay Variation Over Passband		0.0	µs

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution (No Missing Codes from ±10 LSB Ramp Around Midscale)*		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale)	80	86		dB
THD+N (Referenced to Full Scale)			0.022	%
		−77	−73	dB
Signal-to-Intermodulation Distortion*			90	dB
ADC Crosstalk*				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)			−80	dB
Line to MIC (Input LINE, Ground and Select MIC, Read Both Channels)			−80	dB
Line to AUX1			−80	dB
Line to AUX2			−80	dB
Gain Error (Full-Scale Span Relative to Nominal)			±5	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
ADC Offset Error			50	LSBs

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution*		16		Bits
Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale)	80	87		dB
THD+N (Referenced to Full Scale)			0.02	%
		−76	−74	dB
Signal-to-Intermodulation Distortion*			90	dB
Gain Error (Full-Scale Span Relative to Nominal)			±5	%
Interchannel Gain Mismatch (Difference of Gain Errors)			±0.5	dB
DAC Crosstalk* (Input L, Zero R, Measure R_OUT; Input R, Zero L, Measure L_OUT)			−80	dB
Total Out-of-Band Energy* (Measured from $0.55 \times F_S$ to 100 kHz)			−45	dB
Audible Out-of-Band Energy* (Measured from $0.55 \times F_S$ to 22 kHz, All Selectable Sampling Frequencies)			−70	dB

*Guaranteed Not Tested.
Specifications subject to change without notice.

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0 dB to −34.5 dB)	1.3	1.5	1.7	dB
Step Size (−60 dB to −94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation Range Span*	93.5	94.5	95.5	dB

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Output Voltage		0.707		Vrms
	1.85	2.0	2.1	V p-p
Output Impedance			600	Ω
External Load Impedance	10			kΩ
Output Capacitance			15	pF
External Load Capacitance			100	pF
V_{REF}	2.10	2.25	2.40	V
V_{REF} Current Drive		100		μA
V_{REF} Output Impedance		4		kΩ
Mute Attenuation of 0 dB Fundamental* (OUT)			−80	dB
Mute Click (|Muted Output Minus Unmuted Midscale DAC Output|)			5	mV

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
Peak-to-Peak Frequency Response Ripple* (Line In to Line Out)			1.0	dB
Differential Nonlinearity*			±1	Bit
Phase Linearity Deviation*			5	Degrees

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4	(VD+) + 0.3	V
XTAL1/2I	2.4	(VD+) + 0.3	V
Low Level Input Voltage (V_{IL})	−0.3	0.8	V
High Level Output Voltage (V_{OH}) at I_{OH} = −2 mA	2.4		V
Low Level Output Voltage (V_{OL}) at I_{OL} = 2 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	−10	10	μA
Output Leakage Current (GO/NOGO Tested)	−10	10	μA

TIMING PARAMETERS (GUARANTEED OVER OPERATING TEMPERATURE RANGE AND V_{DD} = V_{CC} = 5.0 V ± 5%)

	Min	Max	Units
$\overline{WR}/\overline{RD}$ Strobe Width (t_{STW})	110		ns
$\overline{WR}/\overline{RD}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{BWND})	110		ns
Write Data Setup to $\overline{WR}$ Rising (t_{WDSU})	22		ns
$\overline{RD}$ Falling to Valid Read Data (t_{RDDV})	30	70	ns
$\overline{CS}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{CSSU})	10		ns
$\overline{CS}$ Hold from $\overline{WR}/\overline{RD}$ Rising (t_{CSHD})	0		ns
Adr Setup to $\overline{WR}/\overline{RD}$ Falling (t_{ADSU})	10		ns
Adr Hold from $\overline{WR}/\overline{RD}$ Rising (t_{ADHD})	10		ns
$\overline{DAK}$ Rising to $\overline{WR}/\overline{RD}$ Falling (t_{SUDK1})	60		ns
$\overline{DAK}$ Falling to $\overline{WR}/\overline{RD}$ Rising (t_{SUDK2})	0		ns
$\overline{DAK}$ Setup to $\overline{WR}/\overline{RD}$ Falling (t_{DKSU})	25		ns
Data Hold from $\overline{RD}$ Rising (t_{DHD1})	0	20	ns
Data Hold from $\overline{WR}$ Rising (t_{DHD2})	15		ns
DRQ Hold from $\overline{WR}/\overline{RD}$ Falling (t_{DRHD})	0	25	ns
$\overline{DAK}$ Hold from $\overline{WR}$ Rising (t_{DKHDa})	50		ns
$\overline{DAK}$ Hold from $\overline{RD}$ Rising (t_{DKHDb})	50		ns
$\overline{DBEN}$/DBDIR delay from $\overline{WR}/\overline{RD}$ Falling (t_{DBDL})	0	30	ns

POWER SUPPLY

	Min	Max	Units
Power Supply Range – Analog	4.75	5.25	V
Power Supply Range – 5 V Digital	4.75	5.25	V
Power Supply Current – 5 V Operating (5 V Supplies, 10 kΩ Load)		120	mA
Analog Supply Current – 5 V Operating (10 kΩ Load)		65	mA
Digital Supply Current – 5 V Operating (10 kΩ Load)		55	mA
Digital Power Supply Current – Power Down		1	mA
Analog Power Supply Current – Power Down		1	mA
Power Dissipation – 5 V Operating (Current • Nominal Supplies)		600	mW
Power Dissipation – Power Down (Current • Nominal Supplies)		10	mW
Power Supply Rejection (100 mV p-p Signal @ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40		dB FS

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency		27	MHz
Recommended Clock Duty Cycle Tolerance		±10	%
Initialization Time			
16.9344 MHz Crystal Selected		70	ms
24.576 MHz Crystal Selected		90	ms

*Guaranteed, not tested
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	−0.3	6.0	V
Analog (V_{CC})	−0.3	6.0	V
Input Current (Except Supply Pins)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.3	(VA+) + 0.3	V
Digital Input Voltage (Signal Pins)	−0.3	(VD+) + 0.3	V
Ambient Temperature (Operating)	−40	+85	°C
Storage Temperature	−65	+150	°C
ESD Tolerance (Human Body Model per Method 3015.2 of MIL-STD-883B)	1000		V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

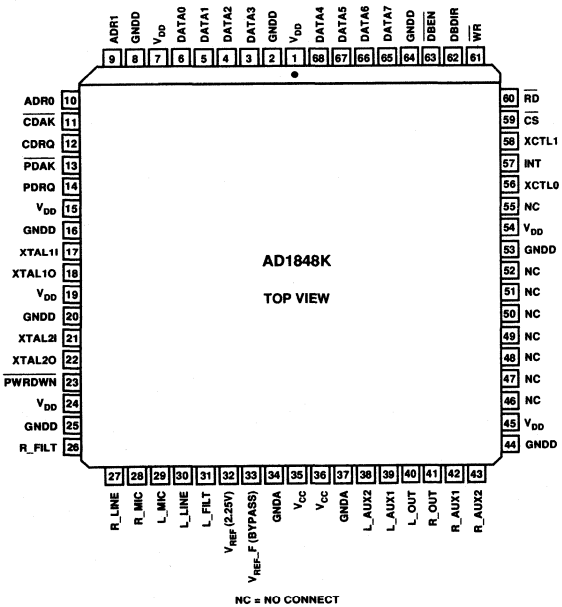
Model	Temperature Range	Package Description	Package Option*
AD1848KP	−40°C to +85°C	68-Lead PLCC	P-68A
AD1848KST	−40°C to +85°C	64-Lead TQFP	ST-64

*For outline information see Package Information section.

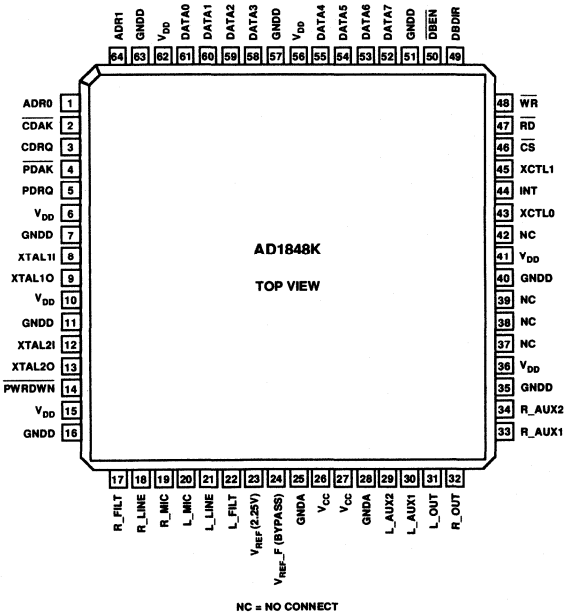
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1848K features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

68-Lead Plastic Leaded Chip Carrier Pinout



64-Lead Thin Quad Flatpack Pinout



PIN DESCRIPTION

Parallel Interface

Pin Name	PLCC	TQFP	I/O	Description
CDRQ	12	3	O	Capture Data Request. The assertion of this signal indicates that the Codec has a captured audio sample from the ADC ready for transfer. This signal will remain asserted until all the bytes from the capture buffer have been transferred.
$\overline{\text{CDAK}}$	11	2	I	Capture Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{RD}}$ cycle occurring is a DMA read from the capture buffer.
PDRQ	14	5	O	Playback Data Request. The assertion of this signal indicates that the Codec is ready for more DAC playback data. The signal will remain asserted until all the bytes needed for a playback sample have been transferred.
$\overline{\text{PDAK}}$	13	4	I	Playback Data Acknowledge. The assertion of this active LO signal indicates that the $\overline{\text{WR}}$ cycle occurring is a DMA write to the playback buffer.
ADR1:0	9 & 10	1 & 64	I	Codec Addresses. These address pins are asserted by the Codec interface logic during a control register/PIO access. The state of these address lines determine which register is accessed.
$\overline{\text{RD}}$	60	47	I	Read Command Strobe. This active LO signal defines a read cycle from the Codec. The cycle may be a read from the control/PIO registers, or the cycles could be a read from the Codec's DMA sample registers.
$\overline{\text{WR}}$	61	48	I	Write Command Strobe. This active LO signal indicates a write cycle to the Codec. The cycle may be a write to the control/PIO registers, or the cycle could be a write to the Codec's DMA sample registers.
$\overline{\text{CS}}$	59	46	I	AD1848K Chip Select. The Codec will not respond to any control/PIO cycle accesses unless this active LO signal is LO. This signal is ignored during DMA transfers.
DATA7:0	3–6 & 65–68	52–55 & 58–61	I/O	Data Bus. These pins transfer data and control information between the Codec and the host.
$\overline{\text{DBEN}}$	63	50	O	Data Bus Enable. This pin enables the external bus drivers. This signal is normally HI. For control register/PIO cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ or $\overline{\text{RD}}$) and $\overline{\text{CS}}$ For DMA cycles, $\overline{\text{DBEN}}$ = ($\overline{\text{WR}}$ or $\overline{\text{RD}}$) and ($\overline{\text{PDAK}}$ or $\overline{\text{CDAK}}$)
DBDIR	62	49	O	Data Bus Direction. This pin controls the direction of the data bus transceiver. HI enables writes from the host to the AD1848K; LO enables reads from the AD1848K to the host bus. This signal is normally HI. For control register/PIO cycles, DBDIR = $\overline{\text{RD}}$ and $\overline{\text{CS}}$ For DMA cycles, DBDIR = $\overline{\text{RD}}$ and ($\overline{\text{PDAK}}$ or $\overline{\text{CDAK}}$)

Analog Signals

Pin Name	PLCC	TQFP	I/O	Description
L_LINE	30	21	I	Left Line Input. Line level input for the left channel.
R_LINE	27	18	I	Right Line Input. Line level input for the right channel.
L_MIC	29	20	I	Left Microphone Input. Microphone input for the left channel. This signal can be either line level or −20 dB from line level.
R_MIC	28	19	I	Right Microphone Input. Microphone input for the right channel. This signal can be either line level or −20 dB from line level.
L_AUX1	39	30	I	Left Auxiliary #1 Line Input
R_AUX1	42	33	I	Right Auxiliary #1 Line Input
L_AUX2	38	29	I	Left Auxiliary #2 Line Input
R_AUX2	43	34	I	Right Auxiliary #2 Line Input
L_OUT	40	31	O	Left Line Level Output
R_OUT	41	32	O	Right Line Level Output

Miscellaneous

Pin Name	PLCC	TQFP	I/O	Description
XTAL1I	17	8	I	24.576 MHz Crystal #1 Input
XTAL1O	18	9	O	24.576 MHz Crystal #1 Output
XTAL2I	21	12	I	16.9344 MHz Crystal #2 Input
XTAL2O	22	13	O	16.9344 MHz Crystal #2 Output
$\overline{\text{PWRDWN}}$	23	14	I	Power-Down Signal. Active LO control places AD1848K in its lowest power consumption mode. All sections of the AD1848K, including the digital interface, are shut down and consume minimal power.
INT	57	44	O	Host Interrupt Pin. This signal is used to notify the host that the DMA Current Count Register has underflowed.
XCTL1:O	56 & 58	43 & 45	O	External Control. These signals reflect the current status of register bits inside the AD1848K. They can be used for signaling or to control external logic.
V_{REF}	32	23	O	Voltage Reference. Nominal 2.25 volt reference available for dc-coupling and level-shifting. V_{REF} should not be used where it will sink or source current.
V_{REF}_F	33	24	I	Voltage Reference Filter. Voltage reference filter point for external bypassing only.
L_FILT	31	22	I	Left Channel Filter Input. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
R_FILT	26	17	I	Right Channel Filter Input. This pin requires a 1.0 μF capacitor to analog ground for proper operation.
N/C	46–52, 55	37–39, 42		No Connect. Do not connect.

Power Supplies

Pin Name	PLCC	TQFP	I/O	Description
V_{CC}	35 & 36	26 & 27	I	Analog Supply Voltage (+5 V)
GNDA	34 & 37	25 & 28	I	Analog Ground
V_{DD}	1, 7, 15, 19, 24, 45, 54	6, 10, 15, 36, 41, 56	I	Digital Supply Voltage (+5 V)
GNDD	2, 8, 16, 20, 25, 44, 53, 64	7, 11, 16, 35, 40, 51, 63	I	Digital Ground

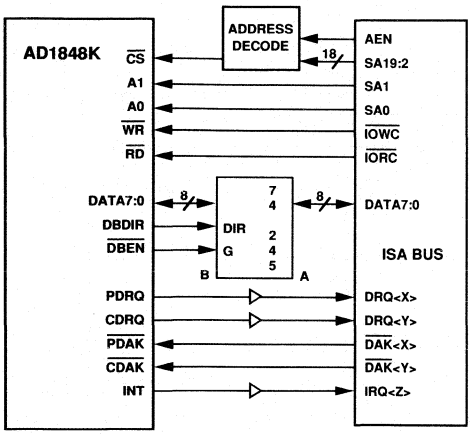


Figure 1. Interface to ISA Bus

The pair of 16-bit outputs from the ADCs is available over a byte-wide bidirectional interface that also supports 16-bit digital input to the DACs and control information. The AD1848K can accept and generate 16-bit twos-complement PCM linear digital data, 8-bit unsigned magnitude PCM linear data, and 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two stereo pairs of auxiliary line-level inputs can also be mixed in the analog domain with the DAC output.

AUDIO FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1848K and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1848K SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. LINE, MIC, and AUX1 inputs and post-mixed DAC output analog stereo signals are multiplexed to the internal programmable gain amplifier stage (PGA). Each channel of the mic inputs can be amplified by +20 dB prior to the PGA to compensate for the voltage swing difference between line levels and typical condenser microphones. Alternatively, the mic inputs can bypass the +20 dB fixed gain block and go straight to the input multiplexer.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left channel inputs appearing at both channel outputs.

Analog Mixing

AUX1 and AUX2 analog stereo signals can be mixed in the analog domain with the DAC output. Each channel of each auxiliary analog input can be independently gained/attenuated from +12 dB to −34.5 dB in −1.5 dB steps or completely muted. The post mixed DAC output is available on OUT externally and as an input to the ADCs.

Even if the AD1848K is not playing back data from its DACs, the analog mix function can still be active.

Analog-to-Digital Datapath

The AD1848K ΣΔ ADCs incorporate a fourth order modulator. A single pole of passive filtering is all that is required for anti-aliasing the analog input due to the ADC's high 64 times oversampling ratio. The ADCs include linear phase digital decimation filters that low-pass filter the input to 0.45 × F_S. ("F_S" is the word rate or "sampling frequency.") ADC input overrange conditions will cause register bits to be set that can be read.

Digital-to-Analog Datapath

The ΣΔ DACs contain a programmable attenuator and a low-pass digital interpolation filter. The anti-imaging interpolation filter nominally oversamples by 64 and digitally filters the higher frequency images. The interpolation ratio is increased at low sample rates to ensure that the shaped quantization noise is inaudible. This feature of the AD1848K represents an improvement over the earlier AD1848J. The attenuator allows independent control of each DAC channel from 0 dB to −94.5 dB in 1.5 dB steps plus full mute. The DACs' ΣΔ noise shapers also oversample by 64 and convert the signal to a single bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output. No external components are required. Phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Changes in DAC output attenuation take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 8 milliseconds at a 48 kHz sampling rate and 48 milliseconds at an 8 kHz sampling rate. (Time out [ms] ≈ 384/F_S [kHz].)

Digital Mixing

Stereo digital output from the ADCs can be mixed digitally with the input to the DACs. Digital output from the ADCs going out of the data port is unaffected by the digital mix. Along the digital mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1848K always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixty-four steps of −1.5 dB attenuation are supported to −94.5 dB. The digital mix datapath can also be completely muted, preventing any mixing of the analog input with the digital input. Note that the level of the mixed signal is also a function of the input PGA settings, since they affect the ADCs' output.

The attenuated digital mix data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators.

In case the AD1848K is capturing data but ADC output data is not removed in time ("ADC overrun"), then the last sample captured before overrun will be used for the digital mix. In case the AD1848K is playing back data but input digital DAC data fails to arrive in time ("DAC underrun"), then a midscale zero will be added to the digital mix data.

Analog Outputs

A stereo line level output is available at external pins. Each channel of this output can be independently muted. When muted, the outputs will settle to a dc value near V_{REF}, the midscale reference voltage.

Digital Data Types

The AD1848K supports four global data types: 16-bit twos-complement linear PCM, eight-bit unsigned linear PCM, companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. Eight-bit data is always left justified in 16-bit fields; said in other words, the MSBs of all data types are always aligned; in yet other words, full-scale representations in all four formats correspond to equivalent full-scale signals. The eight least significant bit positions of 8-bit data in 16-bit fields are ignored on input and zeroed on output.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits.

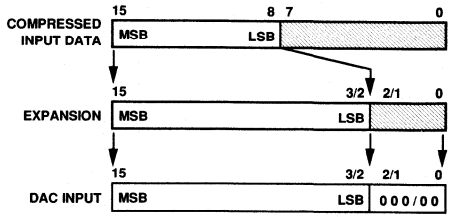


Figure 2. A-Law or μ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified.

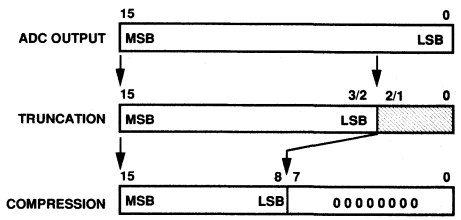


Figure 3. A-Law or μ-Law Compression

Note that all format conversions take place at input or output. Internally, the AD1848K always uses 16-bit linear PCM representations to maintain maximum precision.

Power Supplies and Voltage Reference

The AD1848K operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance though excellent results can be obtained in single supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (V_{REF}). The reference output can be used for biasing op amps used in dc coupling. The internal reference must be externally bypassed to analog ground at the V_{REF}_F pin.

Clocks and Sample Rates

The AD1848K operates from external crystals. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1848K, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates are divided down: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz.

CONTROL REGISTERS

Control Register Architecture

The AD1848K SoundPort Stereo Codec accepts both data and control information through its byte-wide parallel port. Indirect addressing minimizes the number of external pins required to access all 21 of its byte-wide internal registers. Only two external address pins, ADR1:0, are required to accomplish all data and control transfers. These pins select one of five direct registers. (ADR1:0 = 3 addresses two registers, depending on whether the transfer is a playback or a capture.)

ADR1:0	Register Name
0	Index Address Register
1	Indexed Data Register
2	Status Register
3	PIO Data Registers

Figure 4. AD1848K Direct Register Map

A write to or a read from the Indexed Data Register will access the indirect register which is indexed by the value most recently written to the Index Address Register. The Status Register and the PIO Data Register are always accessible directly, without indexing. The 16 indirect registers are indexed in Figure 5.

Index	Register Name
0	Left Input Control
1	Right Input Control
2	Left Aux #1 Input Control
3	Right Aux #1 Input Control
4	Left Aux #2 Input Control
5	Right Aux #2 Input Control
6	Left Output Control
7	Right Output Control
8	Clock and Data Format
9	Interface Configuration
10	Pin Control
11	Test and Initialization
12	Miscellaneous Information
13	Digital Mix
14	Upper Base Count
15	Lower Base Count

Figure 5. AD1848K Indirect Register Map

A detailed map of all direct and indirect register contents is summarized for reference as follows:

Direct Registers:

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

Indirect Registers:

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0
8	res	FMT	L/C	S/M	CFS2	CFS1	CFS0	CSS
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN
10	XCTL1	XCTL0	res	res	res	res	IEN	res
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0
12	res	res	res	res	ID3	ID2	ID1	ID0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

Figure 6. AD1848K Register Summary

Note that the only sticky bit in any of the AD1848K control registers is the interrupt (INT) bit. All other bits change with every sample period.

Direct Control Register Definitions

Index Register (ADR1:0 = 0)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	INIT	MCE	TRD	res	IXA3	IXA2	IXA1	IXA0

IXA3:0 Index Address. These bits define the address of the AD1848K register accessed by the Indexed Data Register. These bits are read/write.

res Reserved for future expansion. Always write a zero to this bit.

TRD Transfer Request Disable. This bit, when set, causes all data transfers to cease when the Interrupt Status (INT) bit of the Status Register is set.

0 Transfers Enabled During Interrupt. PDRQ and CDRQ pin outputs are generated uninhibited by interrupts. DMA Current Counter Register decrements with every sample period when either PEN or CEN are enabled.

1 Transfers Disabled By Interrupt. PDRQ and CDRQ pin outputs are generated only if INT bit is 0 (when either PEN or CEN, respectively, are enabled). Any pending playback or capture requests are allowed to complete at the time when TRD is set. After pending requests complete, midscale inputs will be internally generated for the DACs, and the ADC output buffer will contain the last valid output. Clearing the sticky INT bit (or the TRD bit) will cause the resumption of playback and/or capture requests (presuming PEN and/or CEN are enabled). The DMA Current Counter Register will not decrement while both the TRD bit is set and the INT bit is a one.

MCE Mode Change Enable. This bit must be set whenever the current functional mode of the AD1848K is changed. Specifically, the Clock and Data Format and Interface Configuration registers cannot be changed unless this bit is set. The exceptions are CEN and PEN in the Interface Configuration which can be changed "on-the-fly." MCE should be cleared at the completion of the desired register changes. The DAC outputs are automatically muted when the MCE bit is set. After MCE is cleared, the DAC outputs will be restored to the state specified by the LDM and RDM mute bits.

Both ADCs and DACs are automatically muted for approximately 128 sample cycles after exiting the MCE state to allow the reference and all filters to settle. The ADCs will produce midscale values; the DACs' analog output will be muted. All converters are internally operating during these ≈128 sample cycles, and the AD1848K will expect playback data and will generate (midscale) capture data. Note that the autocalibrate-in-process (ACI) bit will be set on exit from the MCE state regardless of whether or not ACAL was set. ACI will remain HI for these ≈128 sample cycles; system software should poll this bit rather than count cycles.

Special sequences must be followed if autocalibrate (ACAL) is set or sample rates are changed (CFS2:0 and or CSS) during mode change enable. See the "Autocalibration" and "Changing Sample Rates" sections below.

INIT AD1848K Initialization. This bit is set when the AD1848K is in a state which cannot respond to parallel bus cycles. This bit is read only.

Immediately after reset and once the AD1848K has left the INIT state, the initial value of this register will be "0100 0000 (40h)." During AD1848K initialization, this register cannot be written and is always read "1000 0000 (80h)."

Indexed Data Register (ADR1:0 = 1)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	IXD7	IXD6	IXD5	IXD4	IXD3	IXD2	IXD1	IXD0

IXD7:0 Indexed Register Data. These bits contain the contents of the AD1848K register referenced by the Indexed Data Register.

During AD1848K initialization, this register cannot be written and is always read as "1000 0000 (80h)."

Status Register (ADR1:0 = 2)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	CU/L	CL/R	CRDY	SOUR	PU/L	PL/R	PRDY	INT

INT Interrupt Status. This sticky bit (the only one) indicates the status of the interrupt logic of the AD1848K. This bit is cleared by any host write of any value to this register. The IEN bit of the Pin Control Register determines whether the state of this bit is reflected on the INT pin of the AD1848K. The only interrupt condition supported by the AD1848K is generated by the underflow of the DMA Current Count Register.

0 Interrupt pin inactive

1 Interrupt pin active

PRDY Playback Data Register Ready. The PIO Playback Data Register is ready for more data. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 DAC data is still valid. Do not overwrite.

1 DAC data is stale. Ready for next host data write value.

PL/R Playback Left/Right Sample. This bit indicates whether the PIO playback data needed is for the right channel DAC or left channel DAC. This bit is read only.

0 Right channel needed

1 Left channel or mono

PU/L Playback Upper/Lower Byte. This bit indicates whether the PIO playback data needed is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte needed

1 Upper byte needed or any 8-bit mode

SOUR Sample Over/Underrun. This bit indicates that the most recent sample was not serviced in time and therefore either a capture overrun (COR) or playback underrun (PUR) has occurred. The bit indicates an overrun for ADC capture and an underrun for DAC playback. If both capture and playback are enabled, the source which set this bit can be determined by reading COR and PUR. This bit changes on a sample-by-sample basis. This bit is read only.

CRDY Capture Data Ready. The PIO Capture Data Register contains data ready for reading by the host. This bit should only be used when direct programmed I/O data transfers are desired. This bit is read only.

0 ADC data is stale. Do not reread the information.

1 ADC data is fresh. Ready for next host data read.

CL/R Capture Left/Right Sample. This bit indicates whether the PIO capture data waiting is for the right channel ADC or left channel ADC. This bit is read only.

0 Right channel

1 Left channel or mono

CU/L Capture Upper/Lower Byte. This bit indicates whether the PIO capture data ready is for the upper or lower byte of the channel. This bit is read only.

0 Lower byte ready

1 Upper byte ready or any 8-bit mode

The PRDY, CRDY, and INT bits of this status register can change asynchronously to host accesses. The host may access this register while the bits are transitioning. The host read may return a zero value just as these bits are changing, for example. A one value would not be read until the next host access.

This registers's initial state after reset is "1100 1100."

PIO Data Registers (ADR1:0 = 3)

ADR1:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
3	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0

The PIO Data Registers are two registers mapped to the same address. Writes send data to the PIO Playback Data Register (PD7:0). Reads will receive data from the PIO Capture Data Register (CD7:0).

During AD1848K initialization, the PIO Playback Data Register cannot be written and the Capture Data Register is always read "1000 0000 (80h)."

CD7:0 PIO Capture Data Register. This is the control register where capture data is read during programmed I/O data transfers.

The reading of this register will increment the state machine so that the following read will be from the next appropriate byte in the sample. The exact byte which is next to be read can be determined by reading the Status Register. Once all relevant bytes have been read, the state machine will stay pointed to the last byte of the sample until a new sample is received from the ADCs. Once this has occurred, the state machine and status register will point to the first byte of the sample. Until a new sample is received, reads from this register will return the most significant byte of the sample.

PD7:0 PIO Playback Data Register. This is the control register where playback data is written during programmed I/O data transfers.

Writing data to this register will increment the playback byte tracking state machine so that the following write will be to the correct byte of the sample. Once all bytes of a sample have been written, subsequent byte writes to this port are ignored. The state machine is reset when the current sample is sent to the DACs.

Indirect Control Register Definitions

The following control registers are accessed by writing index values to IXA3:0 in the Index Address Register (ADR1:0 = 0) followed by a read/write to the Indexed Data Register (ADR1:0 = 1).

Left Input Control (IXA3:0 = 0)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	LSS1	LSS0	LMGE	res	LIG3	LIG2	LIG1	LIG0

LIG3:0 Left Input Gain Select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LMGE Left Input Microphone Gain Enable. Setting this bit will enable the +20 dB gain of the left mic input signal.

LSS1:0 Left Input Source Select. These bits select the input source for the left gain stage preceding the left ADC.

0 Left Line Source Selected
1 Left Auxiliary 1 Source Selected
2 Left Microphone Source Selected
3 Left Line Post-Mixed DAC Output Source Selected

This register's initial state after reset is "0000 0000."

Right Input Control (IXA3:0 = 1)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
1	RSS1	RSS0	RMGE	res	RIG3	RIG2	RIG1	RIG0

RIG3:0 Right Input Gain Select. The least significant bit of this gain select represents +1.5 dB. Maximum gain is +22.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RMGE Right Input Mic Gain Enable. Setting this bit will enable the +20 dB gain of the right mic input signal.

RSS1:0 Right Input Source Select. These bits select the input source for the right channel gain stage preceding the right ADC.

0 Right Line Source Selected
1 Right Auxiliary 1 Source Selected
2 Right Microphone Source Selected
3 Right Post-Mixed DAC Output Source Selected

This register's initial state after reset is "0000 0000."

Left Auxiliary #1 Input Control (IXA3:0 = 2)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
2	LMX1	res	res	LX1A4	LX1A3	LX1A2	LX1A1	LX1A0

LX1A4:0 Left Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. LX1X4:0 = 0 produces a +12 dB gain. LX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX1 Left Auxiliary #1 Mute. This bit, when set, will mute the left channel of the Auxiliary #1 input source. This bit powers up set.

This register's initial state after reset is "1000 0000 (80h)."

Right Auxiliary #1 Input Control (IXA3:0 = 3)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
3	RMX1	res	res	RX1A4	RX1A3	RX1A2	RX1A1	RX1A0

RX1A4:0 Right Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. RX1A4:0 = 0 produces a +12 dB gain. RX1A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX1 Right Auxiliary #1 Mute. This bit, when set, will mute the right channel of the Auxiliary #1 input source. This bit powers up set.

This register's initial state after reset is "1000 0000 (80h)."

Left Auxiliary #2 Input Control (IXA3:0 = 4)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
4	LMX2	res	res	LX2A4	LX2A3	LX2A2	LX2A1	LX2A0

LX2A4:0 Left Auxiliary Input #2 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. LX2A4:0 = 0 produces a +12 dB gain. LX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

LMX2 Left Auxiliary #2 Mute. This bit, when set to 1, will mute the left channel of the Auxiliary #2 input source. This bit powers up set.

This register's initial state after reset is "1000 0000 (80h)."

Right Auxiliary #2 Input Control (IXA3:0 = 5)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
5	RMX2	res	res	RX2A4	RX2A3	RX2A2	RX2A1	RX2A0

RX2A4:0 Right Auxiliary Input #1 Attenuate Select. The least significant bit of this gain/attenuate select represents −1.5 dB. RX2A4:0 = 0 produces a +12 dB gain. RX2A4:0 = "01000" (8 decimal) produces 0 dB gain. Maximum attenuation is −34.5 dB.

res Reserved for future expansion. Always write zeros to these bits.

RMX2 Right Auxiliary #2 Mute. This bit, when set, will mute the right channel of the Auxiliary #2 input source. This bit powers up set.

This register's initial state after reset is "1000 0000 (80h)."

Left DAC Control (IXA3:0 = 6)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
6	LDM	res	LDA5	LDA4	LDA3	LDA2	LDA1	LDA0

LDA5:0 Left DAC Attenuate Select. The least significant bit of this attenuate select represents −1.5 dB. LDA5:0 = 0 produces a 0 dB attenuation. Maximum attenuation is −94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

LDM Left DAC Mute. This bit, when set to 1, will mute the left DAC output. Auxiliary inputs are muted independently with the Left Auxiliary Input Control Registers. This bit powers up set.

This register's initial state after reset is "1x00 0000."

Right DAC Control (IXA3:0 = 7)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
7	RDM	res	RDA5	RDA4	RDA3	RDA2	RDA1	RDA0

RDA5:0 Right DAC Attenuate Select. The least significant bit of this attenuate select represents −1.5 dB. RDA5:0 = 0 produces 0 dB attenuation. Maximum attenuation is −94.5 dB.

res Reserved for future expansion. Always write a zero to this bit.

RDM Right DAC Mute. This bit, when set to 1, will mute the right DAC output. Auxiliary inputs are muted independently with the Right Auxiliary Input Control Registers. This bit powers up set.

This register's initial state after reset is "1x00 0000."

Clock and Data Format Register (IXA3:0 = 8)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
8	res	FMT	L/C	S/M	CFS2	CFS1	CFS0	CSS

The contents of the Clock and Data Format Register cannot be changed except when the AD1848K is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1848K is not in the MCE state will not be successful.

CSS — Clock Source Select. This bit selects the crystal clock source which will be used for the audio sample rate.

0 XTAL1 (24.576 MHz)

1 XTAL2 (16.9344 MHz)

CFS2:0 — Clock Frequency Divide Select. These bits select the audio sample rate frequency. The actual audio sample rate depends on which crystal clock source is selected and the frequency of that source.

CFS	Divide Factor	XTAL1 24.576 MHz	XTAL2 16.9344 MHz
0	3072	8.0 kHz	5.5125 kHz
1	1536	16.0 kHz	11.025 kHz
2	896	27.42857 kHz	18.9 kHz
3	768	32.0 kHz	22.05 kHz
4	448	Not Supported	37.8 kHz
5	384	Not Supported	44.1 kHz
6	512	48.0 kHz	33.075 kHz
7	2560	9.6 kHz	6.615 kHz

Note that the AD1848K's internal oscillators can be overdriven by external clock sources at the crystal input pins. If an external clock source is applied, it will be divided down by the selected Divide Factor. It need not be at the recommended crystal frequencies.

S/M — Stereo/Mono Select. This bit determines how the audio data streams are formatted. Selecting stereo will result with alternating samples representing left and right audio channels. Mono playback plays the same audio sample on both channels. Mono capture only captures data from the left audio channel.

0 Mono

1 Stereo

L/C — Linear/Companded Select. This bit selects between a linear digital representation of the audio signal or a nonlinear, companded format for all input and output data. The type of linear PCM or the type of companded format is defined by the FMT bits.

0 Linear PCM

1 Companded

FMT — Format Select. This bit defines the format for all digital audio input and outputs based on the state of the L/C bit.

	Linear PCM (L/C = 0)	Companded (L/C = 1)
0	8-bit Unsigned PCM	8-bit μ-law Companded
1	16-bit Twos-Complement PCM	8-bit A-law Companded

res — Reserved for future expansion. Always write a zero to this bit.

This register's initial state after reset is "x000 0000."

Interface Configuration Register (IXA3:0 = 9)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
9	CPIO	PPIO	res	res	ACAL	SDC	CEN	PEN

The contents of the Interface Configuration Register cannot be changed except when the AD1848K is in Mode Change Enable (MCE) state. Write attempts to this register when the AD1848K is not in the MCE state will not be successful. PEN and CEN are exceptions; these bits may always be written.

PEN Playback Enable. This bit will enable the playback of data in the format selected. The AD1848K will generate PDRQ and respond to $\overline{\text{PDAK}}$ signals when this bit is enabled and PPIO = 0. If PPIO = 1, this bit enables Programmed I/O (PIO) playback mode. PEN may be set and reset without setting the MCE bit.

0 Playback disabled (PDRQ and PIO Playback Data Register inactive)

1 Playback enabled

CEN Capture Enable. This bit will enable the capture of data in the format selected. The AD1848K will generate CDRQ and respond to $\overline{\text{CDAK}}$ signals when this bit is enabled and CPIO = 0. If CPIO = 1, this bit enables PIO capture mode. CEN may be set and reset without setting the MCE bit.

0 Capture disabled (CDRQ and PIO Capture Data Register inactive)

1 Capture enabled

SDC Single DMA Channel. This bit will force both capture and playback DMA requests to occur on the Playback DMA channel. The Capture DMA CDRQ pin will be LO. This bit will allow the AD1848K to be used with only one DMA channel. Simultaneous capture and playback cannot occur in this mode. Should both capture and playback be enabled (CEN = PEN = 1) in the mode, only playback will occur. See "Data and Control Transfers" for further explanation.

0 Dual DMA channel mode

1 Single DMA channel mode

ACAL Autocalibrate Enable. This bit determines whether the AD1848K performs an autocalibrate whenever the $\overline{\text{PWRDWN}}$ pin is deasserted or from the Mode Change Enable (MCE) bit being reset. ACAL is normally set. See "Autocalibration" below for a description of a complete autocalibration sequence.

0 No autocalibration

1 Autocalibration after power down/reset or mode change

res Reserved for future expansion. Always write zeros to these bits.

PPIO Playback PIO Enable. This bit determines whether the playback data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

CPIO Capture PIO Enable. This bit determines whether the capture data is transferred via DMA or PIO.

0 DMA transfers only

1 PIO transfers only

This register's initial state after reset is "00xx 1000 (x8h)."

Pin Control Register (IXA3:0 = 10)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
10	XCTL1	XCTL0	res	res	res	res	IEN	res

res Reserved for future expansion. Always write zeros to these bits.

IEN Interrupt Enable. This bit enables the interrupt pin. The Interrupt Pin will go active HI when the number of samples programmed in the Base Count Register is reached.

0 Interrupt disabled

1 Interrupt enabled

XCTL1:0 External Control. The state of these independent bits is reflected on the respective XCTL1:0 pins of the AD1848K.

0 TTL Logic LO on XCTL1:0 pins

1 TTL Logic HI on XCTL1:0 pins

This register's initial state after reset is "00xx xx0x."

Test and Initialization Register (IXA3:0 = 11)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
11	COR	PUR	ACI	DRS	ORR1	ORR0	ORL1	ORL0

ORL1:0 Overrange Left Detect. These bits indicate the overrange on the left input channel. This bit changes on a sample-by-sample basis. This bit is read only.

0 Less than −1 dB underrange

1 Between −1 dB and 0 dB underrange

2 Between 0 dB and +1 dB overrange

3 Greater than +1 dB overrange

ORR1:0 Overrange Right Detect. These bits indicate the overrange on the right input channel. This bit changes on a sample-by-sample basis. This bit is read only.

0 Less than −1 dB underrange

1 Between −1 dB and 0 dB underrange

2 Between 0 dB and +1 dB overrange

3 Greater than +1 dB overrange

DRS Data Request Status. This bit indicates the current status of the PDRQ and CDRQ pins of the AD1848K.

0 CDRQ and PDRQ are presently inactive (LO)

1 CDRQ or PDRQ are presently active (HI)

ACI Autocalibrate-In-Progress. This bit indicates the state of autocalibration or a recent exit from Mode Change Enable (MCE). This bit is read only.

0 Autocalibration is not in progress

1 Autocalibration is in progress or MCE was exited within approximately the last 128 sample periods

PUR Playback Underrun. This bit is set when playback data has not arrived from the host in time to be played. As a result, a midscale value will be sent to the DACs. This bit changes on a sample by sample basis.

COR Capture Overrun. This bit is set when the capture data has not been read by the host before the next sample arrives. The sample being read will not be overwritten by the new sample. The new sample will be ignored. This bit changes on a sample by sample basis.

The occurrence of a PUR and/or COR is designated in the Status Register's Sample Overrun/Underrun (SOUR) bit. The SOUR bit is the logical OR of the COR and PUR bits. This enables a polling host CPU to detect an overrun/underrun condition while checking other status bits.

This register's initial state after reset is "0000 0000."

Miscellaneous Control Register (IXA3:0 = 12)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
12	res	res	res	res	ID3	ID2	ID1	ID0

res Reserved for future expansion. The bits are read only. Do not write to these bits.

ID3:0 AD1848K Revision ID. These four bits define the revision level of the AD1848K. Revisions increment by one LSB. The K-Grade revision is ID = "1010." These bits are read only.

This register's initial state after reset is "xxxx RRRR" where RRRR = Revision ID of the silicon in use.

Digital Mix Control Register (IXA3:0 = 13)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
13	DMA5	DMA4	DMA3	DMA2	DMA1	DMA0	res	DME

DME Digital Mix Enable. This bit will enable the digital mix of the ADCs' output with the DACs' input. When enabled, the data from the ADCs are digitally mixed with other data being delivered to the DACs (regardless of whether or not playback [PEN] is enabled, i.e., set). If capture is enabled (CEN set) and there is a capture overrun (COR), then the last sample captured before overrun will be used for the digital mix. If playback is enabled (PEN set) and there is a playback underrun (PUR), then a midscale zero will be added to the digital mix data.

0 Digital mix disabled (muted)

1 Digital mix enabled

res Reserved for future expansion. Always write a zero to this bit.

DMA5:0 Digital Mix Attenuation. These bits determine the attenuation of the ADC data in mixing with the DAC input. Each attenuate step is −1.5 dB ranging to −94.5 dB.

This register's initial state after reset is "0000 00x0."

DMA Base Count Registers (IXA3:0 = 14 & 15)

The DMA Base Count Registers in the AD1848K simplify integration of the AD1848K in ISA systems. The ISA DMA controller requires an external count mechanism to notify the host CPU via interrupt of a full DMA buffer. The programmable DMA Base Count Registers will allow such interrupts to occur.

The Base Count Registers contain the number of sample periods which will occur before an interrupt is generated on the interrupt (INT) pin. To load, first write a value to the Lower Base Count Register. Writing a value to the Upper Base Register will cause both Base Count Registers to load into the Current Count Register. Once AD1848K transfers are enabled, each sample period the Current Count Register will decrement until zero count is reached. The next sample period after zero will generate the interrupt and reload the Current Count Register with the values in the Base Count Registers. The interrupt is cleared by a write to the Status Register.

The Host Interrupt Pin (INT) will go HI during the sample period in which the Current Count Register underflows when Interrupt Enable (IEN) is set. It will go LO when the Interrupt Status (INT) bit is cleared. Note that both the bit and the pin have the same name (INT). The Current Count Register is decremented every sample period when either the PEN or CEN bit is enabled and also either the Transfer Request Disable (TRD) bit or the Interrupt Status (INT) bit are zero. Note that the internal INT bit will become one on counter underflow even if the external interrupt pin is not enabled, i.e., IEN is zero. The Current Count Register is decremented in both PIO and DMA data transfer modes.

Upper Base Count Register (IXA3:0 = 14)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
14	UB7	UB6	UB5	UB4	UB3	UB2	UB1	UB0

UB7:0 Upper Base Count. This byte is the upper byte of the base count register containing the eight most significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters can not be read.

This register's initial state after reset is "0000 0000."

Lower Upper Base Count Register (IXA3:0 = 15)

IXA3:0	Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
15	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0

LB7:0 Lower Base Count. This byte is the lower byte of the base count register containing the eight least significant bits of the 16-bit base register. Reads from this register return the same value which was written. The current count contained in the counters cannot be read.

This register's initial state after reset is "0000 0000."

Serial-Port 16-Bit SoundPort Stereo Codec

AD1849K

FEATURES

Single-Chip Integrated ΣΔ Digital Audio Stereo Codec
Multiple Channels of Stereo Input and Output
Digital Signal Mixing
On-Chip Speaker and Headphone Drive Capability
Programmable Gain and Attenuation
On-Chip Signal Filters
Digital Interpolation and Decimation
Analog Output Low-Pass
Sample Rates from 5.5 kHz to 48 kHz
44-Lead PLCC and TQFP Packages
Operation from +5 V and Mixed +5 V/+3.3 V Supplies
Serial Interface Compatible with ADSP-21xx Fixed-Point DSμPs
Compatible with CS4215 (See Text)

PRODUCT OVERVIEW

The Serial-Port AD1849K SoundPort® Stereo Codec integrates the key audio data conversion and control functions into a single integrated circuit. The AD1849K is intended to provide a complete, single-chip audio solution for multimedia applications requiring operation from a single +5 V supply. External signal path circuit requirements are limited to three low tolerance capacitors for line level applications; anti-imaging filters are incorporated on-chip. The AD1849K includes on-chip monaural speaker and stereo headphone drive circuits that require no additional external components. Dynamic range exceeds 80 dB over the 20 kHz audio band. Sample rates from 5.5 kHz to 48 kHz are supported from external crystals, from an external clock, or from the serial interface bit clock.

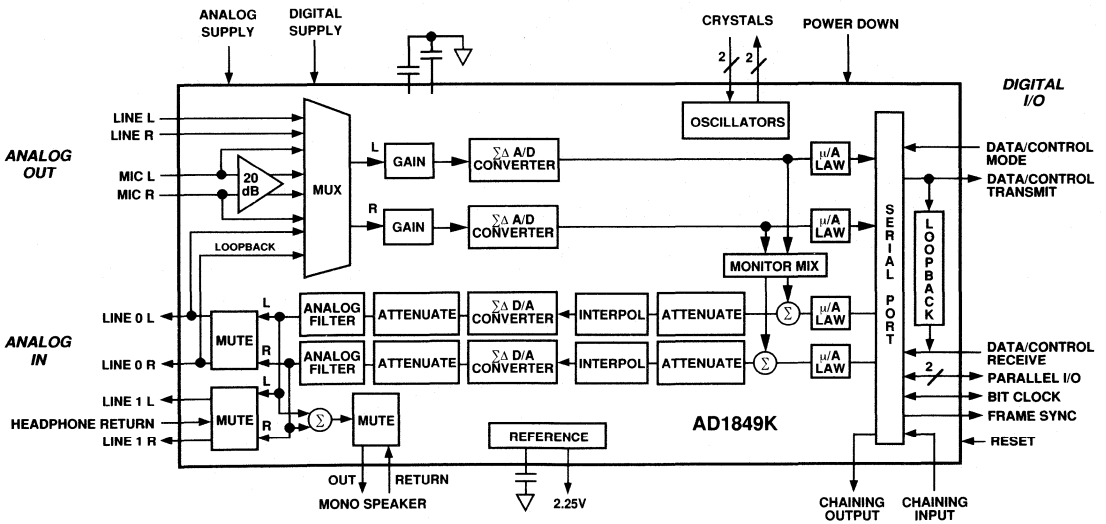
The Codec includes a stereo pair of ΣΔ analog-to-digital converters and a stereo pair of ΣΔ digital-to-analog converters. Analog signals can be input at line levels or microphone levels. A software controlled programmable gain stage allows independent gain for each channel going into the ADC. The ADCs' output can be digitally mixed with the DACs' input.

The left and right channel 16-bit outputs from the ADCs are available over a single bidirectional serial interface that also supports 16-bit digital input to the DACs and control information. The AD1849K can accept and generate 8-bit μ-law or A-law companded digital data.

The ΣΔ DACs are preceded by a digital interpolation filter. An attenuator provides independent user volume control over each DAC channel. Nyquist images and shaped quantization noise are removed from the DACs' analog stereo output by on-chip switched-capacitor and continuous-time filters. Two independent stereo pairs of line-level (or one line-level and one headphone) outputs are generated, as well as drive for a monaural (mono) speaker.

SoundPort is a registered trademark of Analog Devices, Inc.

FUNCTIONAL BLOCK DIAGRAM



This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1849K—SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

STANDARD TEST CONDITIONS UNLESS OTHERWISE NOTED

Temperature	25	°C
Digital Supply (V_{DD})	5.0	V
Analog Supply (V_{CC})	5.0	V
Clock (SCLK)	256	F_S
Master Mode	256 Bits per Frame	
Word Rate (F_S)	48	kHz
Input Signal	1	kHz
Analog Output Passband	20 Hz to 20 kHz	
V_{IH}	2.4	V
V_{IL}	0.8	V
External Load Impedance (Line 0)	10	kΩ
External Load Impedance (Line 1)	48	Ω
External Load Capacitance (Line 0, 1)	100	pF

DAC Input Conditions
0 dB Attenuation
Full-Scale Digital Inputs
16-Bit Linear Mode
OLB = 1

ADC Input Conditions
0 dB PGA Gain
−3.0 dB Relative to Full Scale
Line Input
16-Bit Linear Mode

All tests are performed on all ADC and DAC channels.

ANALOG INPUT

	Min	Typ	Max	Units
Input Voltage*				
(RMS Values Assume Sine Wave Input)				
Line and Mic with 0 dB Gain	0.94	0.99	1.04	V rms
	2.66	2.80	2.94	V p-p
Mic with +20 dB Gain	0.094	0.099	0.104	V rms
	0.266	0.280	0.294	V p-p
Input Capacitance			15	pF

*Accounts for Sum of Worst Case Reference Errors and Worst Case Gain Errors.

PROGRAMMABLE GAIN AMPLIFIER—ADC

	Min	Typ	Max	Units
Step Size (0 dB to 22.5 dB) (All Steps Tested, −30 dB Input)	1.3	1.5	1.7	dB
PGA Gain Range*				
Line and Mic with 0 dB Gain	−0.2		22.7	dB
Mic with +20 dB Gain	19.8		42.7	dB

DIGITAL DECIMATION AND INTERPOLATION FILTERS*

	Min	Max	Units
Passband	0	0.45 × F_S	Hz
Passband Ripple		±0.1	dB
Transition Band	0.45 × F_S	0.55 × F_S	Hz
Stopband	≥ 0.55 × F_S		Hz
Stopband Rejection	74		dB
Group Delay		30/F_S	
Group Delay Variation Over Passband		0.0	μs

ANALOG-TO-DIGITAL CONVERTERS

	Min	Typ	Max	Units
Resolution*		16		Bits
ADC Dynamic Range, A-Weighted Line and Mic with 0 dB Gain (−60 dB Input, THD+N Referenced to Full Scale) Mic with +20 dB Gain (−60 dB Input, THD+N Referenced to Full Scale)	78 72	83 74		dB dB
ADC THD+N, (Referenced to Full Scale) Line and Mic with 0 dB Gain Mic with +20 dB Gain		0.013 −78 0.032 −70	0.020 −74 0.056 −65	% dB % dB
ADC Crosstalk Line to Line (Input L, Ground R, Read R; Input R, Ground L, Read L) Line to Mic (Input LINL & R, Ground and Select MINL & R, Read Both Channels)			−80 −60	dB dB
Gain Error (Full-Scale Span Relative to Nominal)			0.75	dB
ADC Interchannel Gain Mismatch (Line and Mic) (Difference of Gain Errors)			0.3	dB

DIGITAL-TO-ANALOG CONVERTERS

	Min	Typ	Max	Units
Resolution*		16		Bits
DAC Dynamic Range (−60 dB Input, THD+N Referenced to Full Scale)	80	86		dB
DAC THD+N (Referenced to Full Scale) Line 0 and 1 (10 kΩ Load) Line 1 (48 Ω Load) Mono Speaker (48 Ω Load)		0.010 −80 0.022 −73 0.045 −67	0.020 −74 0.100 −60 0.100 −60	% dB % dB % dB
DAC Crosstalk (Input L, Zero R, Measure LOUT0R & 1R; Input R, Zero L, Measure LOUT0L & 1L)			−80	dB
Gain Error (Full-Scale Span Relative to Nominal)			0.75	dB
DAC Interchannel Gain Mismatch (Line 0 and 1) (Difference of Gain Errors)			0.3	dB
Total Out-of-Band Energy* (Measured from 0.55 × F_S to 100 kHz)			−60	dB
Audible Out-of-Band Energy* (Measured from 0.55 F_S to 22 kHz, All Selectable Sampling Frequencies)			−72	dB

*Guaranteed, not tested.

MONITOR MIX ATTENUATOR

	Min	Typ	Max	Units
Step Size (0.0 dB to −60 dB)*	1.3	1.5	1.7	dB
Step Size (−61.5 dB to −94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation*	−95		0.2	dB

DAC ATTENUATOR

	Min	Typ	Max	Units
Step Size (0.0 dB to −60 dB) (Tested at Steps −1.5 dB, −19.5 dB, −39 dB and −60 dB)	1.3	1.5	1.7	dB
Step Size (−61.5 dB to −94.5 dB)*	1.0	1.5	2.0	dB
Output Attenuation*	−95		0.2	dB

SYSTEM SPECIFICATIONS

	Min	Typ	Max	Units
System Frequency Response* (Line In to Line Out, 0 to 0.45 × F_S)	−0.5		+0.2	dB
Differential Nonlinearity*			±0.9	LSB
Phase Linearity Deviation*			5	Degrees

ANALOG OUTPUT

	Min	Typ	Max	Units
Full-Scale Output Voltage (Line 0 & 1)		0.707		V rms
[OLB = 1]	1.85	2.0	2.1	V p-p
Full-Scale Output Voltage (Line 0)		1.0		V rms
[OLB = 0]		2.8		V p-p
Full-Scale Output Voltage (Line 1) [OLB = 0]		4.0		V p-p
Full-Scale Output Voltage (Mono Speaker) [OLB = 1]		4.0		V p-p
Full-Scale Output Voltage (Mono Speaker) [OLB = 0]		8.0		V p-p
CMOUT Voltage (No Load)	1.80	2.25	2.50	V
CMOUT Current Drive*		100		μA
CMOUT Output Impedance		4		kΩ
Mute Attenuation of 0 dB Fundamental* (LINE 0, 1, & MONO)			−80	dB

STATIC DIGITAL SPECIFICATIONS

	Min	Max	Units
High Level Input Voltage (V_{IH})			
Digital Inputs	2.4	(V_{DD}+) + 0.3	V
XTAL1/2I	2.4	(V_{DD}+) + 0.3	V
Low Level Input Voltage (V_{IL})	−0.3	0.8	V
High Level Output Voltage (V_{OH}) at I_{OH} = −2 mA	2.4		V
Low Level Output Voltage (V_{OL}) at I_{OL} = 2 mA		0.4	V
Input Leakage Current (GO/NOGO Tested)	−10	10	μA
Output Leakage Current (GO/NOGO Tested)	−10	10	μA

DIGITAL TIMING PARAMETERS (Guaranteed over +4.75 V to +5.25 V, 0°C to +70°C)

	Min	Typ	Max	Units
SCLK Period (t_{CLK})				
Slave Mode, MS = 0	80			ns
Master Mode, MS = 1*		1/(F_S × Bits per Frame)		s
SCLK HI (t_{HI})*				
Slave Mode, MS = 0	25			ns
SCLK LO (t_{LO})*				
Slave Mode, MS = 0	25			ns
CLKIN Frequency			13.5	MHz
CLKIN HI	30			ns
CLKIN LO	30			ns
Crystals Frequency			27	
Input Setup Time (t_S)	15			ns
Input Hold Time (t_{IH})	10			ns
Output Delay (t_D)			25	ns
Output Hold Time (t_{OH})	0			ns
Output Hi-Z to Valid (t_{ZV})	15			ns
Output Valid to Hi-Z (t_{VZ})			20	ns
Power Up $\overline{\text{RESET}}$ LO Time	50			ms
Operating $\overline{\text{RESET}}$ LO Time	100			ns

POWER SUPPLY

	Min	Typ	Max	Units
Power Supply Voltage Range* —Digital and Analog	4.75		5.25	V
Power Supply Current—Operating (50% I_{VDD}, 50% I_{VCC}, Unloaded Outputs)		100	130	mA
Power Supply Current—Power Down		20	200	μA
Power Supply Rejection (@ 1 kHz)* (At Both Analog and Digital Supply Pins, Both ADCs and DACs)	40			dB

CLOCK SPECIFICATIONS*

	Min	Max	Units
Input Clock Frequency, Crystals		27	MHz
Clock Duty Cycle Tolerance		±10	%
Sample Rate (F_S)	5.5125	50	kHz

*Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
Power Supplies			
Digital (V_{DD})	−0.3	6.0	V
Analog (V_{CC})	−0.3	6.0	V
Input Current (Except Supply Pins and MOUT, MOUTR, LOUT1R, LOUT1L, LOUT1C)		±10.0	mA
Analog Input Voltage (Signal Pins)	−0.3	(V_{CC}+) + 0.3	V
Digital Input Voltage (Signal Pins)	−0.3	(V_{DD}+) + 0.3	V
Ambient Temperature (Operating)	0	+70	°C
Storage Temperature	−65	+150	°C
ESD Tolerance (Human Body Model per Method 3015.2 of MIL-STD-883B)	500		V

WARNING: CMOS device. May be susceptible to high voltage transient-induced latchup.

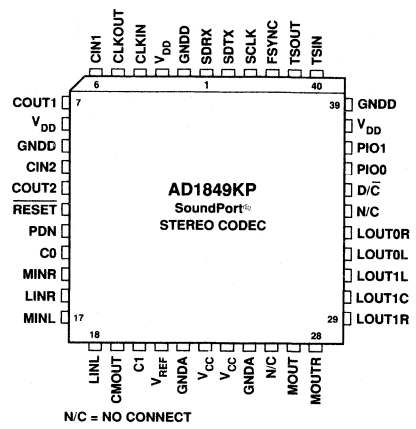
*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1849KP	0°C to +70°C	44-Lead PLCC	P-44A
AD1849KST	0°C to +70°C	44-Lead TQFP	ST-44

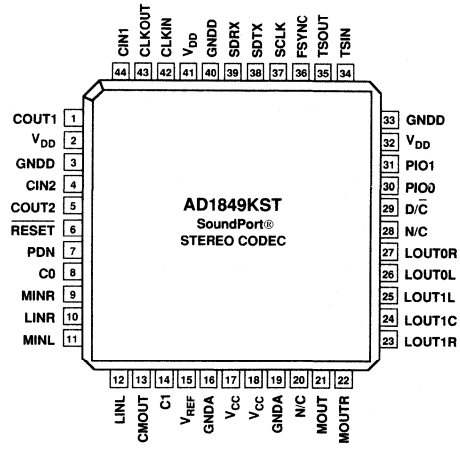
*For outline information see Package Information section.

44-Lead Plastic Leaded Chip Carrier Pinout



N/C = NO CONNECT

44-Lead TQFP



N/C = NO CONNECT

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1849K features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN DESCRIPTION

Digital Signals

Pin Name	PLCC	TQFP	I/O	Description
SDRX	1	39	I	Receive Serial Data Pin
SDTX	44	38	O	Transmit Serial Data Pin
SCLK	43	37	I/O	Bidirectional Serial Bit Clock
FSYNC	42	36	O	Frame Sync Output Signal
TSOUT	41	35	O	Chaining Word Output
TSIN	40	34	I	Chaining Word Input
D/$\overline{C}$	35	29	I	Data/Control Select Input
CIN1	6	44	I	Crystal 1 Input
COUT1	7	1	O	Crystal 1 Output
CIN2	10	4	I	Crystal 2 Input
COUT2	11	5	O	Crystal 2 Output
CLKIN	4	42	I	External Sample Clock Input (256 × F_S)
CLKOUT	5	43	O	External Sample Clock Output (256 × F_S)
$\overline{PDN}$	13	7	I	Power Down Input (Active HI)
$\overline{RESET}$	12	6	I	Reset Input (Active LO)
PIO1	37	31	I/O	Parallel Input/Output Bit 1
PIO0	36	30	I/O	Parallel Input/Output Bit 0

Analog Signals

Pin Name	PLCC	TQFP	I/O	Description
LINL	18	12	I	Left Channel Line Input
LINR	16	10	I	Right Channel Line Input
MINL	17	11	I	Left Channel Microphone Input (−20 dB from Line Level if MB = 0 or Line Level if MB = 1)
MINR	15	9	I	Right Channel Microphone Input (−20 dB from Line Level if MB = 0 or Line Level if MB = 1)
LOUT0L	32	26	O	Left Channel Line Output 0
LOUT0R	33	27	O	Right Channel Line Output 0
LOUT1L	31	25	O	Left Channel Line Output 1
LOUT1R	29	23	O	Right Channel Line Output 1
LOUT1C	30	24	I	Common Return Path for Large Current from External Headphones
MOUT	27	21	O	Mono Speaker Output
MOUTR	28	22	I	Mono Speaker Output Return
C0	14	8	O	External 1.0 μF Capacitor (±10%) Connection
C1	20	14	O	External 1.0 μF Capacitor (±10%) Connection
N/C	26	20		No Connect (Do Not Connect)
N/C	34	28		No Connect (Do Not Connect)
V_{REF}	21	15	O	Voltage Reference (Connect to Bypass Capacitor)
CMOUT	19	13	O	Common Mode Reference Datum Output (Nominally 2.25 V)

Power Supplies

Pin Name	PLCC	TQFP	I/O	Description
V_{CC}	23 & 24	17, 18	I	Analog Supply Voltage (+5 V)
GNDA	22 & 25	16, 19	I	Analog Ground
V_{DD}	3, 8, 38	41, 2, 32	I	Digital Supply Voltage (+5 V)
GNDD	2, 9, 39	40, 3, 33	I	Digital Ground

FUNCTIONAL DESCRIPTION

This section overviews the functionality of the AD1849K and is intended as a general introduction to the capabilities of the device. As much as possible, detailed reference information has been placed in "Control Registers" and other sections. The user is not expected to refer repeatedly to this section.

Analog Inputs

The AD1849K SoundPort Stereo Codec accepts stereo line-level and mic-level inputs. These analog stereo signals are multiplexed to the internal programmable gain amplifier (PGA) stage. The mic inputs can be amplified by +20 dB prior to the PGA to compensate for the voltage swing difference between line levels and typical condenser microphones. The mic inputs can bypass the +20 dB fixed gain block and go straight to the input multiplexer, which often results in an improved system signal-to-noise ratio.

The PGA following the input multiplexer allows independent selectable gains for each channel from 0 to 22.5 dB in +1.5 dB steps. The Codec can operate either in a global stereo mode or in a global mono mode with left-channel inputs appearing at both channel outputs.

Analog-to-Digital Datapath

The AD1849K ΣΔ ADCs incorporate a proprietary fourth-order modulator. A single pole of passive filtering is all that is required for anti-aliasing the analog input because of the ADC's high 64 times oversampling ratio. The ADCs include linear-phase digital decimation filters that low-pass filter the input to $0.45 \times F_S$ ("F_S" is the word rate or "sampling frequency"). ADC input overrange conditions will cause a sticky bit to be set that can be read.

Digital-to-Analog Datapath

The ΣΔ DACs are preceded by a programmable attenuator and a low-pass digital interpolation filter. The attenuator allows independent control of each DAC channel from 0 dB to −94.5 dB in 1.5 dB steps plus full digital mute. The anti-imaging interpolation filter oversamples by 64 and digitally filters the higher frequency images. The DACs' ΣΔ noise shapers also oversample by 64 and convert the signal to a single-bit stream. The DAC outputs are then filtered in the analog domain by a combination of switched-capacitor and continuous-time filters. They remove the very high frequency components of the DAC bitstream output, including both images at the oversampling rate and shaped quantization noise. No external components are required. Phase linearity at the analog output is achieved by internally compensating for the group delay variation of the analog output filters.

Attenuation settings are specified by control bits in the data stream. Changes in DAC output level take effect only on zero crossings of the digital signal, thereby eliminating "zipper" noise. Each channel has its own independent zero-crossing detector and attenuator change control circuitry. A timer guarantees that requested volume changes will occur even in the absence of an input signal that changes sign. The time-out period is 10.7 milliseconds at a 48 kHz sampling rate and 64 milliseconds at an 8 kHz sampling rate (Time-out [ms] ≈ 512/Sampling Rate [kHz]).

Monitor Mix

A monitor mix is supported that digitally mixes a portion of the digitized analog input with the analog output (prior to digitization). The digital output from the ADCs going out of the serial data port is unaffected by the monitor mix. Along the monitor mix datapath, the 16-bit linear output from the ADCs is attenuated by an amount specified with control bits. Both channels of the monitor data are attenuated by the same amount. (Note that internally the AD1849K always works with 16-bit PCM linear data, digital mixing included; format conversions take place at the input and output.)

Sixteen steps of –6 dB attenuation are supported to –94.5 dB. A "0" implies no attenuation, while a "14" implies 84 dB of attenuation. Specifying full scale "15" completely mutes the monitor datapath, preventing any mixing of the analog input with the digital input. Note that the level of the mixed output signal is also a function of the input PGA settings since they affect the ADCs' output.

The attenuated monitor data is digitally summed with the DAC input data prior to the DACs' datapath attenuators. Because both stereo signals are mixed before the output attenuators, mix data is attenuated a second time by the DACs' datapath attenuators. The digital sum of digital mix data and DAC input data is clipped at plus or minus full scale and does not wrap around.

Analog Outputs

One stereo line-level output, one stereo headphone output, and one monaural (mono) speaker output are available at external pins. Each of these outputs can be independently muted. Muting either the line-level stereo output or the headphone stereo output mutes both left and right channels of that output. When muted, the outputs will settle to a dc value near CMOUT, the midscale reference voltage. The mono speaker output is differential. The chip can operate either in a global stereo mode or in a global mono mode with left channel inputs appearing at both outputs.

Digital Data Types

The AD1849K supports four global data types: 16-bit twos-complement linear PCM, 8-bit unsigned linear PCM, 8-bit companded μ-law, and 8-bit companded A-law, as specified by control register bits. Data in all four formats is always transferred MSB first. Sixteen-bit linear data output from the ADCs and input to the DACs is in twos-complement format. Eight-bit data is always left-justified in 16-bit fields; in other words, the MSBs of all data types are always aligned; in yet other words, full-scale representations in all three formats correspond to equivalent full-scale signals. The eight least-significant bit positions of 8-bit linear and companded data in 16-bit fields are ignored on input and zeroed on output.

The 16-bit PCM data format is capable of representing 96 dB of dynamic range. Eight-bit PCM can represent 48 dB of dynamic range. Companded μ-law and A-law data formats use nonlinear coding with less precision for large-amplitude signals. The loss of precision is compensated for by an increase in dynamic range to 64 dB and 72 dB, respectively.

On input, 8-bit companded data is expanded to an internal linear representation, according to whether μ-law or A-law was specified in the Codec's internal registers. Note that when μ-law compressed data is expanded to a linear format, it requires 14 bits. A-law data expanded requires 13 bits, see Figure 1.

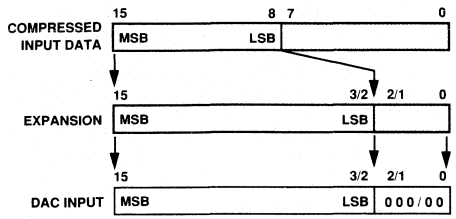


Figure 1. A-Law or μ-Law Expansion

When 8-bit companding is specified, the ADCs' linear output is compressed to the format specified prior to output. See Figure 2.

Note that all format conversions take place at input or output. Internally, the AD1849K always uses 16-bit linear PCM representations to maintain maximum precision.

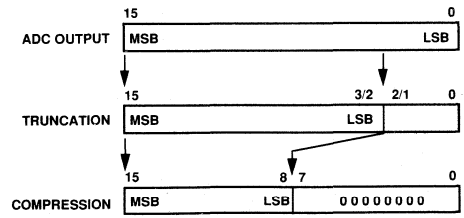


Figure 2. A-Law or μ-Law Compression

Power Supplies and Voltage Reference

The AD1849K operates from +5 V power supplies. Independent analog and digital supplies are recommended for optimal performance, though excellent results can be obtained in single-supply systems. A voltage reference is included on the Codec and its 2.25 V buffered output is available on an external pin (CMOUT). The CMOUT output can be used for biasing op amps used in dc coupling. The internal reference is externally bypassed to analog ground at the V_{REF} pin. Note that V_{REF} should only be connected to its bypass capacitors.

Autocalibration

The AD1849K supports an autocalibration sequence to eliminate DAC and ADC offsets. The autocalibration sequence is initiated in the transition from Control Mode to Data Mode, regardless of the state of the AC bit. The user should specify that analog outputs be muted to prevent undesired outputs. Monitor mix will be automatically disabled by the Codec.

During the autocalibration sequence, the serial data output from the ADCs is meaningless and the ADI bit is asserted. Serial data inputs to the DACs are ignored. Even if the user specified the muting of all analog outputs, near the end of the autocalibration sequence, dc analog outputs very close to CMOUT will be produced at the line outputs and mono speaker output.

An autocalibration sequence is also performed when the AD1849K leaves the reset state (i.e., $\overline{\text{RESET}}$ goes HI). The $\overline{\text{RESET}}$ pin should be held LO for 50 ms after power up or after leaving power-down mode to delay the onset of the autocalibration sequence until after the voltage reference has settled.

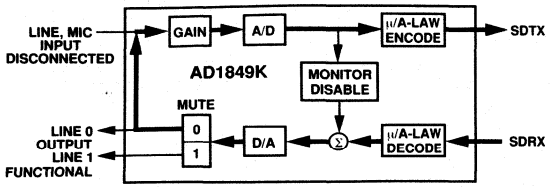
Loopback

Digital and analog loopback modes are supported for device and system testing. The monitor mix datapath is always available for loopback test purposes. Additional loopback tests are enabled by setting the ENL bit (Control Word Bit 33) to a "1."

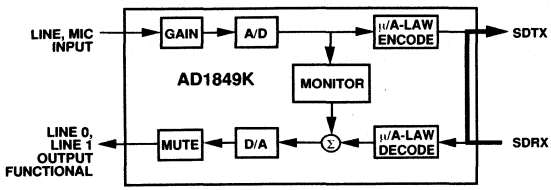
Analog loopback mode D-A-D is enabled by setting the ADL bit (Control Word Bit 32) to a "1" when ENL is a "1." In this mode, the DACs' analog outputs are re-input to the PGAs prior to the ADCs, allowing digital inputs to be compared to digital outputs. The monitor mix will be automatically disabled by the Codec during D-A-D loopback. The analog outputs can be individually attenuated, and the analog inputs are internally disconnected. Note that muting the line 0 output mutes the looped-back signal in this mode.

Digital loopback mode D-D is enabled by resetting the ADL bit (Control Word Bit 32) to a "0" when ENL is a "1." In this mode, the control and data bit pattern presented on the SDRX pin is echoed on the SDTX pin with a two frame delay, allowing the host controller to verify the integrity of the serial interface starting on the third frame after D-D loopback is enabled. During digital loopback mode, the output DACs are operational.

The loopback modes are shown graphically in Figure 3.



AD1849K Analog Loopback D-A-D



AD1849K Digital Loopback D-D

Figure 3. AD1849K Loopback Modes

Clocks and Sample Rates

The AD1849K can operate from external crystals, from a 256 × F_S input clock, from an input clock with a programmable divide factor, or from the serial port's bit clock (at 256 × F_S), selected under software control. Two crystal inputs are provided to generate a wide range of sample rates. The oscillators for these crystals are on the AD1849K, as is a multiplexer for selecting between them. They can be overdriven with external clocks by the user, if so desired. The recommended crystal frequencies are 16.9344 MHz and 24.576 MHz. From them the following sample rates can be internally generated: 5.5125, 6.615, 8, 9.6, 11.025, 16, 18.9, 22.05, 27.42857, 32, 33.075, 37.8, 44.1, 48 kHz. Regardless of clock input source, a clock output of 256 × F_S is generated (with some skew). If an external input clock or the serial port's bit clocks are selected to drive the AD1849K's internal operation, they should be low jitter clocks. If no external clock will be used, Analog Devices recommends tying the clock input pin (CLKIN) to ground. If either external crystal is not used, Analog Devices recommends tying its input (CIN1 and/or CIN2) to ground.

CONTROL REGISTERS

The AD1849K SoundPort Stereo Codec accepts control information through its serial port when in Control Mode. Some control information is also embedded in the data stream when in Data Mode. (See Figure 8.) Control bits can also be read back for system verification. Operation of the AD1849K is determined by the state of these control bits. The 64-bit serial Control Mode and Data Mode control registers have been arbitrarily broken down into bytes for ease of description. All control bits initialize to default states after $\overline{\text{RESET}}$ or Power Down. Those control bits that cannot be changed in Control Mode are initialized to defaults on the transition from Data Mode to Control Mode. See below for a definition of these defaults.

Control Mode Control Registers

Control Byte 1, Status Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	1	MB	OLB	DCB	0	AC
63	62	61	60	59	58	57	56

MB Mic bypass:
- 0 Mic inputs applied to +20 dB fixed gain block.
- 1 Mic inputs bypass +20 dB fixed gain block.

OLB Output level bit:
- 0 Full-scale line 0 output is 2.8 V p-p (1 V rms).
  Full-scale line 1 output is 4.0 V p-p.
  Full-scale mono speaker output is 8.0 V p-p.
- 1 Full-scale line 0 output is 2.0 V p-p.
  Full-scale line 1 output is 2.0 V p-p.
  Full-scale mono speaker output is 4.0 V p-p.

DCB Data/control bit. Used for handshaking in data/control transitions. See "DCB Handshake Protocol."

AC Autocalibration.

Autocalibration will always occur on the Control-to-Data mode transition. The AC bit is ignored. Autocalibration requires an interval of 194 frames. Offsets for all channels of ADC and DAC are zeroed. The user should specify that analog outputs are muted to prevent undesired outputs, i.e., OM0="0," OM1="0," and SM="0." Monitor mix will be automatically disabled by the Codec.

Control Byte 2, Data Format Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	DFR2	DFR1	DFR0	ST	DF1	DF0
55	54	53	52	51	50	49	48

DFR2:0 Data conversion frequency (F_S) select (in kHz):

DFR	Divide Factor	XTAL1 (24.576 MHz)	XTAL2 (16.9344 MHz)
0	3072	8	5.5125
1	1536	16	11.025
2	896	27.42857	18.9
3	768	32	22.05
4	448	N/A	37.8
5	384	N/A	44.1
6	512	48	33.075
7	2560	9.6	6.615

Note that the AD1849K's internal oscillators can be overdriven by external clock sources at the crystal input pins. If an external clock source is used, it should be applied to the crystal input pin (CIN1 or CIN2), and the crystal output pin (COUT1 or COUT2) should be left unconnected. The external clock source need not be at the recommended crystal frequencies, and it will be divided down by the selected Divide Factor.

ST Global stereo mode. Both converters are placed in the same mode.
- 0 Mono mode. The left analog input appears at both ADC outputs. The left digital input appears at both DAC outputs
- 1 Stereo mode

DF1:0 Codec data format selection:
- 0 16-bit twos-complement PCM linear
- 1 8-bit μ-law companded
- 2 8-bit A-law companded
- 3 8-bit unsigned PCM linear

Control Byte 3, Serial Port Control Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
ITS	MCK2	MCK1	MCK0	FSEL1	FSEL0	MS	TXDIS
47	46	45	44	43	42	41	40

ITS Immediate three-state:
- 0 FSYNC, SDTX and SCLK three-state within 3 SCLK cycles after D/$\overline{C}$ goes LO
- 1 FSYNC, SDTX and SCLK three-state immediately after D/$\overline{C}$ goes LO

MCK2:0 Clock source select for Codec internal operation:
- 0 Serial bit clock (SCLK) is the master clock at 256 × F_S
- 1 24.576 MHz crystal (XTAL1) is the clock source
- 2 16.9344 MHz crystal (XTAL2) is the clock source
- 3 External clock (CLKIN) is the clock source at 256 × F_S
- 4 External clock (CLKIN) is the clock source, divided by the factor selected by DFR2:0 (External clock must be stable and valid within 2000 periods after it is selected.)

FSEL1:0 Frame size select:
- 0 64 bits per frame
- 1 128 bits per frame
- 2 256 bits per frame
- 3 Reserved

Note that FSEL is overridden in Data Mode when SCLK is the clock source (MCK = "0"). When SCLK is providing the 256 × F_S clock for internal Codec operation, 256 bits per frame is effectively selected, regardless of FSEL's contents.

MS Master/slave mode for the serial interface:
- 0 Receive serial clock (SCLK) and TSIN from an external device ("slave mode")
- 1 Transmit serial clock (SCLK) and frame sync (FSYNC) to external devices ("master mode")

Note that MS is overridden when SCLK is the clock source (MCK = "0"). When SCLK is providing the clock for internal Codec operation, slave mode is effectively selected, regardless of the contents of MS.

TXDIS Transmitter disable:
- 0 Enable serial output
- 1 Three-state serial data output (high impedance)

Note that Control Mode overrides TXDIS. In Control Mode, the serial output is always enabled.

Control Byte 4, Test Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	ENL	ADL
39	38	37	36	35	34	33	32

ENL Enable loopback testing:
- 0 Disabled
- 1 Enabled

ADL Loopback mode:
- 0 Digital loopback from Data/Control receive to Data/Control transmit (D-D)
- 1 Analog loopback from DACs to ADCs (D-A-D)

Control Byte 5, Parallel Port Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
PIO1	PIO0	0	0	0	0	0	0
31	30	29	28	27	26	25	24

PIO1:0 Parallel I/O bits for system signaling. PIO bits do not affect Codec operation.

Control Byte 6, Reserved Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	0	0
23	22	21	20	19	18	17	16

Reserved bits should be written as 0.

Control Byte 7, Revision Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	1	0	REVID3	REVID2	REVID1	REVID0
15	14	13	12	11	10	9	8

REVID3:0 Silicon revision identification. Reads greater than or equal to 0010 (i.e., 0010, 0011, etc.) for the AD1849K.

Control Byte 8, Reserved Register

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0

Reserved bits should be written as 0.

Data Mode Data and Control Registers

Data Byte 1, Left Audio Data—Most Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
L15	L14	L13	L12	L11	L10	L9	L8
63	62	61	60	59	58	57	56

In 16-bit linear PCM mode, this byte contains the upper eight bits of the left audio data sample. In the 8-bit companded and linear modes, this byte contains the left audio data sample. In mono mode, only the left audio data is used. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 2, Left Audio Data—Least Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
L7	L6	L5	L4	L3	L2	L1	L0
55	54	53	52	51	50	49	48

In 16-bit linear PCM mode, this byte contains the lower eight bits of the left audio data sample. In the 8-bit companded and linear modes, this byte is ignored on input, zeroed on output. In mono mode, only the left audio data is used. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 3, Right Audio Data—Most Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
R15	R14	R13	R12	R11	R10	R9	R8
47	46	45	44	43	42	41	40

In 16-bit linear PCM mode, this byte contains the upper eight bits of the right audio data sample. In the 8-bit companded and linear modes, this byte contains the right audio data sample. In mono mode, this byte is ignored on input, zeroed on output. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 4, Right Audio Data—Least Significant 8 Bits

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
R7	R6	R5	R4	R3	R2	R1	R0
39	38	37	36	35	34	33	32

In 16-bit linear PCM mode, this byte contains the lower eight bits of the right audio data sample. In the 8-bit companded and linear modes, this byte is not used. In mono mode, this byte is ignored on input, zeroed on output. MSB first format is used in all modes, and twos-complement coding is used in 16-bit linear PCM mode.

Data Byte 5, Output Setting Register 1

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
OM1	OM0	LO5	LO4	LO3	LO2	LO1	LO0
31	30	29	28	27	26	25	24

OM1 Output Line 1 Analog Mute:
- 0 Mute Line 1
- 1 Line 1 on

OM0 Output Line 0 Analog Mute:
- 0 Mute Line 0
- 1 Line 0 on

LO5:0 Output attenuation setting for the left DAC channel; "0" represents no attenuation. Step size is 1.5 dB; "62" represents 93 dB of attenuation. Attenuation = 1.5 dB × LO, except for LO = "63," which represents full digital mute.

Data Byte 6, Output Setting Register 2

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
ADI	SM	RO5	RO4	RO3	RO2	RO1	RO0
23	22	21	20	19	18	17	16

ADI — ADC Invalid. This bit is set to "1" during the autocalibration sequence, indicating that the serial data output from the ADCs is meaningless.

SM — Mono Speaker Analog Mute:
- 0 Mute mono speaker
- 1 Mono speaker on

RO5:0 — Output attenuation setting for the right DAC channel; "0" represents no attenuation. Step size is 1.5 dB; "62" represents 93 dB of attenuation. Attenuation = 1.5 dB × RO, except for RO = "63," which represents full digital mute.

Data Byte 7, Input Setting Register 1

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
PIO1	PIO0	OVR	IS	LG3	LG2	LG1	LG0
15	14	13	12	11	10	9	8

PIO1:0 — Parallel I/O bits for system signaling. PIO bits do not affect Codec operation.

OVR — ADC input overrange. This bit is set to "1" if either ADC channel is driven beyond the specified input range. It is "sticky," i.e., it remains set until explicitly cleared by writing a "0" to OVR. A "1" written to OVR is ignored, allowing OVR to remain "0" until an overrange condition occurs.

IS — Input selection:
- 0 Line-level stereo inputs
- 1 Microphone (condenser-type) level inputs if MB = 0 (+20 dB gain), or line-level stereo inputs if MB = 1 (0 dB gain).

LG3:0 — Input gain for left channel. "0" represents no gain. Step size is 1.5 dB; "15" represents +22.5 dB of input gain. Gain = 1.5 dB × LG.

Data Byte 8, Input Setting Register 2

Data 7	Data 6	Data 5	Data 4	Data 3	Data 2	Data 1	Data 0
MA3	MA2	MA1	MA0	RG3	RG2	RG1	RG0
7	6	5	4	3	2	1	0

MA3:0 — Monitor mix. "0" represents no attenuation, i.e., the ADCs' output is fully mixed with the DACs' input. Step size is 6 dB; "14" represents an attenuation of both channels of the ADCs' output along the monitor datapath of 84 dB. Mix attenuation = 6 dB × MA, except for MA = "15," which disables monitor mix entirely.

RG3:0 — Input gain for right channel. "0" represents no gain. Step size is 1.5 dB; "15" represents +22.5 dB of input gain. Gain = 1.5 dB × RG.

Control Register Defaults
Upon coming out of $\overline{\text{RESET}}$ or Power Down, internal control registers will be initialized to the following values:

Defaults Coming Out of $\overline{\text{RESET}}$ or Power Down

MB	0	Mic Input Applied to +20 dB Fixed Gain Block
OLB	0	Full-Scale Line 0 Output 2.8 V p-p, Full-Scale Line 1 Output 4.0 V p-p, Full-Scale Mono Speaker Output 8.0 V p-p
DCB	1	Data/Control Bit HI
AC	0	Autocalibration Disabled
DFR2:0	0	8 or 5.5125 kHz
ST	0	Monophonic Mode
DF1:0	1	8-Bit μ-Law Data
ITS	0	FSYNC, SDTX and SCLK Three-State within 3 SCLK Cycles after D/$\overline{\text{C}}$ Goes LO
MCK2:0	0	Serial Bit Clock [SCLK] is the Master Clock
FSEL1:0	2	256 Bits per Frame
MS	0	Slave Mode
TXDIS	1	Three-State Serial Data Output
ENL	0	Loopback Disabled
ADL	0	Digital Loopback
PIO1:0	3	"1"s, i.e., Three-State for the Open Collector Outputs
OM1:0	0	Mute Line 0 and Line 1 Outputs
LO5:0	63	Mute Left DAC
ADI	1	ADC Data Invalid, Autocalibration in Progress
SM	0	Mute Mono Speaker
RO5:0	63	Mute Right DAC
OVR	0	No Overrange
IS	0	Line-Level Stereo Inputs
LG3:0	0	No Gain on Left Channel
MA3:0	15	No Mix
RG3:0	0	No Gain on Right Channel

Also, when making a transition from Control Mode to Data Mode, those control register values that are *not* changeable in Control Mode get reset to the defaults above (except PIO). The control registers that *can* be changed in Control Mode will have the values they were just assigned. The subset of the above list of control registers that are assigned default values on the transition from Control Mode to Data Mode are:

Defaults at a Control-to-Data Mode Transition

OM1:0	0	Mute Line 0 and Line 1
LO5:0	63	Mute Left DAC
SM	0	Mute Mono Speaker
RO5:0	63	Mute Right DAC
OVR	0	No Overrange
IS	0	Line-Level Stereo Inputs
LG3:0	0	No Gain
MA3:0	15	No Mix
RG3:0	0	No Gain

Note that all these defaults can be changed with control information in the first Data Word. Note also that the PIO bits in the output serial streams *always* reflect the values most recently read from the external PIO pins. (See "Parallel I/O Bits" below for timing details.) A Control-to-Data Mode transition is no exception.

An important consequence of these defaults is that *the AD1849K Codec always comes out of reset or power down in slave mode with an externally supplied serial bit clock (SCLK) as the clock source.* An external device *must* supply the serial bit clock and the chaining word input signal (TSIN) initially. (See "Codec Startup, Modes, and Transitions" below for more details.)

ANALOG DEVICES

PSTN Signal Port

AD28msp01

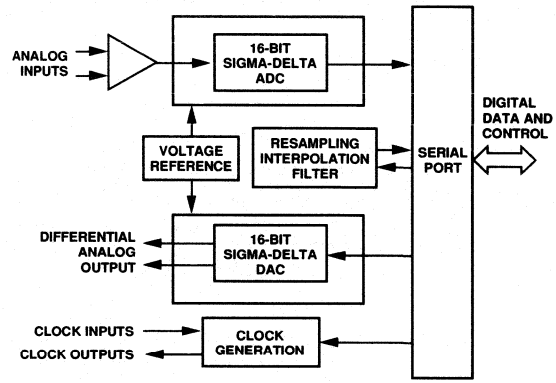
FEATURES

Complete Analog I/O Port for DSP-Based FAX/MODEM Applications
Linear-Coded 16-Bit Sigma-Delta ADC
Linear-Coded 16-Bit Sigma-Delta DAC
On-Chip Anti-Alias and Anti-Image Filters
Digital Resampling/Interpolation Filter
7.2 kHz, 8.0 kHz, and 9.6 kHz Sampling Rates
8/7 Mode for 8.23 kHz, 9.14 kHz, and 10.97 kHz Sampling Rates
Synchronous and Asynchronous DAC/ADC Modes
Bit and Baud Clock Generation
Transmit Digital Phase-Locked Loop for Terminal Synchronization
Independent Transmit and Receive Phase Adjustment
Serial Interface to DSP Processors
+5 V Operation with Power-Down Mode
28-Pin Plastic DIP/44-Lead PLCC/28-Lead SOIC

APPLICATIONS

High Performance DSP-Based Modems
V.32ter, V.32bis, V.32, V.22bis, V.22, V.21, Bell 212A, 103
Fax and Cellular-Compatible Modems
V.33, V.29, V.27ter, V.27bis, V.27, V.26bis
Integrated Fax, Modem, and Speech Processing

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD28msp01 is a complete analog front end for high performance DSP-based modems. The device includes all data conversion, filtering, and clock generation circuitry needed to implement an echo-cancelling modem with a single host digital signal processor. Software-programmable sample rates and clocking modes support all established modem standards. The AD28msp01 simplifies overall system design by requiring only +5 volts.

The inclusion of on-chip anti-aliasing and anti-imaging filters and 16-bit sigma-delta ADC and DAC ensures a highly integrated and compact solution for FAX or data MODEM applications. Sigma-delta conversion technology eliminates the need for complex off-chip anti-aliasing filters and sample-and-hold circuitry.

The AD28msp01 utilizes advanced sigma-delta technology to move the entire echo-cancelling modem implementation into the digital domain. The device maintains a −72 dB SNR throughout all filtering and data conversion. Purely DSP-based echo cancellation algorithms can thereby maintain robust bit error rates under worst-case signal attenuation and echo amplitude conditions. The AD28msp01's on-chip interpolation filter resamples the received signal after echo cancellation in the DSP, freeing the processor for other voice or data communications tasks.

On-chip bit and baud clock generation circuitry provides for either synchronous or asynchronous operation of the transmit (DAC) and receive (ADC) paths. Each path features independent phase advance and retard adjustments via software control. The AD28msp01 can also synchronize modem operation to an external terminal bit clock.

The AD28msp01's serial I/O port provides an easy interface to host DSP microprocessors such as the ADSP-2101, ADSP-2105, and ADSP-2111. Packaged in a 28-pin plastic DIP, 44-lead PLCC, 44-pin TQFP, or 28-lead SOIC, the AD28msp01 provides a compact solution for space-constrained environments. The device operates from a +5 V supply and offers a low power sleep mode for battery-powered systems.

A detailed block diagram of the AD28msp01 is shown in Figure 1.

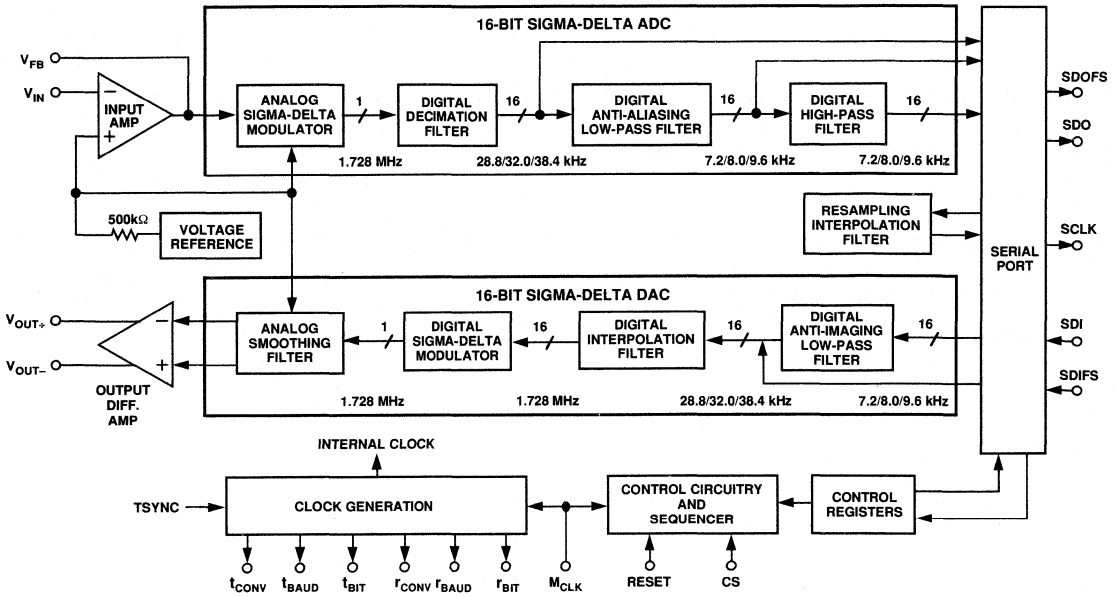


Figure 1. AD28msp01 Block Diagram

PIN DESCRIPTIONS

Name	Type	Description
Analog Interface		
V_{IN}	I	Analog input to the inverting terminal of the input amplifier.
V_{FB}	O	Feedback terminal of the input amplifier.
V_{OUTP}	O	Analog output from the noninverting terminal of the output differential amplifier.
V_{OUTN}	O	Analog output from inverting terminal of the output differential amplifier.
Serial Interface		
SCLK	O/Z	Serial clock used for clocking data or control bits to/from the serial port (SPORT). The frequency of this clock is 1.7280 MHz. This pin is 3-stated when the CS is low.
SDI	I	Serial data input of the SPORT. Both data and control information are input on this pin. This pin is ignored when CS is low.
SDO	O/Z	Serial data output of the SPORT. Both data and control information are output on this pin. This pin is 3-stated when CS is low.
SDIFS	I	Framing synchronization signal for serial data transfers to the AD28msp01 (via the SDI pin). This pin is ignored when CS is low.
SDOFS	O/Z	Framing synchronization signal for serial data transfers from the AD28msp01 (via the SDO pin). This pin is 3-stated when CS is low.
Clock Generation		
TSYNC	I	Transmit synchronization clock. This signal is used to synchronize the transmit clocks and the converter clocks to an external terminal/ bit-rate clock. It is used in the V.32 TSYNC and Asynchronous TSYNC modes and is ignored in other operating modes. The frequency of the external clock must be programmed in Control Register 0. This pin must be tied high or low if it is not being used.
TBIT	O	Transmit bit rate clock. This is an output clock whose frequency is programmable via Control Register 3. It is synchronized with the TCONV clock.
TBAUD	O	Transmit baud rate clock. This is an output clock whose frequency is programmable via Control Register 3. It is synchronized with the TCONV clock.

PIN DESCRIPTIONS (Continued)

Name	Type	Description
TCONV	O	Transmit conversion clock. This clock indicates when the ADC has finished a sampling cycle. The frequency of TCONV is programmed by setting the sample rate field in Control Register 0. The programmed TCONV rate can be scaled by a factor of 8/7 by setting bit 9 in Control Register 1. The phase of TCONV can be adjusted by writing the Transmit Phase Adjust Register (Control Register 5).
RBIT	O	Receive bit rate clock. This is an output clock whose frequency is programmable via Control Register 2. It is synchronized with the RCONV clock.
RBAUD	O	Receive baud rate clock. This is an output clock whose frequency is programmable via Control Register 2. It is synchronized with the RCONV clock.
RCONV	O	Receive conversion clock. This clock indicates when the DAC has finished a sampling cycle. The frequency of RCONV is programmed by setting the sample rate field in Control Register 0. The programmed RCONV rate can be scaled by a factor of 8/7 by setting Bit 9 in Control Register 1. The phase of RCONV can be adjusted by writing the Receive Phase Adjust Register (Control Register 4).
Miscellaneous		
MCLK	I	AD28msp01 master clock input. The frequency of this clock must be 13.824 MHz to guarantee listed specifications.
$\overline{\text{RESET}}$	I	Active-low chip reset. This signal sets all AD28msp01 control registers to their default values and clears the device's digital filters. SPORT output pins are 3-stated when $\overline{\text{RESET}}$ is low. SPORT input pins are ignored when $\overline{\text{RESET}}$ is low.
CS	I	Active-high chip select. This signal 3-states all SPORT output pins and forces the AD28msp01 to ignore all SPORT input pins. If CS is deasserted during a serial data transfer, the 16-bit word being transmitted is lost.
Power Supplies		
V_{CC}		Analog supply voltage (nominally +5 V)
GND_A		Analog ground
V_{DD}		Digital supply voltage (nominally +5 V)
GND_D		Digital ground

FUNCTIONAL DESCRIPTION

A/D Conversion

The A/D conversion circuitry of the AD28msp01 consists of an analog input amplifier and a sigma-delta analog-to-digital converter (ADC). The analog input signal to the AD28msp01 must be ac coupled.

Analog Input Amplifier

The analog input amplifier is internally biased by an on-chip voltage reference in order to allow operation of the AD28msp01 with a +5 V power supply.

Input signal level to the sigma-delta modulator should not exceed V_{INMAX}, which is specified under "Analog Interface Electrical Characteristics." Refer to "Analog Input" in the "Design Considerations" section of this data sheet for more information.

ADC

The ADC consists of a 3rd-order analog sigma-delta modulator, a decimation filter, an anti-aliasing low-pass filter, and a high-pass filter. The analog input is applied to the input amplifier. The output of this amplifier is applied to an analog sigma-delta modulator which noise-shapes it and produces 1-bit samples at a 1.7280 MHz rate. This bit stream is fed to the decimation filter, which increases the resolution to 16-bits and decreases the sampling frequency. The parallel data stream is then processed by the anti-aliasing low-pass filter which further reduces the sampling rate. Finally, the high-pass filter removes input frequency components at the low end of the spectrum.

Either the high-pass filter alone or the high-pass/anti-aliasing low-pass filter combination can be bypassed by setting the appropriate bits in Control Register 1, thus producing samples at 7.2/8.0/9.6 kHz or 28.8/32.0/38.4 kHz, respectively. The gain and the frequency response of the AD28msp01 are altered when these filters are bypassed. The DSP processor that receives samples from the AD28msp01 may need to compensate for this change.

Decimation Filter

The decimation filter is a sinc^4 digital filter that increases resolution to 16 bits and reduces the sample rate to 28.8, 32.0, or 38.4 kHz (depending on the input sample rate). The 16 bit, parallel data stream output of the decimation filter is then processed by the anti-aliasing low-pass filter.

Anti-Aliasing Low-Pass Filter

The anti-aliasing low-pass filter further reduces the sampling rate by a factor of four to 7.2, 8.0, or 9.6 kHz (depending on the output sample rate of the decimation filter). The output is fed to the high-pass filter. The low-pass/high-pass filter combination can be bypassed by setting the appropriate bits in Control Register 1. If the filters are bypassed, the signal must be scaled by the following multipliers to achieve normal levels: 2.046 for 9.6 kHz, 0.987 for 8.0 kHz, and 0.647 for 7.2 kHz.

When the filters are bypassed, the host DSP must be able to receive data at the 28.8/32.0/38.4 kHz rates. In this case, resampling interpolation should be disabled because of insufficient bandwidth to transmit both ADC and resampled data to the SPORT.

High-Pass Filter

The digital high pass filter removes frequency components at the low end of the spectrum. The high pass filter can be bypassed by setting the appropriate bits in Control Register 1.

The output of the ADC is transferred to the AD28msp01's serial port (SPORT) for transmission to the host DSP processor.

D/A CONVERSION

The D/A conversion circuitry of the AD28msp01 consists of a sigma-delta digital-to-analog converter (DAC) and a differential output amplifier.

DAC

The DAC consists of an anti-imaging low-pass filter, an interpolation filter, a digital sigma-delta modulator, and an analog smoothing filter. These filters have the same characteristics as the ADC's anti-aliasing filter and decimation filter.

The DAC receives 16-bit samples from the host DSP processor via AD28msp01's SPORT. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered first by the DAC's anti-imaging low-pass filter and then by the interpolation filter. The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples. The output of the sigma-delta modulator is fed to the AD28msp01's analog smoothing filter where it is converted into a low-pass filtered, analog voltage.

Anti-Imaging Low-Pass Filter

The anti-imaging low-pass filter filters the 7.2, 8.0, or 9.6 kHz data stream form the SPORTs, and raises the sampling rate to 28.8, 32.0, or 38.4 kHz.

The anti-imaging low-pass filter can be bypassed by setting the appropriate bit in Control Register 1. This results in a gain change. If the filter is bypassed, the signal must be scaled by the following multipliers to achieve normal levels: 2.046 for 9.6 kHz, 0.987 for 8.0 kHz, and 0.647 for 7.2 kHz.

When the filter is bypassed, the host DSP must be able to transmit data at the 28.8/32.0/38.4 kHz rates. In this case, resampling interpolation should be disabled because of insufficient bandwidth to transmit both ADC and resampled data to the SPORT.

Interpolation Filter

The interpolation filter contains is a sinc^4 digital filter which raises the sampling rate to 1.7280 MHz by interpolating between the samples. These 16-bit samples are then processed by the digital sigma-delta modulator which noise-shapes the data stream and reduces the sample width to a single bit stream.

Analog Smoothing Filter

The AD28msp01's analog smoothing filter consists of a 2nd-order Sallen-Key continuous-time filter and a 3rd-order switched capacitor filter. The Sallen-Key filter has a 3 dB point at approximately 80 kHz.

The analog smoothing filter converts the 1.7280 MHz bit stream output of the sigma-delta modulator into a low-pass filtered, differential analog signal.

Differential Output Amplifier

The differential output amplifier produces the AD28msp01's analog output (V_{OUTP}, V_{OUTN}). It can drive loads of 2 kΩ or greater and has a maximum differential output voltage swing of 6.312 V peak-to-peak. The output signal is dc biased to the AD28msp01's on-chip voltage reference (2.5 V nominal) and can be ac coupled directly to a load or dc coupled to an external amplifier. Refer to "Analog Output" in the "Design Considerations" section of this data sheet for more information.

The V_{OUTP} and V_{OUTN} outputs must be used as differential outputs; do not use either as a single-ended output.

SERIAL PORT

The AD28msp01 includes a full-duplex synchronous serial port (SPORT) used to communicate with a host processor. The SPORT is used to read and write all data and control registers in the AD28msp01. The SPORT transfers 16-bit words, MSB first, at a serial clock rate of 1.7280 MHz.

When the AD28msp01 exits reset, both the analog circuitry and the digital circuitry are powered down. The serial port will not transmit data to the host until the host sets the digital power-down bit (PWDD) to 1 in Control Register 1. All control registers should be initialized before this bit is set.

The SPORT is configured for an externally generated receive frame sync (SDIFS), an internally generated serial clock (SCLK), and an internally generated transmit frame sync (SDOFS). The host processor should be configured for an external serial clock and receive frame sync and an internal transmit frame sync.

DSP Processor Interface

The AD28msp01-to-host processor interface is shown in Figure 2.

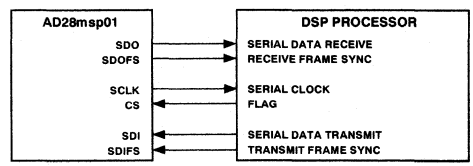


Figure 2. AD28msp01-to-DSP Processor Interface

The AD28msp01's chip select (CS) must be held high to enable SPORT operation. CS can be used to 3-state the SPORT pins and disable communication with the host processor.

To use the ADSP-2101 or ADSP-2111 as host DSP processor for the AD28msp01, refer to Figure 3.

Note that the ADSP-2101's SPORT0 communicates with the AD28msp01's SPORT while the ADSP-2101's Flag Output (FO) is used to signal the AD28msp01's CS input. SPORT1 on the ADSP-2101 must be configured for flags and interrupts in this system.

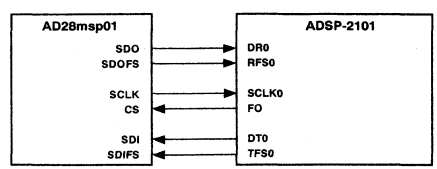


Figure 3. AD28msp01-to-ADSP-2101 Interface

Figure 4 shows an ADSP-2101 assembly language program that initializes the AD28msp01 and implements a digital loopback through the processor.

```
{This ADSP-2101 program initializes the AD28msp01}
{and executes a loopback, or talk-through, routine.}

.MODULE/RAM/BOOT = 0 MSP01;
.VAR/DM/CIRC rec[2];                        {Receive word buffer}
.VAR/DM/CIRC trans[2];                      {Transmit word buffer}
                                            {Interrupt Vectors}
rset:       JUMP start;
            RTI; RTI; RTI;
irq2v:      RTI; RTI; RTI; RTI;
sprt0t:     AX0 = 0x25; DM(0x3ff3) = AX0;   {Disable TX autobuffer}
            RTI; RTI;
sprt0r:     JUMP receive;
            RTI; RTI; RTI;
sprt1t:     RTI; RTI; RTI; RTI;
sprt1r:     RTI; RTI; RTI; RTI;
timerv:     RTI; RTI; RTI; RTI;
                                            {Initialize DAGs}
start:

            I2 = ^rec;
            L2 = %rec;

            I3 = ^trans;
            L3 = %trans;
            M0 = 0;
            M1 = 1;
            SI = 0;
            DM(0x3000) = SI;                {Reset the AD28msp01}
                                            {Initialize the ADSP-2101}
init_dsp:
            AX0 = 0x2a0f;                   {Ext RFS, Int TfS, Ext SCLK, SLEN = 15}
            DM(0x3ff6) = AX0;               {SPORT0 control register}
            AX0 = 0x101f;                   {Enable SPORT0}
            DM(0x3fff) = AX0;               {System control register}
                                            {Initialize AD28msp01 control register}
init_msp01:                                 {Note: This section could be autobuffered.}
            IMASK = 0x10;                   {Enable SPORT0 TX interrupt}
            AR = 0;
            CNTR = 6;
            DO initi UNTIL CE;
                  TX0 = AR;                 {Transmit address}
                  IDLE;
                  TX0 = SI;                 {Transmit control word}
                  IDLE;
                  AY0 = AR;
initi:            AR = AY0 +1;              {Increment address}
            AX1 = 1;
            AR = 0x18;                      {Power up AD28msp01}
            TX0 = AX1;
            IDLE;
            TX0 = AR;
            AR = B#0025;                    {Enable RX autobuffering with I2, M1}
            DM(0x3ff3) = AR;                {Autobuffer control register}
            IMASK = 0x18;                   {Enable RX and TX interrupt}
wait:       JUMP wait;                      {Wait for receive interrupt}
                                            {Receive Interrupt Routine}
receive:
            DM(0x3ff3) = SI;                {Disable autobuffering}
            AX1 = DM(I2, M1);               {Read first receive word from buffer}
```

```
                AX0 = DM(I2, M1);          {Read data word}
                AY0 = 8;                   {Verify AD28msp01 address = 8}
                AR = AX1 - AY0;
                IF EQ JUMP goodstuff;
                RTI;
goodstuff:
                MODIFY (I3, M1);           {Point to second word of TX buffer}
                DM(I3, M0) = AX0;
                MX1 = 6;                   {Load address word into MX1}
                AR = 0x06a7;               {Enable TX and RX autobuffer}
                DM(0x3ff3) = AR;           {Write to SPORT control Register}
                TX0 = MX1;                 {Autobuffer start}
                RTI;
.ENDMOD;
```

Figure 4. AD28msp01 Initialization and ADSP-2101 Loopback Routine

Serial Data Output

When the digital power-down bit ($\overline{\text{PWDD}}$) of Control Register 1 is set to 1, the AD28msp01's SPORT begins transmitting data to the host processor. All transfers between the host processor and the AD28msp01 consist of a serial data output frame sync (SDOFS) followed by a 16-bit address word, then a second frame sync followed by a 16-bit data word. Address/data word pairs are transmitted whenever they become available. The ADC takes precedence over the Interpolator output data. If a new word becomes available while a serial transfer is in progress, the current serial transfer is completed before the new word starts transmission.

Serial Data Input

The host processor must initiate data transfers to the AD28msp01 by asserting the serial data input frame sync (SDIFS) high. Each of the 16-bit address word and 16-bit data word transfers begins one serial clock cycle after SDIFS is asserted. The address word always precedes the data word. The second serial data input frame sync for the data word can be asserted as early as the last bit of the address word is transmitted, or any time after.

The host processor must assert SDIFS shortly after the rising edge of SCLK and must maintain SDIFS high for one cycle because SDIFS is clocked by the SCLK falling edge. Data is then driven from the host processor shortly after the rising edge of the next SCLK and is clocked into the AD28msp01 on the falling edge of SCLK in that cycle. Each bit of a 16-bit address and 16-bit data word is thus clocked into the AD28msp01 on the falling edge of SCLK (MSB first).

If SDIFS is asserted high again before the end of the present data word transfer, it is not recognized until the falling edge of SCLK in the last (LSB) cycle.

When the serial port receives an interpolator or DAC input word, it writes the value to an internal register which is read by the AD28msp01 when it is needed. This allows the host to send data words at any time during the sample period.

NOTE: Exact SPORT timing requirements are defined in the "Specifications" section of this data sheet.

Clock Generation

The AD28msp01 generates all transmit and receive clocks necessary to implement standard voice-grade modems. The AD28msp01 can generate six different clock signals for transmit and receive timing as well as an additional clock signal for serial port timing.

The receive clocks are the RCONV, RBIT and RBAUD signals. The individual clock rates are programmable and are all synchronized with RCONV.

The transmit clocks are the TCONV, TBIT and TBAUD signals. The individual clock rates are programmable and are all synchronized with TCONV.

Depending on the operating mode, the converter clocks can be synchronized to an external clock signal (TSYNC) or can be generated internally. The clocks can be adjusted in phase by setting the appropriate phase adjust register. All the AD28msp01 Bit/Baud clocks have a 50% duty cycle except the 1600 Hz baud rate. This baud rate has a 33%–66% duty cycle.

Resampling Interpolation Filter

The resampling interpolation filter interpolates the data from the TCONV rate to 1.7280 MHz. The data is then resampled (decimated) in phase with the RCONV clock. The frequency response characteristics of the resampling interpolation filter are identical to the frequency response characteristics of the anti-imaging, low-pass filter/interpolation filter combination.

Figure 5 illustrates the effects of a resampling interpolation filter.

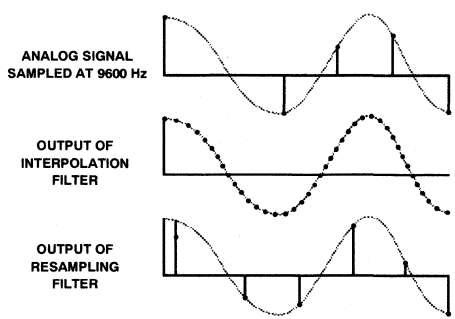


Figure 5. Effects of Interpolation Filter

Since the resample phase is locked to RCONV, it can be advanced or slipped by writing a signed-magnitude value to the Receive Phase Adjust Register (Control Register 2). The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 4.

The change in phase requires a maximum of two RCONV cycles to complete. If the value written to Control Register 4 is less than the oversampling ratio, then the change will complete in one RCONV cycle.

Control Registers

The AD28msp01's six control registers configure the device for various operating modes including filter bypass and power-down. The AD28msp01's host processor can read and write to the control register through the AD28msp01's serial port (SPORT).

The control registers should be set up for the desired mode of operation before bringing the AD28msp01 out of power-down (by writing ones to the $\overline{\text{PWDA}}$ and $\overline{\text{PWDD}}$ bits in Control Register 1).

The control registers are cleared (set to 0x0000) when the AD28msp01 is reset.

The sampling rate should be set before writing ones to the power-down bits. Changing the sampling rate at any other time will force a soft reset. For more information about soft resets, refer to the end of this section of the data sheet.

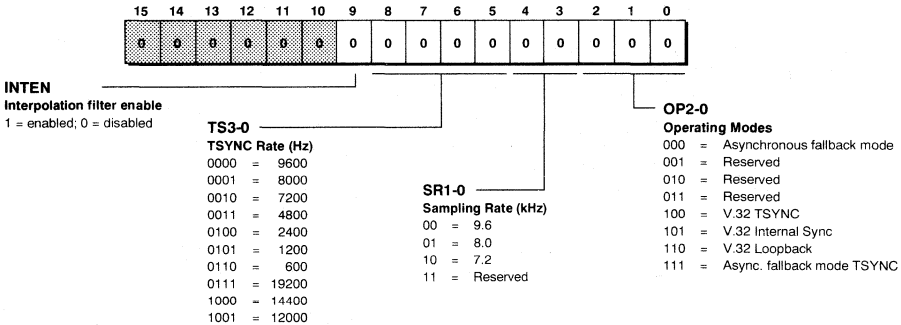
NOTE: Reserved bits should always be cleared to 0.

3

Control Register 0 address = 0x00

This register is used to:

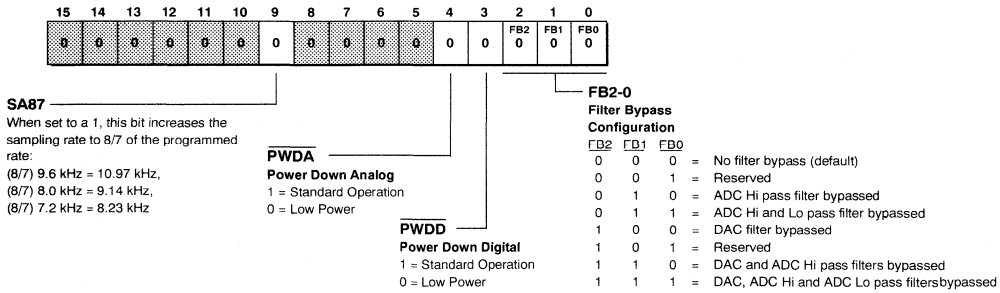
- Enable/disable the resampling interpolation filter
- Set the external TSYNC clock rate
- Select the sampling rate
- Select the operating mode



Control Register 1 address = 0x01

This register is used to:

- Increase the sampling rate to 8/7 the rate selected in Control Register 0
- Power down the device
- Bypass the digital filters

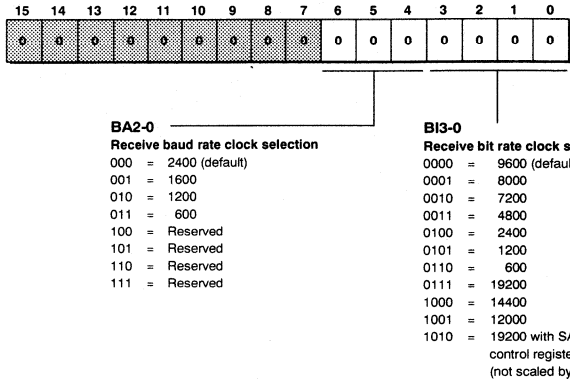


If any low-pass filter is bypassed, the resampling interpolation filter should be disabled (in Control Register 0.)

Control Register 2 address = 0x02

This register is used to:

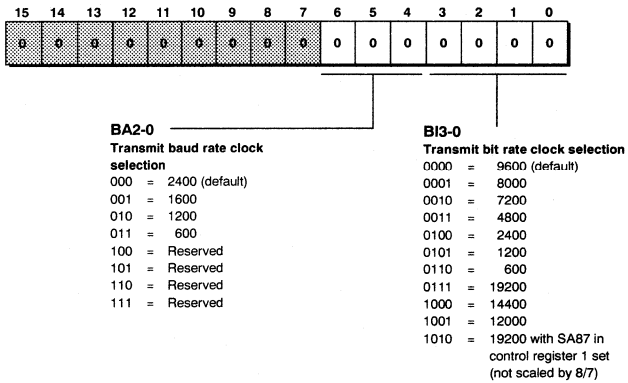
- Select the frequency of the Receive baud clock (RBAUD)
- Select the frequency of the Receive bit clock (RBIT)



Control Register 3 address = 0x03

This register is used to:

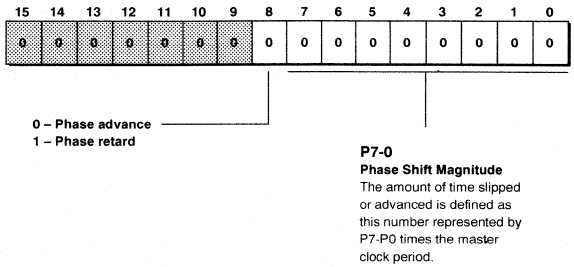
- Select the frequency of the Transmit baud clock (TBAUD)
- Select the frequency of the Transmit bit clock (TBIT)



Control Register 4 address = 0x04

This register is the *Receive Phase Adjust Register* and it is used to:

- Change the phase of the receive clocks (RBAUD, RBIT, RCONV)



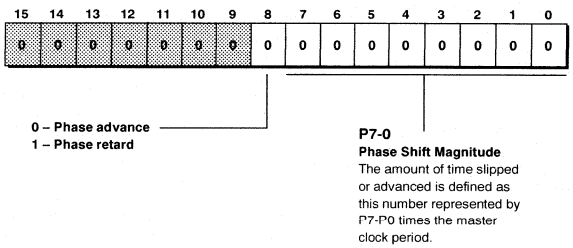
Once you have written a value to the register, subsequent writes are ignored until the register is finished incrementing/decrementing to zero.

The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 4. The AD28msp01 decrements Control Register 4 as it adjusts the phase of RCONV. Control Register 4 will equal zero when the phase shift is complete.

Control Register 5 address = 0x05

This register is the *Transmit Phase Adjust Register* and it is used to:

- Change the phase of the Transmit clocks (TBAUD, TBIT, TCONV)



This register must be equal to zero before its value can be changed. Once you have written a value to the register, subsequent writes are ignored until the register is finished incrementing/decrementing to zero.

The phase advance or slip is equal to the master clock period (13.824 MHz) multiplied by the signed-magnitude 9-bit value in Control Register 5. The AD28msp01 decrements Control Register 5 as it adjusts the phase of TCONV. Control Register 5 will equal zero when the phase shift is complete.

Soft Resets

Certain conditions cause the AD28msp01 to perform a *soft reset*; the DSP is reset but the control register values do not change.

Table I shows when a soft reset is caused by changing the values of certain control register bits while the device is operating. When these bits are modified, the AD28msp01 will perform a soft reset and start up again in the new configuration. Reserved bits in the control registers should always be set to zero.

Table I. Soft Reset

Bits	Configures
Control Register 0, SR1–SR0	Sampling rate
Control Register 0, OP2–OP0	Clock generation operating modes (async-to-V.32 or V.32-to-async)
Control Register 0, TS3–TS0	TSYNC rate
Control Register 1, FB2–FB0	Filter bypass configuration
Control Register 1, SA87	Sampling rate scaling by 8/7

Data Registers

The AD28msp01 contains four data registers.

Data Register 0 address = 0x06

DAC Input Register (write-only): The 16-bit twos complement values written to this register are input to the AD28msp01's digital-to-analog converter.

Data Register 1 address = 0x07

Interpolation Filter Input Register (write-only): The 16-bit twos complement values written to this register are input to the resampling interpolation filter.

Data Register 2 address = 0x08

ADC Output Register (read-only): The 16-bit twos complement values read from this register are the output of the AD28msp01's analog-to-digital converter.

Data Register 3 address = 0x09

Interpolation Filter Output Register (read-only): The 16-bit twos complement values read from this register are the output of the resampling interpolation filter.

Addresses 0x0A – 0x1F are reserved.

Table II contains the register addresses.

Table II. Register Addresses

Address Bits 4–0	Register	Description
00000	Control Register 0	Data rate and synchronization rate selects, interpolation filter enable
00001	Control Register 1	Filter bypass, test, power-down mode bits, V.32ter mode select bits
00010	Control Register 2	ADC bit and baud rate selects
00011	Control Register 3	DAC bit and baud rate selects
00100	Control Register 4	Receive phase adjust
00101	Control Register 5	Transmit phase adjust
00110	Data Register 0	DAC input register
00111	Data Register 1	Interpolation filter input register
01000	Data Register 2	ADC output register
01001	Data Register 3	Interpolation filter output register
01010	Reserved	
. . . .	. . . . .	
. . . .	. . . . .	
11111	Reserved	

Transferring Data and Control Words to the AD28msp01

Data and control word transfers to the AD28msp01 can only be initiated by the host processor. When transferring data to the AD28msp01, the host processor specifies the destination register by first transmitting a 16-bit address word (Figure 6) and then transmitting the 16-bit data word. The read/write bit in the address word must be deasserted. The serial data stream from the host processor will consist of a sequence of alternating address and data words. The AD28msp01 will not write the target register until both the address word and data word are completely transferred.

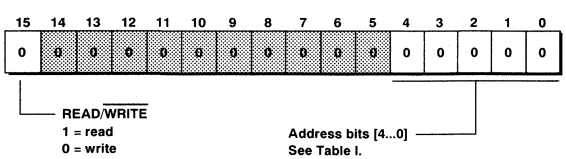


Figure 6. Address Word

Example

Transferring the following 16-bit words to the AD28msp01 will initialize Control Registers 0–3.

Word Transferred	Description
0x0000	Control Register 0 Address Word
0x0254	Write this value to Control Register 0
0x0002	Control Register 2 Address Word
0x0031	Write this value to Control Register 2
0x0003	Control Register 3 Address Word
0x0032	Write this value to Control Register 3
0x0001	Control Register 1 Address Word
0x0018	Write this value to Control Register 1

Note that in this example the power-down bits in Control Register 1 are released (set to 1) only after the AD28msp01 is fully configured by writing to Control Registers 0, 2, and 3.

Transferring Data from the AD28msp01 to the Host

Data transfers to the host processor can only be initiated by the AD28msp01. When transferring data the AD28msp01 first specifies the source register by transferring a 16-bit address word and then transfers the contents of the source register. Bits 5–14 of the address word will always be forced to zero. When transferring data, the serial data stream from the AD28msp01 will consist of a sequence of alternating address and data words.

Transferring Control Words from the AD28msp01 to the Host

All control registers in the AD28msp01 are host-readable. To read a control register, the host must transmit a 16-bit address word with the Read/Write bit set, then transmit a dummy data word. The AD28msp01 will respond by first completing any AD28msp01-to-Host transfer in progress. As soon as the dummy data word is received, the device will transfer a 16-bit word with the control register address and then transmit the contents of the control register.

Example

The following data streams show how a host can read the contents of an AD28msp01 control register:

Host Transfer	AD28msp01 Transfer	Description
0x8001		Read Control Register 1
0x1234		Dummy data word
	0x____	AD28msp01 completes data
	0x____	Transfer in progress
	0x0001	Address word
	0x0023	Contents of Control Register 1

Serial Port Timing

All serial transfers are synchronous. The receive data (SDI) and receive frame sync (SDIFS) are clocked into the device on the falling edge of SCLK. The receive frame sync (SDIFS) must be asserted one SCLK cycle before the first data bit is transferred. When receiving data, the AD28msp01 ignores the receive frame sync pin until the least significant bit is being received.

When transmitting data, the AD28msp01 asserts transmit frame sync (SDOFS) and transmit data (SDO) synchronous with the rising edge of SCLK. Transmit frame sync is transmitted one SCLK cycle before the first data bit is transferred.

Operating Modes
The AD28msp01 is capable of operating in several different modes, as described below.

V.32 TSYNC Mode
In V.32 TSYNC Mode, shown in Figure 7, the AD28msp01's transmit circuitry is synchronized to an external TSYNC signal. The AD28msp01's receive circuitry is sampled synchronous to the transmit circuitry, but the data can be resampled at a different phase by using the resampling interpolation filter.

TCONV, TBIT and TBAUD are generated internally but are phase-locked to the external TSYNC input signal with the digital phase-locked loop. RCONV, RBIT and RBAUD are generated internally (but frequency locked to TSYNC) and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

TCONV initiates a new DAC sample update, loads the ADC register (Data Register 2), and loads the DAC register (Data Register 0) with a new sample.

The digital resampling interpolation filter can be used for digital resampling of the received signal. Enable this function by setting Bit 9 in Control Register 0. The phase of the resampled signal is adjusted with the Receive Phase Adjust Register. Samples are loaded into the interpolator at the TCONV rate and are resampled at the RCONV rate.

When entering V.32 TSYNC Mode, RCONV is locked to TCONV before TCONV is locked to TSYNC. If this mode is entered from a non-V.32 mode, the device performs a soft reset. The time required to lock TCONV to RCONV is dependent on the phase difference between RCONV and TCONV when entering the mode.

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit rates, baud rates and TSYNC rate can be set to any combination of clock rates listed in the control register descriptions. The TSYNC field on Control Register 0 must be set to the frequency of the input pin.

Example
Transferring the following word sequence to the AD28msp01 will configure the device for V.32 TSYNC Mode at the clock rates indicated:

Word Transferred	Description
0x0000	Control Register 0 address word
0x0254	Enable interpolation filter, TSYNC = 7200, sample rate = 7200, mode = V.32 TSYNC
0x0002	Control Register 2 address word
0x0002	RBAUD = 2400, RBIT = 7200
0x0003	Control Register 3 address word
0x0023	TBAUD = 1200, TBIT = 4800
0x0001	Control Register 1 address word
0x0018	Configure and powerup device

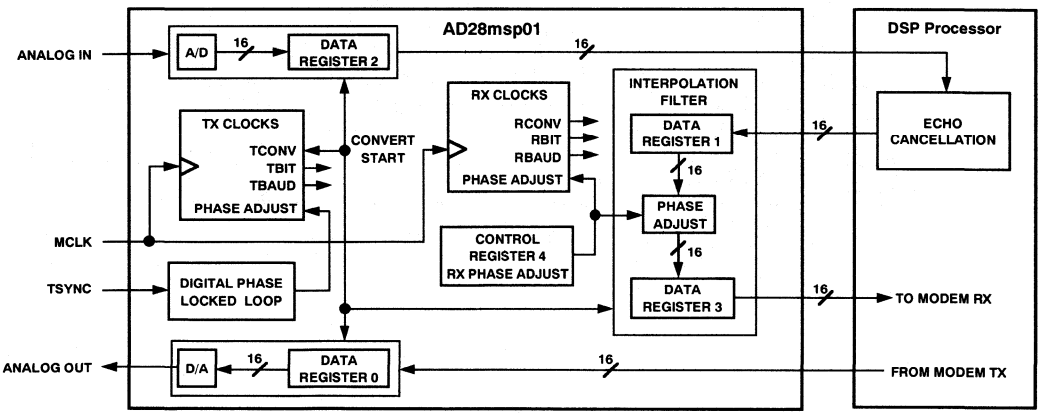


Figure 7. V.32 TSYNC Mode Block Diagram

V.32 Internal Sync Mode

In V.32 Internal Sync Mode, shown in Figure 8, the AD28msp01's transmit clocks are generated internally. The receive circuitry operates synchronous to the transmit circuitry, but the data can be resampled at a different phase through the resampling interpolation filter.

TCONV, TBIT and TBAUD are generated internally and can be phase adjusted with the Transmit Phase Adjust Register (Control Register 5). RCONV, RBIT and RBAUD are also generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

TCONV initiates a new ADC sample update, loads the ADC register (Data Register 2), and loads the DAC register (Data Register 0) with a new sample.

The digital resampling interpolation filter can be used for digital resampling of the received signal. Enable this function by setting Bit 9 in Control Register 0. The phase of the resampled signal is adjusted with the Receive Phase Adjust Register. Samples are loaded into the interpolator at the TCONV rate and are resampled at the RCONV rate.

When entering V.32 Internal Sync Mode, RCONV is first locked to TCONV. RCONV is then phase adjusted whenever a new value is written to the Receive Phase Adjust Register (Control Register 4). If this mode is entered from a non-V.32 mode, the device performs a soft reset. The time required to lock TCONV to RCONV is dependent on the phase difference between RCONV and TCONV when entering the mode.

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

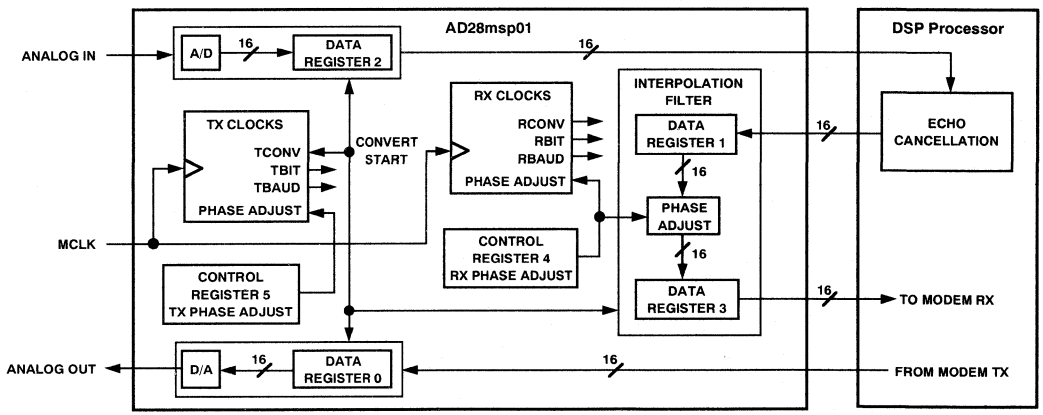


Figure 8. V.32 Internal Sync Mode Block Diagram

V.32 Loopback Mode

In V.32 Loopback Mode, shown in Figure 9, the AD28msp01's receive circuitry and transmit circuitry are locked together.

RCONV is generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4). RBIT, RBAUD, TCONV, TBIT and TBAUD are all locked to RCONV.

RCONV initiates a new DAC sample update and loads Data Register 2 with a new sample. The RCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

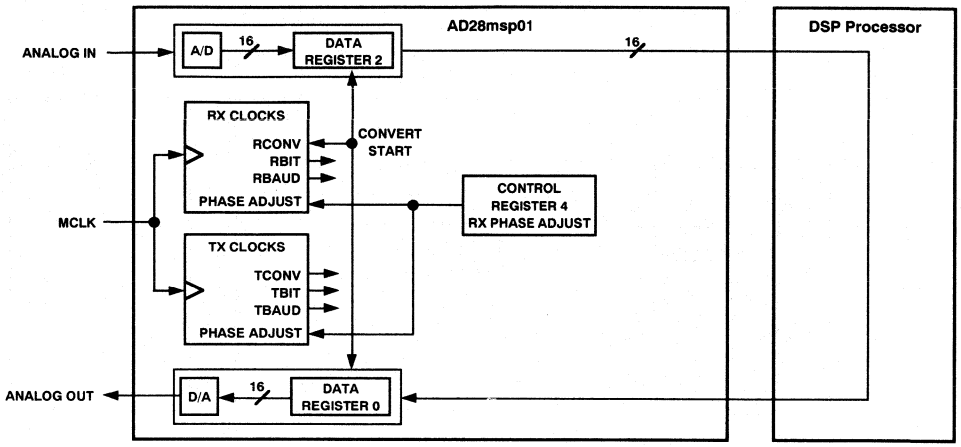


Figure 9. Loopback Mode Block Diagram

V.32ter TSYNC Mode

This mode is identical to V.32 TSYNC Mode except all clocks are scaled by a factor of 8/7 over the corresponding V.32 TSYNC rate. In this mode, the maximum value to which the receive and transmit phase adjust registers (Control Registers 4 and 5) may be set is +192.

Both TBIT and RBIT can be set to a 19,200 Hz rate that will not be scaled by a factor of 8/7, by setting the appropriate fields in Control Registers 2 and 3.

V.32ter Internal Sync Mode

This mode is identical to V.32 TSYNC Mode except all clocks are scaled by a factor of 8/7 over the corresponding V.32 TSYNC rate. In this mode, the maximum value to which the phase adjust registers (Control Registers 4 and 5) may be set is +192.

Both TBIT and RBIT can be set to a 19,200 Hz rate that will not be scaled by a factor of 8/7, by setting the appropriate fields in Control Registers 2 and 3.

Asynchronous Fallback TSYNC Mode

The Asynchronous Fallback TSYNC Mode is shown in Figure 10. TCONV, TBIT and TBAUD are generated internally but phase locked to the external TSYNC input signal. RCONV, RBIT and RBAUD are generated internally and can be phase adjusted with the Receive Phase Adjust Register (Control Register 4).

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit rates, baud rates and TSYNC rate can be set to any combination of clock rates listed in the control register descriptions.

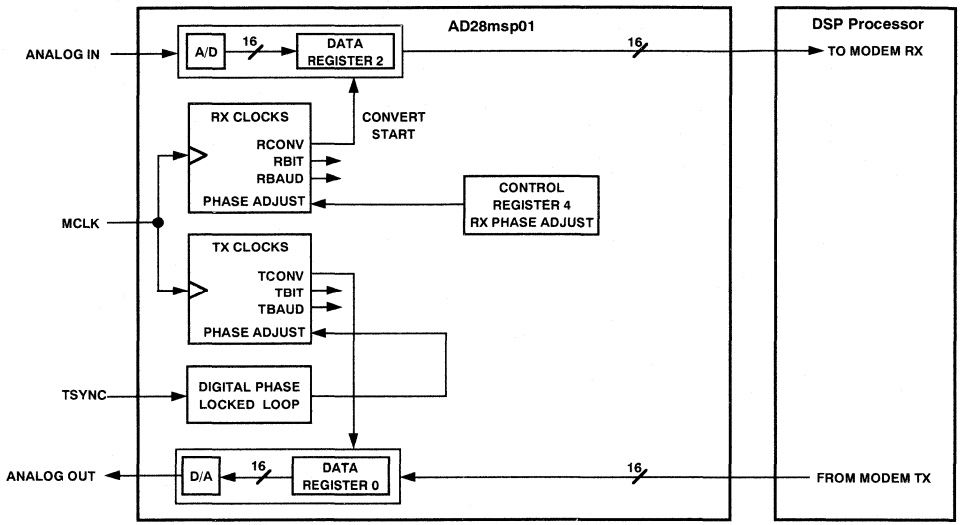


Figure 10. Asynchronous Fallback TSYNC Driven Mode Block Diagram

Asynchronous Fallback Mode

The Asynchronous Fallback Mode is shown in Figure 11. TCONV, TBIT and TBAUD are generated internally and can be phase adjusted with the Transmit Phase Adjust Register (Control Register 5). RCONV, RBIT and RBAUD are generated internally and can also be phase adjusted with the Receive Phase Adjust Register (Control Register 4). The digital phase-locked loop is not used in this operating mode.

This mode is entered by setting the Operating Mode field in Control Register 0. The RCONV/TCONV rate can be set to 9.6 kHz, 8.0 kHz or 7.2 kHz by setting the sample rate bit field in Control Register 0. The TBIT and TBAUD clock rates are set by adjusting the appropriate bits in Control Register 3. The RBIT and RBAUD clock rates are set by adjusting the appropriate bits in Control Register 2. The bit and baud rates can be set to any combination of clock rates listed in the control register descriptions.

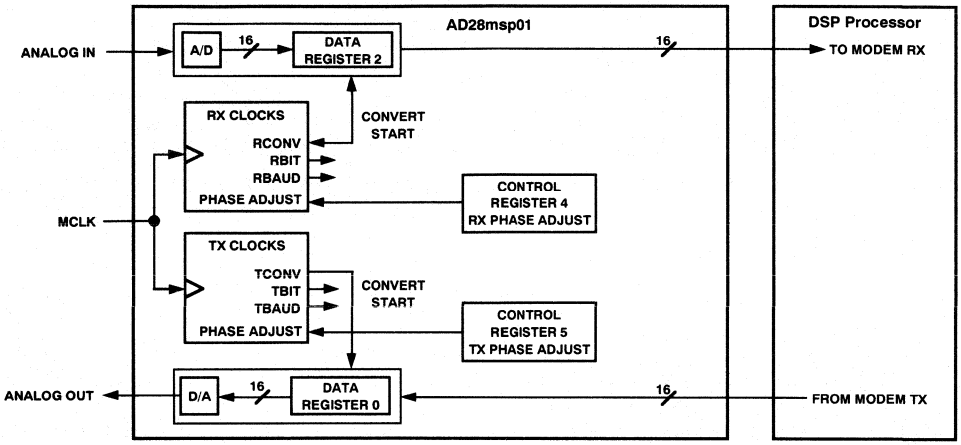


Figure 11. Asynchronous Fallback Mode Block Diagram

Operating Mode Summary
Table III summarizes the operating modes.

Table III. Operating Mode Summary

Mode	Initial Phase Lock After Entering Mode	Normal DPLL* Operation	Phase Adjust Register Programmable†	Resampling Interpolator	Internal Filter Operation Synchronous To: ADC	DAC	Control Register 0 OP 2–0
Async Fallback	no phase lock	no phase lock	RCV, TX	not used	RCONV	TCONV	0 0 0
Async TSYNC	TCONV lock to TSYNC	TCONV lock to TSYNC	RCV	not used	RCONV	TCONV	1 1 1
V.32 TSYNC	RCONV lock to TCONV	TCONV lock to TSYNC	RCV	Input synchronous and in phase with TCONV, Output synchronous and in phase with RCONV	TCONV	TCONV	1 0 0
V.32 Internal Sync	RCONV lock to TCONV	no phase lock	RCV, TX	Input synchronous and in phase with TCONV, Output synchronous and in phase with RCONV	TCONV	TCONV	1 0 1
V.32 Loopback	TCONV lock to RCONV	no phase lock	RCV††	not used	TCONV	TCONV	1 1 0

NOTES
*DPLL – Digital Phase-Locked Loop.
†RCV phase adjusted via Control Register 4, TX phase adjusted via Control Register 5.
††Adjusting RCV phase also adjusts TX phase in this mode.
Note: All receive clocks: RBIT, RBAUD are synchronous to RCONV. All transmit clocks: TBIT, TBAUD are synchronous to TCONV.

DESIGN CONSIDERATIONS

Analog Input

The analog input signal to the AD28msp01 must be ac coupled. Figure 12 shows the recommended input circuit for the AD28msp01's analog input pin (V_{IN}). The circuit of Figure 12 implements a first-order low-pass filter with a 3 dB point at 20 kHz; this is the only filter that must be implemented external to the AD28msp01 to prevent aliasing of the sampled signal. Since the AD28msp01's ADC uses a highly oversampled approach that transfers the bulk of the anti-aliasing filtering into the digital domain, the off-chip anti-aliasing filter need only be of low order.

In the circuit shown in Figure 12, scaling of the analog input is achieved by the resistors R_{IN} and R_{FB}. The input signal gain, $-R_{FB}/R_{IN}$, can be adjusted by varying the values of these resistors. Total gain must be configured to ensure that a full-scale input signal (at C_{IN} in Figure 12) produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed V_{INMAX}, which is specified under "Analog Interface Electrical Characteristics." If the total gain is increased above unity (i.e., gain >1), signal-to-noise (SNR + THD) performance may not meet the listed specifications.

The DC offsetting of the analog input signal is accomplished with an on-chip voltage reference which nominally equals 2.5 V. The input signal must be ac coupled with an external coupling capacitor (C_{IN}). C_{IN} and R_{IN} should be chosen to ensure a coupling corner frequency of 30 Hz. C_{IN} should be 0.1 μF or larger.

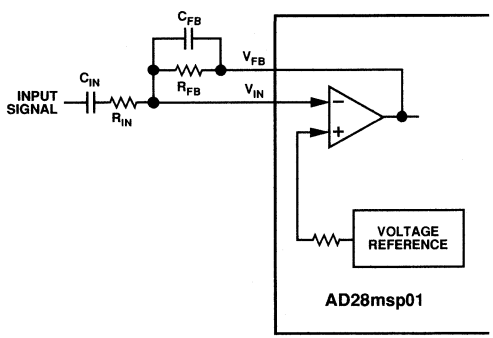


Figure 12. Recommended Analog Input Circuit

To select values for the components shown in Figure 12, use the following equations:

$$Gain = \frac{-R_{FB}}{R_{IN}}$$

$$C_{IN} = \frac{1}{60\pi R_{IN}}$$

$$C_{FB} = \frac{1}{(2\pi)(20 \star 10^3)R_{FB}}$$

$10\ k\Omega \leq R_{FB}, R_{IN} \leq 50\ k\Omega$

$150\ pF \leq C_{FB} \leq 600\ pF$

Figure 13 shows an example of a typical input circuit configured for 0 dB gain. The circuit's diodes are used to prevent the input signal from exceeding maximum limits.

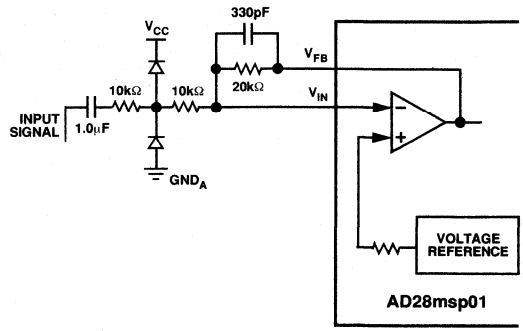


Figure 13. Typical Input Circuit (0 dB Gain)

Analog Output

The AD28msp01's differential analog output (V_{OUTP},V_{OUTN}) is produced by an on-chip differential amplifier. The differential amplifier can drive a minimum load of 2 kΩ ($R_L \geq 2\ k\Omega$) and has a maximum differential output voltage swing of 6.312 V peak-to-peak (3.17 dBm0). The differential output can be ac-coupled directly to a load or dc-coupled to an external amplifier.

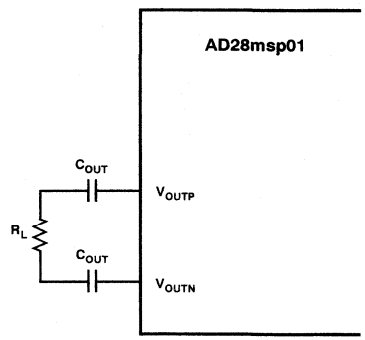


Figure 14. Example Circuit for Differential Output with AC Coupling

Figure 14 shows a simple circuit providing a differential output with ac coupling. The capacitor of this circuit (C_{OUT}) is optional; if used, its value can be chosen as follows:

$$C_{OUT} = \frac{1}{(60\ \pi)\ R_L}$$

The V_{OUTP}–V_{OUTN} outputs must be used as differential outputs; do not use either as a single-ended output. Figure 15 shows an example circuit which can be used to convert the differential output to a single-ended output. The circuit uses a differential-to-single-ended amplifier, the Analog Devices SSM-2141.

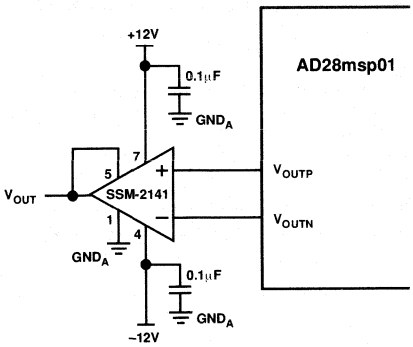


Figure 15. Example Circuit for Single-Ended Output

Single Power Supply Operation
Use of a single +5 V power supply is possible with the AD28msp01. If a single supply is used, the analog power supply input to the device must be properly filtered. The proper filter is dependent on the noise present in your system.

PC Board Layout Considerations
Separate analog and digital ground planes should be provided for the AD28msp01 in order to assure the characteristics of the device's ADC and DAC. The two ground planes should be connected only at a single point. The point of connection may be at the system power supply, at the PC board power connection, or at any other appropriate location. Multiple connections between the analog and digital ground planes should be avoided.

The ground planes should be designed such that all noise-sensitive areas are isolated from one another and critical signal traces (such as digital clocks and analog signals) are as short as possible.

Each +5 V supply pin of the AD28msp01 should be bypassed to ground with a 0.1 μF capacitor. These capacitors should be low inductance, monolithic, ceramic, and surface-mount. The capacitor leads and PC board traces should be as short as possible to minimize inductive effects. In addition, a 10 μF capacitor should be connected between V_{DD} and ground, near the PC board power connection.

MCLK Frequency
The sigma-delta converters and digital filters of the AD28msp01 are specifically designed to operate at a master clock (MCLK) frequency of 13.824 MHz. MCLK must equal 13.824 MHz to guarantee the filter characteristics and sample rate of the ADC and DAC. The AD28msp01 is not tested or characterized at any other clock frequency.

DEFINITION OF SPECIFICATIONS

Typical (Typ) specifications represent nominal performance at 25°C with V_{CC} and V_{DD} set to +5 V.

Minimum (Min) and Maximum (Max) specifications are guaranteed across the full operating range, however, devices are tested only at the indicated test conditions.

Absolute Gain
Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured with a 1.0 kHz sine wave at 0 dBm0. The absolute gain specification is used as a reference for gain tracking error specification.

Gain Tracking Error
Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 1 kHz at 0 dBm0 (equal to absolute gain). Gain tracking error at 0 dBm0 is 0 dB by definition.

SNR
Signal-to-noise ratio is defined to be the ratio of the rms value of the measured input signal to the rms sum of all the spectral components in the specified passband, excluding dc and harmonic components.

THD
Total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of the harmonic components in the specified passband.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, f_a and f_b, any active device with nonlinearities will create distortion products at sum and difference frequencies of $mf_a \pm nf_b$ where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. This specification contains the second order terms include $(f_a + f_b)$ and $(f_a - f_b)$, and the third order terms include $(2f_a + f_b)$, $(2f_a - f_b)$, $(f_a + 2f_b)$, and $(f_a - 2f_b)$.

Idle Channel Noise
Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the specified passband).

Crosstalk
Crosstalk is defined as the ratio of the amplitude of a 0 dB signal appearing on one channel to the amplitude of the same signal coupled onto the other, idle channel. Crosstalk is expressed in dB.

Power Supply Rejection
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a 1 kHz, 100 mV p-p sine wave and measuring the relative level at the output.

Group Delay
Group delay is defined as the derivative of radian phase with respect to radian frequency, $\partial\phi(\omega)/\partial\omega$. Group delay is a measure of the linearity of the phase response of a linear system. A linear system with a constant group delay has a linear phase response. The deviation of the group delay away from a constant indicates the degree of nonlinear phase response of the system.

AD28msp01—SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	K Grade Min	K Grade Max	Unit
V_{DD}, V_{CC}	Supply Voltage	4.75	5.25	V
T_{AMB}	Ambient Operating Temperature	0	+70	°C

Refer to Environmental Conditions for information on case temperature and thermal specifications.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . . . 0°C to +70°C
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature (5 seconds) SOIC . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Test Conditions Unless Otherwise Noted

Temperature	+25°C
Sample Rate (F_S)	9.6 kHz
Input Signal Frequency	993.75 Hz
Input Signal Level	0.0 dBm0
Analog Input Gain	Unity
Analog Output Passband	220 Hz to 3.4 kHz

ESD SENSITIVITY

The AD28msp01 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per Method 3015 of MIL-STD-883D, the AD28msp01 has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam, trays, or tubes, and the foam should be discharged to the destination socket before devices are removed.

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2.4			V	V_{DD} = max
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = min
V_{OH}	Output High Voltage	2.4			V	V_{DD} = min, I_{OH} = −0.5 mA
V_{OL}	Output Low Voltage			0.4	V	V_{DD} = min, I_{OL} = 2 mA
I_{IH}	High Level Input Current			10	μA	V_{DD} = max, V_{IN} = max
I_{IL}	Low Level Input Current			10	μA	V_{DD} = max, V_{IN} = 0 V
I_{OZL}	Low Level Output 3-State Leakage Current			10	μA	V_{DD} = max, V_{IN} = max
I_{OZH}	High Level Output 3-State Leakage Current			10	μA	V_{DD} = max, V_{IN} = 0 V
C_I	Digital Input Capacitance[1]			10	pF	

[1]Guaranteed but not tested.

3

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ADC:					
I_L	Input Leakage Current at V_{IN}		10		nA
R_I	Input Resistance at V_{IN}		100		MΩ
C_{IL}	Input Load Capacitance at V_{FB}		10		pF
VIN_{MAX}	Maximum Input Range[1]		3.156		V p–p
DAC:					
R_O	Output Resistance		1		Ω
V_{OFF}	Output DC Offset[2]	−400		400	mV
C_{OL}	Output Load Capacitance			100	pF
V_O	Maximum Voltage Output Swing (p–p) Across R_L				
	Single-Ended		3.156		V
	Differential		6.312		V
R_L	Load Resistance	2			kΩ

Test Conditions for all analog interface tests: Unity input gain, no load on analog output (V_{OUTP}–V_{OUTN}).

[1]At unity gain on input.
[2]Between V_{OUTP} and V_{OUTN}.

POWER DISSIPATION

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Analog Operating Voltage	4.75	5.0	5.25	V
V_{DD}	Digital Operating Voltage	4.75	5.0	5.25	V
I_{CC}	Analog Operating Current Active[1]		24	35	mA
I_{DD}	Digital Operating Current Active[1]		11	20	mA
P_1	Power Dissipation Active[1]			350	mW
I_{CC}	Analog Operating Current Inactive[2]			300	μA
I_{DD}	Digital Operating Current Inactive[2]			200	μA
P_0	Power Dissipation Inactive[2]			4.0	mW

Test conditions: V_{DD} = V_{CC} = 5.0 V, MCLK frequency 13.824 MHz, no load on digital pins, analog inputs ac-coupled to ground, no load on analog output (V_{OUTP}–V_{OUTN}).

[1]Active: AD28msp01 operational ($\overline{PWDD}$ and $\overline{PWDA}$ set to 1 in control register 1).
[2]Inactive: AD28msp01 in power-down state ($\overline{PWDD}$ and $\overline{PWDA}$ set to 0 in Control Register 1) and MCLK tied to V_{DD}.

TIMING PARAMETERS

Parameter		Min	Max	Unit
Clock Signals				
Timing Requirement:				
F_{MCK}	MCLK Frequency	13.824	13.824	MHz ± 50 ppm
t_{MCK}	MCLK Period	72.34	72.34	ns
t_{MKL}	MCLK Width Low	$0.5t_{MCK}$ − 10	$0.5t_{MCK}$ + 10	ns
t_{MKH}	MCLK Width High	$0.5t_{MCK}$ − 10	$0.5t_{MCK}$ + 10	ns
Switching Characteristic:				
t_{SCK}	SCLK Period	$8t_{MCK}$ − 10	$8t_{MCK}$ + 10	ns
t_{SKL}	SCLK Width Low	$4t_{MCK}$ − 10	$4t_{MCK}$ + 10	ns
t_{SKH}	SCLK Width High	$4t_{MCK}$ − 10	$4t_{MCK}$ + 10	ns
Control Signals				
Timing Requirement:				
t_{RSP}	$\overline{\text{RESET}}$ Width Low	$5t_{MCK}$[1]		ns

NOTE
[1]Applies after power-up sequence is complete. Internal phase lock loop requires no more than 1000 processor cycles assuming stable CLKIN (not including crystal oscillator start-up time).

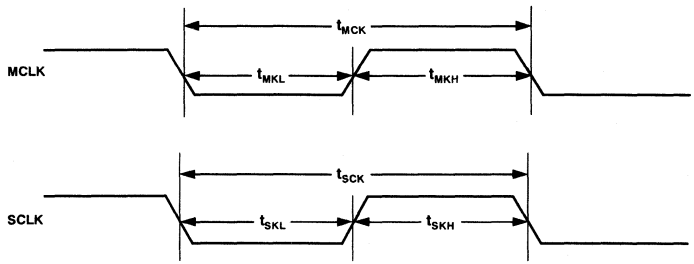


Figure 16. Clock Signals

Serial Port 3-State

Parameter		Min	Max	Unit
Switching Characteristic:				
t_{SPD}	CS Low to SDO, SDOFS, SCLK Disable		20	ns
t_{SPE}	CS High to SDO, SDOFS, SCLK Enable	0		ns
t_{SPV}	CS High to SDO, SDOFS, SCLK Valid		25	ns

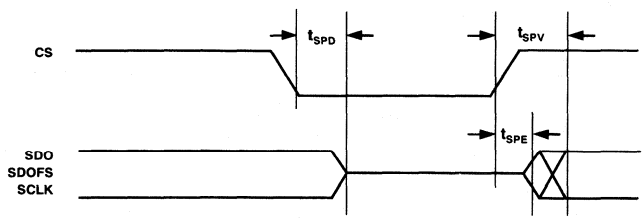


Figure 17. Serial Port 3-State

Output Disable Time

Output pins are considered to be disabled when they have stopped driving and started a transition from the measured output high or low voltage to a high-impedance state. The output disable time (t_{DIS}) is the difference of $t_{MEASURED}$ and t_{DECAY}, as shown in the Output Enable/Disable diagram. The time, $t_{MEASURED}$, is the interval from when a reference signal reaches a high or low voltage level to when the output voltages have changed by 0.5 V from the measured output high or low voltage. The decay time, t_{DECAY}, is dependent on the capacitive load, C_L, and the current load, i_L, on the output pin. It can be approximated by the following equation:

$$t_{DECAY} = \frac{C_L \cdot 0.5\ V}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. If multiple pins (such as the data bus) are disabled, the measurement value is that of the last pin to stop driving.

Output Enable Time

Output pins are considered to be enabled when they have made a transition from a high-impedance state to when they start driving. The output enable time (t_{ENA}) is the interval from when a reference signal reaches a high or low voltage level to when the output has reached a specified high or low trip point, as shown in the Output Enable/Disable diagram. If multiple pins (such as the data bus) are enabled, the measurement value is that of the first pin to start driving.

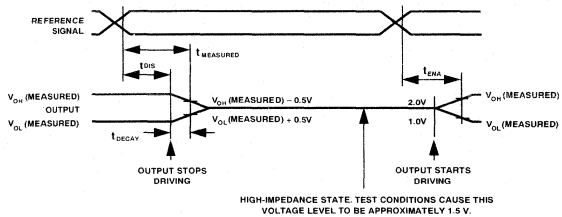


Figure 18. Output Enable/Disable

Serial Ports

Parameter		Min	Max	Unit
Timing Requirement:				
t_{SCS}	SDI/SDIFS Setup before SCLK Low	10		ns
t_{SCH}	SDI/SDIFS Hold after SCLK Low	15		ns
Switching Characteristic:				
t_{RD}	SDOFS Delay from SCLK High		30	ns
t_{RH}	SDOFS Hold after SCLK High	0		ns
t_{SCDH}	SDO Hold after SCLK High	0		ns
t_{SCDD}	SDO Delay from SCLK High		30	ns

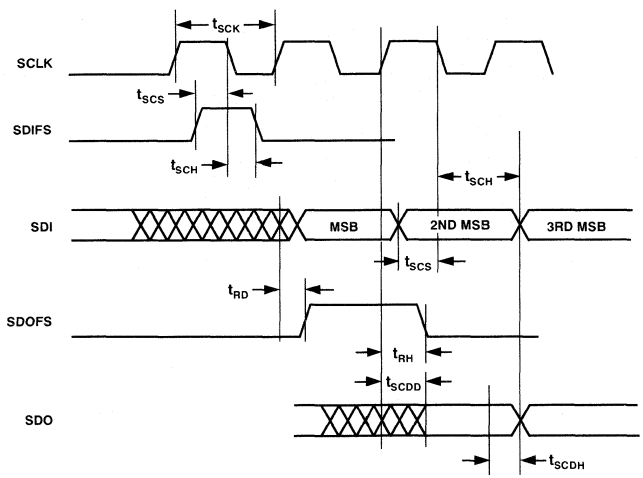


Figure 19. Serial Ports

DIGITAL TEST CONDITIONS

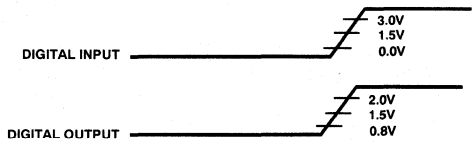


Figure 20. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

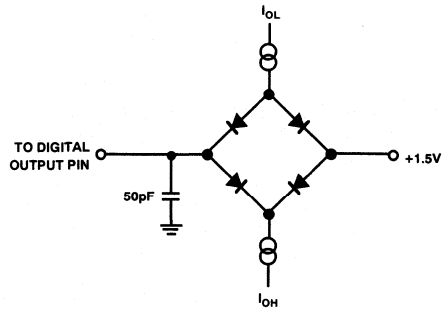


Figure 21. Equivalent Device Loading for AC Measurements (Includes ALI Fixtures)

GAIN

Parameter	Min	Typ	Max	Unit	Test Conditions
ADC Absolute Gain	−0.5	0	0.5	dBm0	1.0 kHz, 0 dBm0
ADC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 and −60 dBm0
DAC Absolute Gain	−0.5	0	0.5	dBm0	1.0 kHz, 0 dBm0
DAC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 and −60 dBm0

Frequency Response*

ADC	9.6 kHz	8.0 kHz	7.2 kHz
Passband Ripple	<0.2 dB	<0.2 dB	<0.2 dB
Low-Pass Passband Cutoff Frequency	3.4 kHz	3.4 kHz	3.3 kHz
Low-Pass Stopband Cutoff Frequency	4.8 kHz	4.0 kHz	3.6 kHz
High-Pass Passband Cutoff Frequency	220 Hz	220 Hz	220 Hz
High-Pass Stopband Cutoff Frequency	60 Hz	60 Hz	60 Hz
Low-Pass Stopband Rejection	−50 dB	−50 dB	−50 dB
High-Pass Stopband Rejection	−50 dB	−50 dB	−50 dB
DAC	**9.6 kHz**	**8.0 kHz**	**7.2 kHz**
Passband Ripple	<0.2 dB	<0.2 dB	<0.2 dB
Passband Cutoff Frequency	3.4 kHz	3.4 kHz	3.4 kHz
Low-Pass Stopband Cutoff Frequency	4.8 kHz	4.0 kHz	3.6 kHz
Stopband Rejection	−50 dB	−50 dB	−50 dB

*Frequency Response is guaranteed but not tested.

NOISE AND DISTORTION

Parameter	Min	Typ	Max	Unit
ADC Signal-to-Noise Ratio	+72	+80		dB
ADC Total Harmonic Distortion			−72	dB
DAC Signal-to-Noise Ratio	+72	+80		dB
DAC Total Harmonic Distortion			−72	dB
ADC Idle Channel Noise		−80	−72	dBm0
DAC Idle Channel Noise		−80	−72	dBm0
ADC Crosstalk[1]			−72	dB
DAC Crosstalk[1]			−72	dB
ADC Intermodulation Distortion[1]			−72	dB
DAC Intermodulation Distortion[1]			−72	dB
ADC Digital Power Supply Rejection[1]			−45	dB
DAC Digital Power Supply Rejection[1]			−45	dB
ADC Analog Power Supply Rejection[1]			−35	dB
DAC Analog Power Supply Rejection[1]			−35	dB

[1]Guaranteed but not tested.

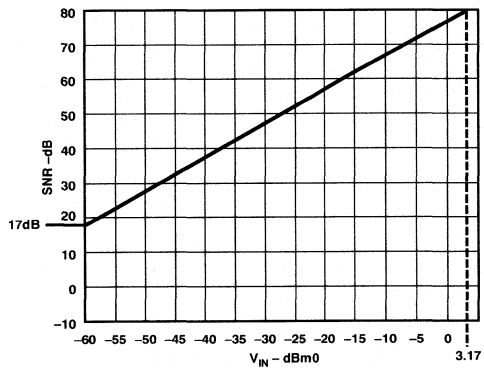


Figure 22. Typical SNR vs. V_{IN}

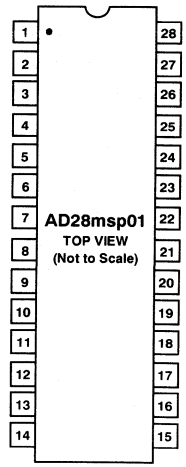
GROUP DELAY*

	9.6 kHz	8.0 kHz	7.2 kHz	Unit
ADC Group Delay	12	13	15	ms
ADC Low-Pass Filter Group Delay	2	3	5	ms
ADC High-Pass Filter Group Delay	10	10	10	ms
DAC Group Delay	2	3	5	ms
Resampling Filter Group Delay	2	3	5	ms

*Group Delay is guaranteed but not tested.

PIN CONFIGURATIONS
28-Pin DIP and 28-Lead SOIC

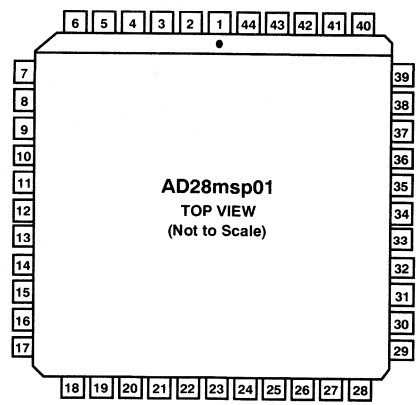
PIN	NAME	PIN	NAME
1	V_{CC}	15	GND_D
2	V_{OUTP}	16	V_{DD}
3	V_{OUTN}	17	V_{DD}
4	GND_A	18	SCLK
5	GND_D	19	SDO
6	$\overline{RESET}$	20	SDOFS
7	TSYNC	21	SDIFS
8	TCONV	22	SDI
9	TBIT	23	CS
10	TBAUD	24	GND_D
11	RCONV	25	GND_A
12	RBIT	26	V_{FB}
13	RBAUD	27	V_{IN}
14	MCLK	28	NC



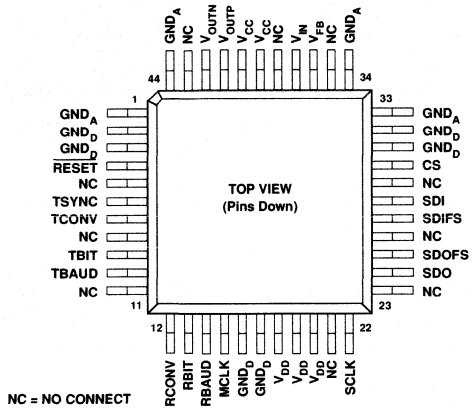
PIN CONFIGURATIONS
44-Lead Plastic Leaded Chip Carrier (PLCC)

PIN	NAME	PIN	NAME
1	V_{CC}	23	GND_D
2	V_{CC}	24	V_{DD}
3	V_{OUTP}	25	V_{DD}
4	V_{OUTN}	26	V_{DD}
5	NC	27	NC
6	GND_A	28	SCLK
7	GND_A	29	NC
8	GND_D	30	SDO
9	GND_D	31	SDOFS
10	$\overline{RESET}$	32	NC
11	NC	33	SDIFS
12	TSYNC	34	SDI
13	TCONV	35	NC
14	NC	36	CS
15	TBIT	37	GND_D
16	TBAUD	38	GND_D
17	NC	39	GND_A
18	RCONV	40	GND_A
19	RBIT	41	NC
20	RBAUD	42	V_{FB}
21	MCLK	43	V_{IN}
22	GND_D	44	NC

NC = NO CONNECT



44-Lead Thin Quad Flatpack



3

PIN CONFIGURATIONS

PIN	NAME	PIN	NAME
1	GND_A	23	NC
2	GND_D	24	SDO
3	GND_D	25	SDOFS
4	$\overline{RESET}$	26	NC
5	NC	27	SDIFS
6	TSYNC	28	SDI
7	TCONV	29	NC
8	NC	30	CS
9	TBIT	31	GND_D
10	TBAUD	32	GND_D
11	NC	33	GND_A
12	RCONV	34	GND_A
13	RBIT	35	NC
14	RBAUD	36	V_{FB}
15	MCLK	37	V_{IN}
16	GND_D	38	NC
17	GND_D	39	V_{CC}
18	V_{DD}	40	V_{CC}
19	V_{DD}	41	V_{OUTP}
20	V_{DD}	42	V_{OUTN}
21	NC	43	NC
22	SCLK	44	GND_A

ORDERING GUIDE

Part Number	Temperature Range	Package	Package Option*
AD28msp01KP	0°C to +70°C	44-Pin PLCC	P-44A
AD28msp01KN	0°C to +70°C	28-Pin Plastic DIP	N-28A
AD28msp01KR	0°C to +70°C	28-Lead SOIC	R-28
AD28msp01KST†	0°C to +70°C	44-Lead TQFP	ST-44A

NOTES
*P = PLCC, N = Plastic DIP, R = Small Outline (SOIC), ST = TQFP. For outline information see Package Information section.
†In Development

ANALOG DEVICES

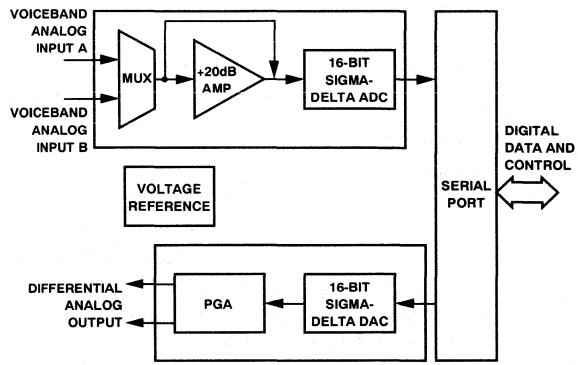
Voiceband Signal Port

AD28msp02

FEATURES

Complete Analog I/O Port for Voiceband DSP Applications
Linear-Coded 16-Bit Sigma-Delta ADC
Linear-Coded 16-Bit Sigma-Delta DAC
On-Chip Anti-Aliasing and Anti-Imaging Filters
On-Chip Voltage Reference
8 kHz Sampling Frequency
Twos Complement Coding
65 dB SNR + THD
Programmable Gain on DAC and ADC
Serial Interface To DSP Processors
24-Pin DIP/28-Lead SOIC
Single 5 V Power Supply

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD28msp02 Voiceband Signal Port is a complete analog front end for high performance voiceband DSP applications. Compared to traditional μ-law and A-law codecs, the AD28msp02's linear-coded ADC and DAC maintain wide dynamic range while maintaining superior SNR and THD. A sampling rate of 8.0 kHz coupled with 65 dB SNR + THD performance make the AD28msp02 attractive in many telecom and speech processing applications, for example digital cellular radio and high quality telephones. The AD28msp02 simplifies overall system design by requiring only a single +5 V power supply.

The inclusion of on-chip anti-aliasing and anti-imaging filters, 16-bit sigma-delta ADC and DAC, and programmable gain amplifiers ensures a highly integrated and compact solution to voiceband analog processing requirements. Sigma-delta conversion technology eliminates the need for complex off-chip anti-aliasing filters and sample-and-hold circuitry.

The AD28msp02's serial I/O port provides an easy interface to host DSP microprocessors such as the ADSP-2101, ADSP-2105, and ADSP-2111. The AD28msp02 is available in a 24-pin, 0.3″ plastic DIP and a 28-lead SOIC package.

FUNCTIONAL DESCRIPTION

Figure 1 shows a block diagram of the AD28msp02.

A/D CONVERSION

The A/D conversion circuitry of the AD28msp02 consists of two analog input amplifiers, an optional 20 dB preamplifier, and a sigma-delta analog-to-digital converter (ADC). The analog input signal to the AD28msp02 must be ac-coupled.

Analog Input Amplifiers

The two analog input amplifiers (NORM, AUX) are internally biased by an on-chip voltage reference in order to allow operation of the AD28msp02 with a single +5 V power supply.

An analog multiplexer selects either the NORM or AUX amplifier as the input to the ADC's sigma-delta modulator. The optional 20 dB preamplifier may be used to increase the signal level; the preamplifier can be inserted before the modulator or can be bypassed. Input signal level to the sigma-delta modulator should not exceed V_{INMAX}, which is specified under "Analog Interface Electrical Characteristics." Refer to "Analog Input" in the "Design Considerations" section of this data sheet for more information.

The input multiplexer and 20 dB preamplifier are configured by bits 0 and 1 (IPS, IMS) of the AD28msp02's control register. If the multiplexer setting is changed while an input signal is being processed, the ADC's output must be allowed time to settle to ensure that the output data is valid.

ADC

The ADC consists of a 2nd-order analog sigma-delta modulator, an anti-aliasing decimation filter, and a digital high-pass filter. The sigma-delta modulator noise-shapes the signal and produces 1-bit samples at a 1.0 MHz rate. This bit stream, which represents the analog input signal, is fed to the anti-aliasing decimation filter.

Decimation Filter

The anti-aliasing decimation filter contains two stages. The first stage is a $sinc^4$ digital filter that increases resolution to 16 bits and reduces the sample rate to 40 kHz. The second stage is an IIR low-pass filter.

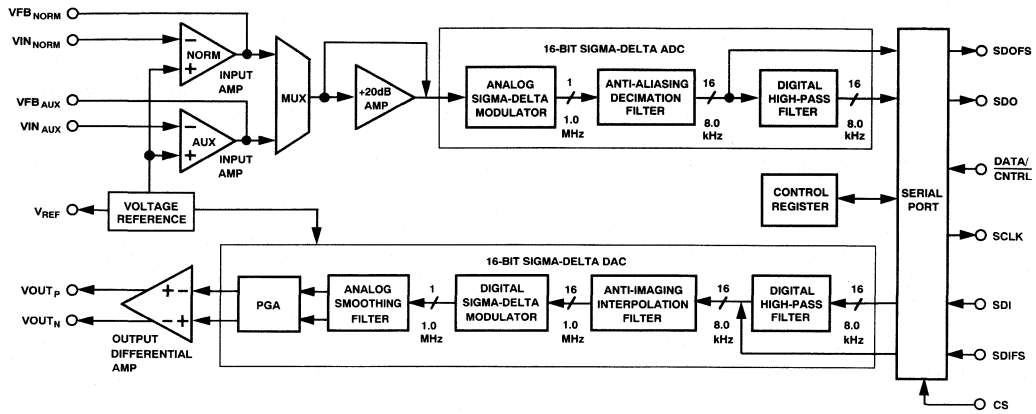


Figure 1. AD28msp02 Block Diagram

The IIR low-pass filter is a 10th-order elliptic filter with a passband edge at 3.7 kHz and a stopband attenuation of 65 dB at 4 kHz. This filter has the following specifications:

Filter type:	10th-order low-pass elliptic IIR
Sample frequency:	40.0 kHz
Passband cutoff:*	3.70 kHz
Passband ripple:	±0.2 dB
Stopband cutoff:	4.0 kHz
Stopband ripple:	−65.00 dB

*The passband cutoff frequency is defined to be the last point in the passband that meets the passband ripple specification.

(Note that these specifications apply only to this filter, and not to the entire ADC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 2 shows the frequency response of the IIR low-pass filter.

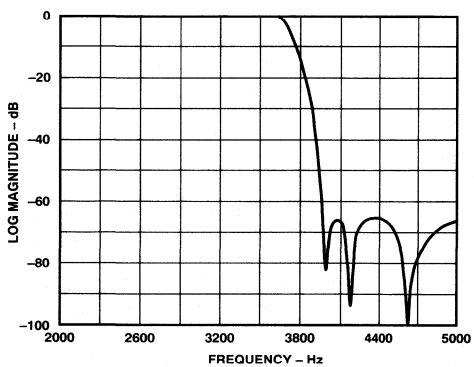


Figure 2. IIR Low-Pass Filter Frequency Response

High-Pass Filter

The digital high-pass filter removes frequency components at the low end of the spectrum; it attenuates signal energy below the passband of the converter. The high-pass filter can be bypassed by setting the ADBY bit (Bit 3) of the AD28msp02's control register.

The high-pass filter is a 4th-order elliptic filter with a passband cutoff at 150 Hz. Stopband attenuation is 25 dB. This filter has the following specifications:

Filter type:	4th-order high-pass elliptic IIR
Sample frequency:	8.0 kHz
Passband cutoff:	150.0 Hz
Passband ripple:	±0.2 dB
Stopband cutoff:	100.0 Hz
Stopband ripple:	−25.00 dB

(Note that these specifications apply only to this filter, and not to the entire ADC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 3 shows the frequency response of the high-pass filter.

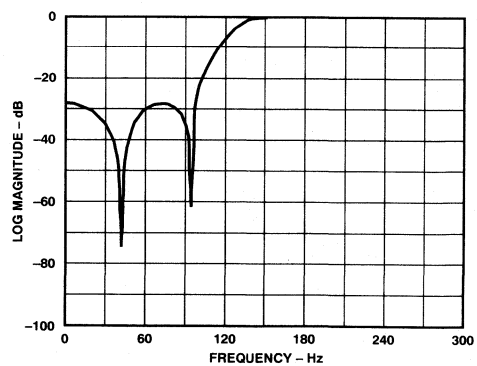


Figure 3. High-Pass Filter Frequency Response

Passband ripple is ±0.2 dB for the combined effects of the ADC's digital filters (i.e., high-pass filter and IIR low-pass of the decimation filter) in the 300 Hz–3400 Hz passband.

The output of the ADC is transferred to the AD28msp02's serial port (SPORT) at an 8 kHz rate, for transmission to the host DSP processor. Maximum group delay in the ADC will not exceed 1 ms in the region from 300 Hz to 3 kHz.

PIN DESCRIPTIONS

Pin Name	I/O/Z	Function
VIN_{NORM}	I	Analog input to inverting terminal of NORM input amplifier.
VFB_{NORM}	O	Output terminal of NORM amplifier.
VIN_{AUX}	I	Analog input to inverting terminal of AUX input amplifier.
VFB_{AUX}	O	Output terminal of AUX amplifier.
$VOUT_P$	O	Analog output from noninverting terminal of differential output amplifier.
$VOUT_N$	O	Analog output from inverting terminal of differential output amplifier.
V_{REF}	O	On-chip bandgap voltage reference (2.5 V ± 10%).
MCLK	I	Master clock input; frequency must equal 13.0 MHz to guarantee listed specifications.
SCLK	O/Z	Serial clock used to clock data or control bits to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by 5. SCLK is 3-stated when CS is low.
SDI	I	Serial data input of SPORT. Both data and control information are input on this pin. Input at SDI is ignored when CS is low.
SDO	O/Z	Serial data output of SPORT. Both data and control information are output on this pin. SDO is 3-stated when CS is low.
SDIFS	I	Framing signal for SDI serial transfers. Input at SDIFS is ignored when CS is low.
SDOFS	O/Z	Framing signal for SDO serial transfers. SDOFS is 3-stated when CS is low.
DATA/$\overline{\text{CNTRL}}$	I	Configures AD28msp02 for either data or control information transfers (via SPORT).
CS	I	Active-high chip select. Can be used to 3-state the SPORT interface; when CS is low, the SCLK, SDO, and SDOFS outputs are 3-stated and the SDI and SDIFS inputs are ignored. If CS is deasserted during a serial data transfer, the 16-bit word being transmitted is lost.
$\overline{\text{RESET}}$	I	Active low reset signal; resets Control Register and clears digital filters. $\overline{\text{RESET}}$ does not 3-state the SPORT outputs (SCLK, SDO, SDOFS).
V_{CC}		Analog supply voltage; nominal +5 V.
GND_A		Analog ground.
V_{DD}		Digital supply voltage; nominal +5 V.
GND_D		Digital ground.

D/A CONVERSION

The D/A conversion circuitry of the AD28msp02 consists of a sigma-delta digital-to-analog converter (DAC), an analog smoothing filter, a programmable gain amplifier, and a differential output amplifier.

DAC

The AD28msp02's sigma-delta DAC implements digital filters and a sigma-delta modulator with the same characteristics as the filters and modulator of the ADC. The DAC consists of a digital high-pass filter, an anti-imaging interpolation filter, and a digital sigma-delta modulator.

The DAC receives 16-bit samples from the host DSP processor via AD28msp02's serial port at an 8 kHz rate. If the host processor fails to write a new value to the serial port, the existing (previous) data is read again. The data stream is filtered first by the DAC's high-pass filter and then by the anti-imaging interpolation filter. These filters have the same characteristics as the ADC's anti-aliasing decimation filter and digital high-pass filter.

The output of the interpolation filter is fed to the DAC's digital sigma-delta modulator, which converts the 16-bit data to 1-bit samples at a 1.0 MHz rate. The modulator noise-shapes the signal such that errors inherent to the process are minimized in the passband of the converter. The bit stream output of the sigma-delta modulator is fed to the AD28msp02's analog smoothing filter where it is converted to an analog voltage.

High-Pass Filter

The digital high-pass filter of the AD28msp02's DAC has the same characteristics as the high-pass filter of the ADC. The high-pass filter removes frequency components at the low end of the spectrum; it attenuates signal energy below the passband of the converter. The DAC's high-pass filter can be bypassed by setting the DABY bit (Bit 2) of the AD28msp02's control register.

The high-pass filter is a 4th-order elliptic filter with a passband cutoff at 150 Hz. Stopband attenuation is 25 dB. This filter has the following specifications:

Filter type:	4th-order high pass elliptic IIR
Sample frequency:	8.0 kHz
Passband cutoff:	150.0 Hz
Passband ripple:	±0.2 dB
Stopband cutoff:	100.0 Hz
Stopband ripple:	−25.00 dB

(Note that these specifications apply only to this filter, and not to the entire DAC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 3 shows the frequency response of the high-pass filter.

Interpolation Filter

The anti-imaging interpolation filter contains two stages. The first stage is an IIR low-pass filter that interpolates the data rate from 8 kHz to 40 kHz and removes images produced by the interpolation process. The output of this stage is then interpolated to 1.0 MHz and fed to the second stage, a $sinc^4$ digital filter that attenuates images produced by the 40 kHz to 1.0 MHz interpolation process.

The IIR low-pass filter is a 10th-order elliptic filter with a passband edge at 3.70 kHz and a stopband attenuation of 65 dB at 4 kHz. This filter has the following specifications:

Filter type:	10th-order low-pass elliptic IIR
Sample frequency:	40.0 kHz
Passband cutoff:*	3.70 kHz
Passband ripple:	±0.2 dB
Stopband cutoff:	4.0 kHz
Stopband ripple:	−65.00 dB

*The passband cutoff frequency is defined to be the last point in the passband that meets the passband ripple specification.

(Note that these specifications apply only to this filter, and not to the entire DAC. The specifications can be used to perform further analysis of the exact characteristics of the filter, for example using a digital filter design software package.)

Figure 2 shows the frequency response of the IIR low-pass filter.

Passband ripple is ±0.2 dB for the combined effects of the DAC's digital filters (i.e., high-pass filter and IIR low pass of the interpolation filter) in the 300 Hz–3400 Hz passband.

Analog Smoothing Filter & Programmable Gain Amplifier
The programmable gain amplifier (PGA) can be used to adjust the output signal level by −15 dB to +6 dB. This gain is selected by bits 7–9 (OG0, OG1, OG2) of the AD28msp02's control register.

The AD28msp02's analog smoothing filter consists of a 2nd-order Sallen-Key continuous-time filter and a 3rd-order switched capacitor filter. The Sallen-Key filter has a 3 dB point at approximately 80 kHz.

Differential Output Amplifier
The AD28msp02's analog output ($VOUT_P$, $VOUT_N$) is produced by a differential output amplifier. The differential amplifier can drive loads of 2 kΩ or greater and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The output signal is dc-biased to the AD28msp02's on-chip voltage reference (V_{REF}) and can be ac-coupled directly to a load or dc-coupled to an external amplifier. Refer to "Analog Output" in the "Design Considerations" section of this data sheet for more information.

The $VOUT_P$–$VOUT_N$ outputs must be used as differential outputs; do not use either as a single-ended output.

SERIAL PORT
The AD28msp02 communicates with a host processor via the bidirectional synchronous serial port (SPORT). The SPORT is used to transmit and receive digital data and control information.

All serial transfers are 16 bits long, MSB first. Data bits are transferred at the serial clock rate (SCLK). SCLK equals the master clock frequency divided by 5. SCLK=2.6 MHz for the master clock frequency MCLK=13.0 MHz.

Host Processor Interface
The AD28msp02-to-host processor interface is shown in Figure 4.

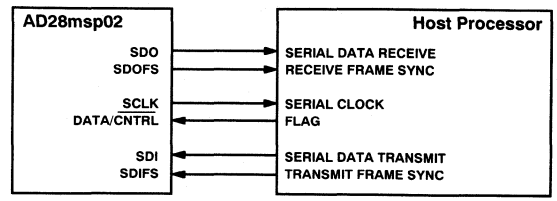


Figure 4. AD28msp02-to-Host Processor Interface

Table I describes the SPORT signals and how they are used to communicate with the host processor. The AD28msp02's chip select (CS) must be held high to enable SPORT operation. CS can be used to 3-state the SPORT pins and disable communication with the host processor.

To use the ADSP-2101 or ADSP-2111 as host DSP processor for the AD28msp02, the following connections can be used (as shown in Figure 5):

AD28msp02 Pin		ADSP-2101/2111 Pin
SCLK	—	SCLK0
SDO	—	DR0
SDOFS	—	RFS0
SDI	—	DT0
SDIFS	—	TFS0
DATA/$\overline{\text{CNTRL}}$	—	FO (Flag Output)

Table I. SPORT Signals

Signal Name	Description	Generated By	Signal State When $\overline{\text{RESET}}$ Low (CS High)	Signal State During Powerdown (CS High)
SCLK	Serial clock	AD28msp02	Low	Active
SDO	Serial data output	AD28msp02	Low	Active*
SDOFS	Serial data output frame sync	AD28msp02	Low	Low
SDI	Serial data input	Host Processor	—	—
SDIFS	Serial data input frame sync	Host Processor	—	—

(CS must be held high to enable SPORT operation.)

*Outputs last data value that was valid prior to entering powerdown.

Note that the ADSP-2101's SPORT0 communicates with the AD28msp02's SPORT while the ADSP-2101's Flag Output (FO) is used to signal the AD28msp02's DATA/$\overline{\text{CNTRL}}$ input. SPORT1 on the ADSP-2101 must be configured for flags and interrupts in this system.

Figure 6 shows an ADSP-2101 assembly language program that initializes the AD28msp02 and implements digital loopback through the DSP processor.

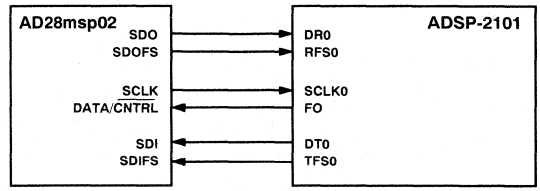


Figure 5. AD28msp02-to-ADSP-2101 Interface

```
{ This ADSP-2101 program initializes the AD28msp02 }
{ and executes a loopback, or talk-through, routine. }

.MODULE/ABS=0/BOOT=0    test1;

resetv:     JUMP begin;             {restart}
            RTI; RTI; RTI;
irq2v:      RTI; RTI; RTI; RTI;     {IRQ2}
st0x:       RTI; RTI; RTI; RTI;     {SPORT0 Tx}
sr0x:       ax0 = rx0;              {SPORT0 Rx}
            tx0 = ax0;
            RTI; RTI;
irq1v:      RTI; RTI; RTI; RTI;     {irq1}
irq0v:      RTI; RTI; RTI; RTI;     {irq0}
timerv:     RTI; RTI; RTI; RTI;

begin:      RESET FLAG_OUT;
            AX0 = 0x2A0F;           {Configure ADSP-2101 SPORT0 for }
            DM (0x3FF6) = AX0;      { ext. SCLK, ext. RFS, int. TFS }

            AX0 = 0x101F;           { Enable ADSP-2101 SPORT0,    }
            DM (0x3FFF) = AX0;      { configure SPORT1 for Flag Out }

            IMASK = 0x10;
            AX0 = 0x30;             { Write control word to take}
            TX0 = AX0;              { AD28msp02 out of powerdown }

            IDLE;
            NOP;
            IMASK = 0x08;
            SET FLAG_OUT;
wait:       JUMP wait;              { Wait for receive interrupt }
            NOP;
.ENDMOD;
```

Figure 6. ADSP-2101 Digital Loopback Routine

Serial Data Output
The AD28msp02's SPORT will begin transmitting data to the host processor at an 8 kHz rate when the PWDD and PWDA bits (Bits 4, 5) of the control register are set to 1. In the program shown in Figure 6, the instructions

AX0 = 0x30; { *Write control word to take* }
TX0 = AX0; { *AD28msp02 out of powerdown* }
accomplish this by writing 0x30 to the AD28msp02's control register. There is a short startup time (after the end of this control register write) before the AD28msp02 raises SDOFS and begins transmitting data; see Figure 11.

At the 13 MHz MCLK frequency, data is transmitted at an 8 kHz rate with a single 16-bit word transmitted every 125 μs. While data is being output, the AD28msp02 asserts SDOFS at an 8 kHz rate. Each 16-bit word transfer begins one serial clock cycle after SDOFS is asserted.

Serial Data Input
The host processor must initiate data transfers to the AD28msp02 by asserting the serial data input frame sync (SDIFS) high. The 16-bit word transfer begins one serial clock cycle after SDIFS is asserted. The DATA/CNTRL line must be driven high when SDIFS is driven high.

The host processor must assert SDIFS shortly after the rising edge of SCLK and must maintain SDIFS high for one cycle. Data is then driven from the host processor (to the SDI input) shortly after the rising edge of the next SCLK and is clocked into the AD28msp02 on the falling edge of SCLK in that cycle.

Each bit of a 16-bit data word is thus clocked into the AD28msp02 on the falling edge of SCLK (MSB first).

If SDIFS is asserted high again before the end of the present data word transfer, it is not recognized until the falling edge of SCLK in the last (LSB) cycle.

(Note: Exact SPORT timing requirements are defined in the "Specifications" section of this data sheet.)

CONTROL REGISTER
The AD28msp02's control register configures the device for various modes of operation including ADC and DAC gain settings, ADC input mux selection, filter bypass, and powerdown. The AD28msp02's host processor can read and write to the control register through the AD28msp02's serial port (SPORT) by driving the DATA/$\overline{\text{CNTRL}}$ pin low.

The control register is cleared (set to 0x0000) when the AD28msp02 is reset.

Control Register Writes
To write the control register, the host processor must assert DATA/$\overline{\text{CNTRL}}$ low when it asserts SDIFS. If the MSB of the bit stream is also low, the SPORT recognizes the incoming serial data as a new control word and copies it to the AD28msp02's control register. The format for the control word write is shown in Table II; reserved Bits 10–15 must be set to zero.

Table II. Control Word Write Format

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	OG2	OG1	OG0	0	PWDD	PWDA	ADBY	DABY	IMS	IPS

0	IPS	Analog input preamplifier select: 1 = insert (+20 dB), 0 = bypass (0 dB)
1	IMS	Analog input multiplexer select: 1 = AUX input, 0 = NORM input
2	DABY	DAC high-pass filter bypass select: 0 = insert, 1 = bypass
3	ADBY	ADC high-pass filter bypass select: 0 = insert, 1 = bypass
4	PWDA	Powerdown analog: 0 = powerdown, 1 = operating
5	PWDD	Powerdown digital: 0 = powerdown, 1 = operating
7–9	OG2–OG0	Analog output gain setting (for D/A output PGA)
10–15		Reserved

Gain	OG2	OG1	OG0
+6 dB	0	0	0
+3 dB	0	0	1
0 dB	0	1	0
−3 dB	0	1	1
−6 dB	1	0	0
−9 dB	1	0	1
−12 dB	1	1	0
−15 dB	1	1	1

Gain settings are accurate within ±0.6 dB.

(Control Register is set to 0x0000 at RESET. Reserved Bits 10–15 must be set to 0 for all Control Register writes.)

Table III. Control Word Read Format

Read Request

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Read Ready

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

3

Control Register Reads

To read the control register, the host processor must transfer two control words. For each transfer, the DATA/$\overline{\text{CNTRL}}$ pin must be low when SDIFS is asserted. If the MSB of the bit stream is high, the SPORT recognizes the incoming serial data as a request for control information. The protocol for reading the control register is as follows:

1. The host processor sends a "Read Request" control word to the AD28msp02. Since the MSB of this control word is high, the SPORT recognized the incoming serial data as a read request and does not overwrite the control register.
2. When the AD28msp02 receives the read request, it finishes any data transfers in progress and waits for a "Read Ready" control word.
3. The host processor then transfers a "Read Ready" control word to the AD28msp02. Upon receiving this control word, the AD28msp02 transfers the control register contents to the host processor via the SPORT.
4. When the SPORT completes the control register transfer, it immediately resumes transmitting data at an 8 kHz rate.

This scheme allows any data transfers in progress to be completed and resolves any ambiguities between data and control words. The format for the read control words is shown in Table III.

DESIGN CONSIDERATIONS

Analog Input

The analog input signal to the AD28msp02 must be ac-coupled. Figure 7 shows the recommended input circuit for the AD28msp02's analog input pin (either VIN_{NORM} or VIN_{AUX}). The circuit of Figure 7 implements a first-order low-pass filter with a 3 dB point at 20 kHz; this is the only filter that must be implemented external to the AD28msp02 to prevent aliasing of the sampled signal. Since the AD28msp02's ADC uses a highly oversampled approach that transfers the bulk of the anti-aliasing filtering into the digital domain, the off-chip anti-aliasing filter need only be of low order.

In the circuit shown in Figure 7, scaling of the analog input is achieved by the resistors R_{IN} and R_{FB}. The input signal gain, $-R_{FB}/R_{IN}$, can be adjusted from −12 dB to +26 dB by varying the values of these resistors. The AD28msp02's on-chip 20 dB preamplifier can be enabled when there is not enough gain in the input circuit; the preamplifier is configured by Bit 0 (IPS) of the control register. Total gain must be configured to ensure that a full-scale input signal (at C_{IN} in Figure 7) produces a signal level at the input to the sigma-delta modulator of the ADC that does not exceed V_{INMAX}, which is specified under "Analog Interface Electrical Characteristics." If the total gain is increased above unity, signal-to-noise (SNR + THD) performance will not meet the listed specifications.

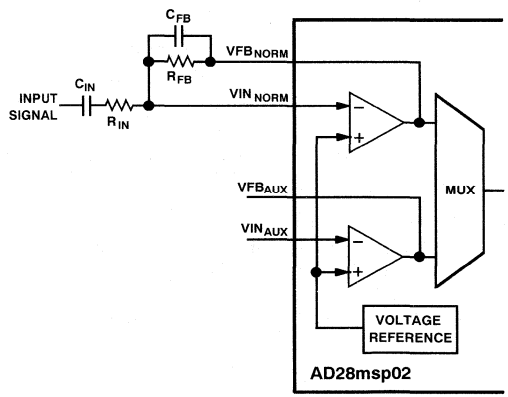


Figure 7. Recommended Analog Input Circuit

The dc biasing of the analog input signal is accomplished with an on-chip voltage reference which nominally equals 2.5 V. The input signal must be ac-coupled with an external coupling capacitor (C_{IN}). C_{IN} and R_{IN} should be chosen to ensure a coupling corner frequency of 30 Hz. C_{IN} should be 0.1 μF or larger.

To select values for the components shown in Figure 7, use the following equations:

$$Gain = -\frac{R_{FB}}{R_{IN}}$$

$$C_{IN} = \frac{1}{60\pi R_{IN}}$$

$$C_{FB} = \frac{1}{(2\pi)(20 \times 10^3)R_{FB}}$$

$10\ k\Omega \leq R_{FB}, R_{IN} \leq 50\ k\Omega$
$150\ pF \leq C_{FB} \leq 600\ pF$

Figure 8 shows an example of a typical input circuit configured for 0 dB gain. The circuit's diodes are used to prevent the input signal from exceeding maximum limits.

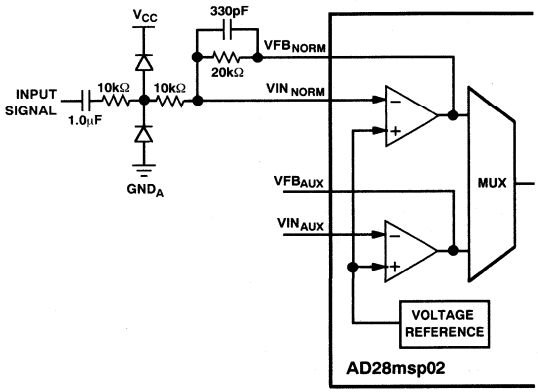


Figure 8. Example Analog Input Circuit for 0 dB Gain

Analog Output

The AD28msp02's differential analog output ($VOUT_P$,$VOUT_N$) is produced by an on-chip differential amplifier. The differential amplifier can drive a minimum load of 2 kΩ ($R_L \geq 2\ k\Omega$) and has a maximum differential output voltage swing of ±3.156 V peak-to-peak (3.17 dBm0). The differential output can be ac-coupled directly to a load or dc-coupled to an external amplifier.

Figure 9 shows a simple circuit providing a differential output with ac coupling. The capacitor of this circuit (C_{OUT}) is optional; if used, its value can be chosen as follows:

$$C_{OUT} = \frac{1}{(60\pi)R_L}$$

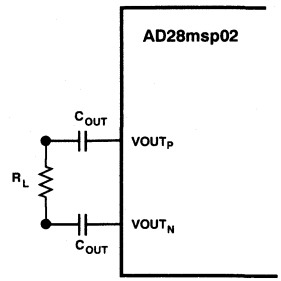


Figure 9. Example Circuit for Differential Output

The $VOUT_P$–$VOUT_N$ outputs must be used as differential outputs; do not use either as a single-ended output. Figure 10 shows an example circuit which can be used to convert the differential output to a single-ended output. The circuit uses a differential-to-single-ended amplifier, the Analog Devices SSM-2141.

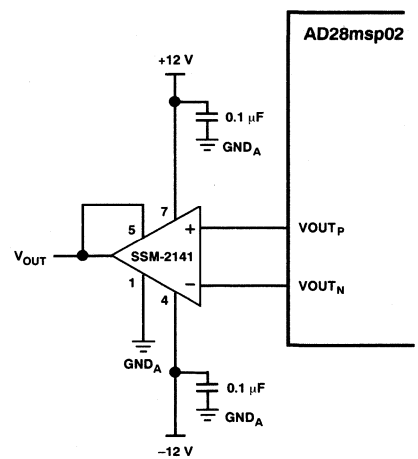


Figure 10. Example Circuit for Single-Ended Output

Serial Output Startup Time

The AD28msp02 begins transmitting data to the host processor after it is taken out of powerdown. To take the AD28msp02 out of powerdown, the host processor writes a control word to the AD28msp02.

The startup time (from the start of this control word write) before the AD28msp02 begins transmitting data is shown in Figure 11.

PC Board Layout Considerations

Separate analog and digital ground planes should be provided for the AD28msp02 in order to ensure the characteristics of the device's ADC and DAC. The two ground planes should be connected at a single point—this is often referred to as a "Star" or "Mecca" grounding configuration. The point of connection may be at the system power supply, at the PC board power connection, or at any other appropriate location. Because ground loops increase susceptibility to EMF, multiple connections between the analog and digital ground planes should be avoided.

The ground planes should be designed such that all noise-sensitive areas are isolated from one another and critical signal traces (such as digital clocks and analog signals) are as short as possible.

Each +5 V digital supply pin, V_{DD}, of the AD28msp02 (SOIC Pins 20, 21) should be bypassed to ground with a 0.1 μF capacitor. These capacitors should be low inductance, monolithic, ceramic, and surface-mount. The capacitor leads and PC board traces should be as short as possible to minimize inductive effects. In addition, a 10 μF capacitor should be connected between V_{DD} and ground, near the PC board power connection.

MCLK Frequency

The sigma-delta converters and digital filters of the AD28msp02 are specifically designed to operate at a master clock (MCLK) frequency of 13.0 MHz. MCLK must equal 13.0 MHz to guarantee the filter characteristics and sample rate of the ADC and DAC. The AD28msp02 is not tested or characterized at any other clock frequency.

A low cost crystal with a different frequency, for example 12.288 MHz, can be used for the master clock input; in this case, however, the AD28msp02 is not guaranteed to meet the specifications listed in this data sheet.

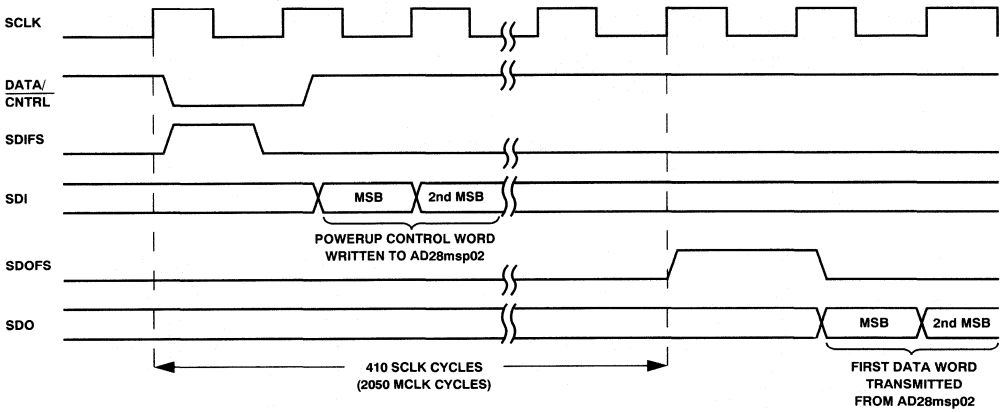


Figure 11. Serial Output Startup Time

DEFINITION OF SPECIFICATIONS

Absolute Gain

Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured with a 1.0 kHz sine wave at 0 dBm0. The absolute gain specification is used as a reference for gain tracking error specification.

Gain Tracking Error

Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 1 kHz at 0 dBm0 (equal to absolute gain). Gain tracking error at 0 dBm0 is 0 dB by definition.

SNR + THD

Signal-to-noise ratio plus total harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300–3400 Hz, including harmonics but excluding dc.

Intermodulation Distortion

With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m or n are equal to zero. For final testing, the second order terms include (fa + fb) and (fa − fb), while the third order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

Idle Channel Noise

Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300–3400 Hz).

Crosstalk

Crosstalk is defined as the ratio of the amplitude of a full-scale signal appearing on one channel to the amplitude of the same signal which couples onto the adjacent channel. Crosstalk is expressed in dB.

Power Supply Rejection

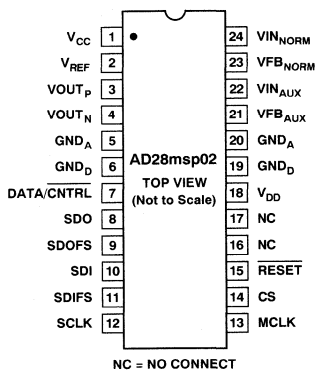
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Group Delay

Group delay is defined as the derivative of radian phase with respect to radian frequency, $\partial\phi(\omega)/\partial\omega$. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay away from a constant indicates the degree of nonlinear phase response of the system.

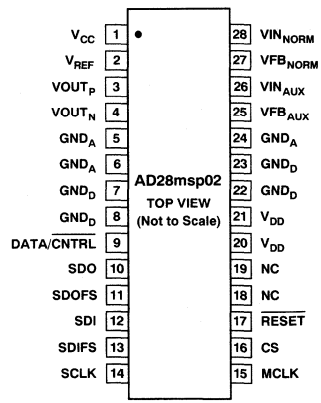
PIN CONFIGURATIONS

24-Pin DIP



NC = NO CONNECT

28-Lead SOIC



NC = NO CONNECT

SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

Parameter		K Grade Min	K Grade Max	B Grade Min	B Grade Max	Unit
V_{DD}, V_{CC}	Supply Voltage	4.50	5.50	4.50	5.50	V
T_{AMB}	Ambient Operating Temperature	0	+70	−40	+85	°C

Refer to Environmental Conditions for information on case temperature and thermal specifications.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . −0.3 V to +7 V
Input Voltage . . . . . −0.3 V to V_{DD} + 0.3 V
Output Voltage Swing . . . . . −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range (Ambient) . . . −40°C to +85°C
Storage Temperature Range . . . . . −55°C to +150°C
Lead Temperature (5 seconds) SOIC . . . . . +280°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections o f this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD SENSITIVITY

The AD28msp02 features proprietary input protection circuitry to dissipate high-energy discharges (Human Body Model). Per method 3015 of MIL-STD-883C, the AD28msp02 has been classified as a Class 1 device.

Proper ESD precautions are strongly recommended to avoid functional damage or performance degradation. Charges readily accumulate on the human body and test equipment and discharge without detection. Unused devices must be stored in conductive foam or shunts, and the foam should be discharged to the destination socket before devices are removed.

DIGITAL INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IH}	Input High Voltage	2.4			V	V_{DD} = max
V_{IL}	Input Low Voltage			0.8	V	V_{DD} = min
V_{OH}	Output High Voltage	2.4			V	V_{DD} = min, I_{OH} = −0.5 mA
V_{OL}	Output Low Voltage			0.4	V	V_{DD} = min, I_{OL} = 2 mA
I_{IH}	High Level Input Current			10	μA	V_{DD} = max, V_{IN} = max
I_{IL}	Low Level Input Current			10	μA	V_{DD} = max, V_{IN} = 0 V
I_{OZL}	Low Level Output 3-State Leakage Current			10	μA	V_{DD} = max, V_{IN} = max
I_{OZH}	High Level Output 3-State Leakage Current			10	μA	V_{DD} = max, V_{IN} = 0 V
C_I	Digital Input Capacitance			10	pF	

ANALOG INTERFACE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Unit
ADC:					
I_L	Input Leakage Current at VIN_{NORM}, VIN_{AUX}		10		nA
R_I	Input Resistance[4] at VIN_{NORM}, VIN_{AUX}		100		MΩ
C_{IL}	Input Load Capacitance[4] at VFB_{NORM}, VFB_{AUX}		10		pF
VIN_{MAX}	Maximum Input Range[1]			3.156	V p–p
DAC:					
R_O	Output Resistance[2, 4]		1		Ω
V_{OOFF}	Output DC Offset[3]			400	mV
C_{OL}	Output Load Capacitance[2]			100	pF
V_{VREF}	Voltage Reference (V_{REF})	2.25		2.75	V
V_O	Maximum Voltage Output Swing (p–p) Across R_L				
	Single-Ended			3.156	V
	Differential			6.312	V
R_L	Load Resistance[2]	2			kΩ

Test Conditions for all analog interface tests: Unity input gain, A/D 20 dB preamplifier bypassed, D/A PGA set for 0 dB gain, no load on analog output ($VOUT_P$–$VOUT_N$).

[1]At input to sigma-delta modulator of ADC.
[2]At $VOUT_P$–$VOUT_N$.
[3]Between $VOUT_P$ and $VOUT_N$.
[4]Guaranteed but not tested.

POWER DISSIPATION

Symbol	Parameter	Min	Max	Unit
V_{CC}	Analog Operating Voltage	4.5	5.5	V
V_{DD}	Digital Operating Voltage	4.5	5.5	V
I_{DD}	Operating Current Active[1]		40	mA
P_I	Power Dissipation Active[1]		200	mW
I_{DD}	Operating Current Inactive[2]		0.5	mA
P_0	Power Dissipation Inactive[2]		2.5	mW

Test conditions: V_{DD} = V_{CC} = 5.0 V, MCLK frequency 13.0 MHz, no load on digital pins, analog inputs ac-coupled to ground, no load on analog output ($VOUT_P$–$VOUT_N$).

[1]Active: AD28msp02 operational (PWDD and PWDA set to 1 in control register).
[2]Inactive: AD28msp02 in powerdown state (PWDD and PWDA set to 0 in control register) and MCLK tied to V_{DD}.

TIMING PARAMETERS

Clock Signals

Parameter		Min	Max	Unit
Timing Requirement:				
t_{MCK}	MCLK Period	76.9	76.9	ns
t_{MKL}	MCLK Width Low	$0.5t_{MCK} - 10$	$0.5t_{MCK} + 10$	ns
t_{MKH}	MCLK Width High	$0.5t_{MCK} - 10$	$0.5t_{MCK} + 10$	ns
Switching Characteristic:				
t_{SCK}	SCLK Period	$5t_{MCK}$		ns
t_{SKL}	SCLK Width Low	$3t_{MCK} - 10$	$3t_{MCK} + 10$	ns
t_{SKH}	SCLK Width High	$2t_{MCK} - 10$	$2t_{MCK} + 10$	ns

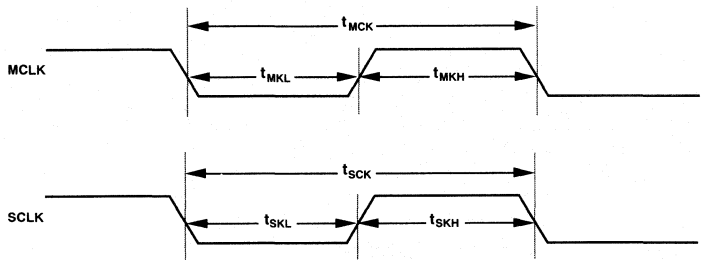


Figure 12. Clock Signals

Serial Port 3-State

Parameter		Min	Max	Unit
Switching Characteristic:				
t_{SPD}	CS Low to SDO, SDOFS, SCLK Disable		25	ns
t_{SPE}	CS High to SDO, SDOFS, SCLK Enable	0		ns
t_{SPV}	CS High to SDO, SDOFS, SCLK Valid		10	ns

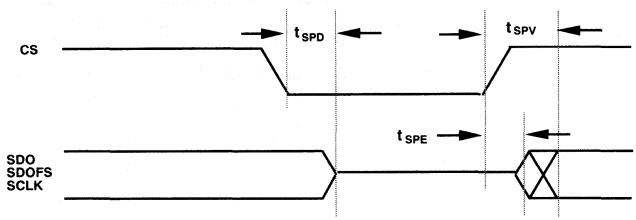


Figure 13. Serial Port 3-State

Serial Ports

Parameter		Min	Max	Unit
Timing Requirement:				
t_{SCS}	SDI/SDIFS Setup before SCLK Low	10		ns
t_{SCH}	SDI/SDIFS Hold after SCLK Low	10		ns
t_{DCS}	DATA/$\overline{\text{CNTRL}}$ Setup before SCLK Low	10		ns
t_{DCH}	DATA/$\overline{\text{CNTRL}}$ Hold after SCLK Low	10		ns
Switching Characteristic:				
t_{RD}	SDOFS Delay from SCLK High		15	ns
t_{RH}	SDOFS Hold after SCLK High	0		ns
t_{SCDH}	SDO Hold after SCLK High	0		ns
t_{SCDD}	SDO Delay from SCLK High		30	ns

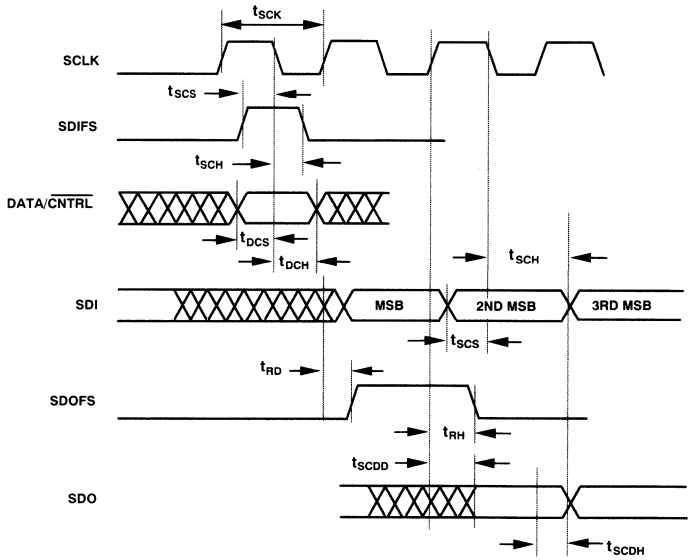


Figure 14. Serial Ports

DIGITAL TEST CONDITIONS

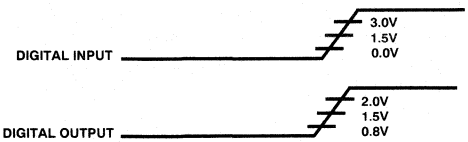


Figure 15. Voltage Reference Levels for AC Measurements

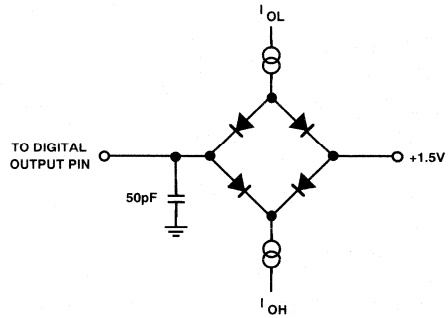


Figure 16. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

3

GAIN

Parameter	Min	Typ	Max	Unit	Test Conditions
ADC Absolute Gain	−0.2	0	0.2	dBm0	1.0 kHz, 0 dBm0
ADC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0
DAC Absolute Gain	−0.2	0	0.2	dBm0	1.0 kHz, 0 dBm0
DAC Gain Tracking Error	−0.1	0	0.1	dBm0	1.0 kHz, +3 to −50 dBm0

FREQUENCY RESPONSE

Input Freq (Hz)	Min Output (dB)	Max Output (dB)
0	−∞	−25
100	−∞	−25
150	−0.3	+0.3
200	−0.3	+0.3
300	−0.2	+0.2
1000	−0.2	+0.2
2000	−0.2	+0.2
3000	−0.2	+0.2
3400	−0.2	+0.2
3700	−0.3	+0.3
4000	−∞	−60
>4000	−∞	−60

Frequency responses of ADC and DAC measured with input at audio reference level (the input level that produces an output level of −10 dBm0), with 20 dB preamplifier bypassed and input gain of 0 dB. The in-band ripple shall not exceed 0.2 dB.

NOISE AND DISTORTION

Parameter	Min	Max	Unit	Test Conditions
ADC Intermodulation Distortion		−70	dB	
DAC Intermodulation Distortion		−70	dB	
ADC Idle Channel Noise		72	dBm0	
DAC Idle Channel Noise		72	dBm0	
ADC Crosstalk		−65	dB	ADC input signal level: 1.0 kHz, 0 dBm0 DAC input at idle.
DAC Crosstalk		−65	dB	ADC input signal level: analog ground DAC output signal level: 1.0 kHz, 0 dBm0
ADC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
DAC Power Supply Rejection		−55	dB	Input signal level at V_{CC} and V_{DD} pins: 1.0 kHz, 100 mV p–p sine wave
ADC Group Delay[1]		1	ms	300−3000 Hz
DAC Group Delay[1]		1	ms	300−3000 Hz

[1]Guaranteed but not tested.

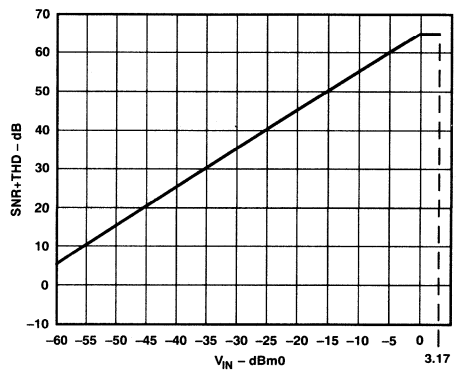


Figure 17. SNR+THD vs. V_{IN}

ORDERING GUIDE

Part Number	Temperature Range	Package	Package Option*
AD28msp02KN	0°C to +70°C	24-Pin Plastic DIP	N-24
AD28msp02KR	0°C to +70°C	28-Lead SOIC	R-28
AD28msp02BN	−40°C to +85°C	24-Pin Plastic DIP	N-24
AD28msp02BR	−40°C to +85°C	28-Lead SOIC	R-28

*N = Plastic DIP, R = Small Outline (SOIC). For outline information see Package Information section.

Sound Processing Products, Digital Audio
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Introduction

Analog Devices is a world leading supplier of IC products for digital audio applications. The digital audio components offered by Analog Devices include digital-to-analog converters (DACs), analog-to-digital converters (ADCs), and SamplePort® asynchronous sample rate converters (ASRCs). These components are suitable for equipment designed for the professional audio market, the "pro-sumer" audio market, and the consumer audio market, as well as for high performance computer audio designs and digital audio communications system designs. The resolutions of these converters ranges from 16 bits to 20 bits, allowing the designer to choose the appropriate level of performance for the application. The DACs, ADCs and ASRCs are offered in a variety of through-hole and surface mount packages so that low volume and high volume OEMs can select the package types that are compatible with their production equipment. These digital audio products are manufactured in a variety of process technologies; all new products are fabricated in standard CMOS, enabling Analog Devices to price these components aggressively, and ensuring customers access to high volume supplies. Technical support for these components is provided by Analog Devices' Field Applications engineers deployed worldwide, as well as by the Factory Applications staff of the Computer Products Division. Analog Devices is committed to total quality management, and this commitment is reflected in these products. Many of the digital audio IC models are manufactured and tested at Analog's Wilmington, Massachusetts manufacturing site, which is ISO 9001 certified.

Audio DACs

Analog Devices offers a comprehensive selection of multi-bit audio DACs, from stereo, 16-bit, +5 V supply (the AD1866) to mono, 20-bit, ±5 V supply (the AD1862). These DACs integrate the serial-to-parallel digital input interface, voltage reference, DAC and voltage output amplifier (except the AD1862) functions, and they all support oversampling operation up to 16 times F_S using external interpolation filters. They are characterized by a "partially segmented" architecture in which the LSBs are segmented into elements and the LSBs are produced using an R-2R network. The segment and R-2R silicon chromium thin-film resistors are laser trimmed to provide low harmonic distortion. Various advanced techniques, such as digital midscale offset, on-chip analog noise reduction capacitors, and low stress packaging, together result in sonically superior products. The on-chip voltage output amplifiers are designed to achieve fast settling times and high slew rates, and reduce the need for external components. The +5 V supply DACs dissipate 50 mW typically, and will continue to operate with a reduced supply voltage, making them suitable for battery powered systems.

Audio ADCs

Analog Devices is a pioneer in the development and application of sigma-delta data conversion technology. The AD1879 was the world's first single package 18-bit audio ADC. The AD1879 and AD1878 (a 16-bit version of the AD1879) employ an advanced, fifth-order, 64 times oversampling sigma-delta modulator and a single stage, 4096 tap digital decimation filter. The AD1879 achieves a typical 103 dB signal-to-noise ratio and –98 dB THD+N. The ADMOD79 is the modulator portion of the AD1879 packaged separately for designers who wish to construct their own high performance ADC system. The AD1877 is a low cost, high performance 16-bit sigma-delta ADC that requires only a single +5 V supply. The AD1877 uses a fourth-order, 64 times oversampling modulator, with a three-stage FIR decimation filter. Its input structure is single ended, and the serial digital output interface offers eight pin-selectable modes, which equates to ease of use for the designer. The AD1877 requires a minimum of external components, which means that the total installed cost is lower than that of competitive products.

SamplePort is a registered trademark of Analog Devices, Inc.

Audio DAC Selection Guide

Model	Bits	Channels	SNR (typ)	THD+N (typ)	Supply	Power (typ)	Pins
AD1851	16	Single	110 dB	0.003%	±5 V	100 mW	16
AD1861	18	Single	110 dB	0.003%	±5 V	100 mW	16
AD1862	20	Single	119 dB	0.0012%	±5 V to ±12 V	288 mW	16
AD1865	18	Dual	110 dB	0.0017%	±5 V	225 mW	24/28
AD1866	16	Dual	95 dB	0.005%	+5 V	45 mW	16
AD1868	18	Dual	97.5 dB	0.004%	+5 V	50 mW	16

Audio ADC Selection Guide

Model	Bits	Type	Channels	SNR (typ)	THD+N (typ)	Input	Supply	Power (typ)	Pins
AD1877	16	ΣΔ	Stereo	92 dB	–90 dB	Single Ended	+5 V	255 mW	28
AD1878	16	ΣΔ	Stereo	97 dB	–95 dB	Differential	±5 V	1130 mW	28
AD1879	18	ΣΔ	Stereo	103 dB	–98 dB	Differential	±5 V	1130 mW	28
ADMOD79	N/A	ΣΔ	Stereo	103 dB	–98 dB	Differential	±5 V	845 mW	28

Audio SamplePorts

Analog Devices is the world leader in IC sample rate conversion technology. The 20-bit AD1890 was the world's first monolithic IC solution for Asynchronous Sample Rate Conversion (ASRC). The 16-bit AD1893 takes this same high quality digital-to-digital conversion algorithm into the lower cost consumer and "pro-sumer" price range. These ASRCs all offer sample clock jitter rejection, a wide 1:2 to 2:1 ratio between the input and output sample clocks, and the ability to track dynamically changing sample clocks. The AD1893 adds an on-chip oscillator, a right-justified serial-port mode, a power-down mode, and performance specified at 3 V. The AD1890 and the 16-bit AD1891 are offered in PDIP and PLCC packages; the AD1893 is offered in PDIP and TQPP packages.

Audio SamplePort Selection Guide

Model	Bits	SNR (typ)	THD+N (typ @ 1 kHz)	Supply	Power (typ @ 3 V)	Pins
AD1890	20	120 dB	106 dB	2.7 V to 5.5 V	57 mW	28
AD1891	16	96 dB	–96 dB	2.7 V to 5.5 V	57 mW	28
AD1893	16	96 dB	–96 dB	2.7 V to 5.5 V	45 mW	28/44

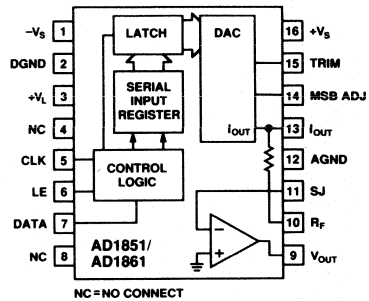
16-Bit/18-Bit, 16× F_S PCM Audio DACs

AD1851/AD1861

FEATURES
110 dB SNR
Fast Settling Permits 16× Oversampling
±3 V Output
Optional Trim Allows Super-Linear Performance
±5 V Operation
16-Pin Plastic DIP and SOIC Packages
Pin-Compatible with AD1856 & AD1860 Audio DACs
2s Complement, Serial Input

APPLICATIONS
High-End Compact Disc Players
Digital Audio Amplifiers
DAT Recorders and Players
Synthesizers and Keyboards

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD1851/AD1861 is a monolithic PCM audio DAC. The AD1851 is a 16-bit device, while the AD1861 is an 18-bit device. Each device provides a voltage output amplifier, DAC, serial-to-parallel register and voltage reference. The digital portion of the AD1851/AD1861 is fabricated with CMOS logic elements that are provided by Analog Devices' 2 μm ABCMOS process. The analog portion of the AD1851/AD1861 is fabricated with bipolar and MOS devices as well as thin-film resistors.

This combination of circuit elements, as well as careful design and layout techniques, results in high performance audio playback. Laser-trimming of the linearity error affords low total harmonic distortion. An optional linearity trim pin is provided to allow residual differential linearity error at midscale to be eliminated. This feature is particularly valuable for low distortion reproductions of low amplitude signals. Output glitch is also small, contributing to the overall high level of performance. The output amplifier achieves fast settling and high slew rates, providing a full ±3 V signal at load currents up to 8 mA. When used in current output mode, the AD1851/AD1861 provides a ±1 mA output signal. The output amplifier is short circuit protected and can withstand indefinite shorts to ground.

The serial input interface consists of the clock, data and latch enable pins. The serial 2s complement data word is clocked into the DAC, MSB first, by the external clock. The latch enable signal transfers the input word from the internal serial input register to the parallel DAC input register. The AD1851 input clock can support a 12.5 MHz data rate, while the AD1861 input clock can support a 13.5 MHz data rate. This serial input port is compatible with second generation digital filter chips used in consumer audio products. These filters operate at oversampling rates of 2×, 4×, 8× and 16× sampling frequencies.

The critical specifications of THD+N and signal-to-noise ratio are 100% tested for all devices.

The AD1851/AD1861 operates with ±5 V power supplies, making it suitable for home use markets. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital crosstalk. Separate analog and digital ground pins are also provided. Power dissipation is 100 mW typical.

The AD1851/AD1861 is available in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Both packages incorporate the industry standard pinout found on the AD1856 and AD1860 PCM audio DACs. As a result, the AD1851/AD1861 is a drop-in replacement for designs where ±5 V supplies have been used with the AD1856/AD1860. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

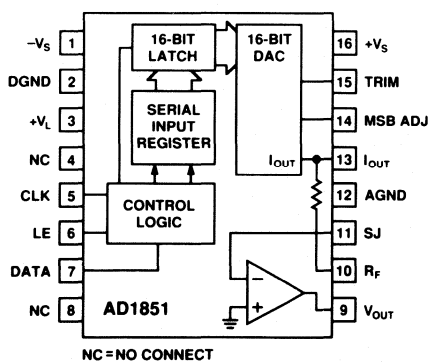
1. AD1851 16-bit resolution provides 96 dB dynamic range. AD1861 18-bit resolution provides 108 dB dynamic range.
2. No external components are required.
3. Operates with ±5 V supplies.
4. Space saving 16-pin SOIC and plastic DIP packages.
5. 100 mW power dissipation.
6. High input clock data rates and 1.5 μs settling time permits 2×, 4×, 8× and 16× oversampling.
7. ±3 V or ±1 mA output capability.
8. THD + Noise and SNR are 100% tested.
9. Pin-compatible with AD1856 & AD1860 PCM audio DACs.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

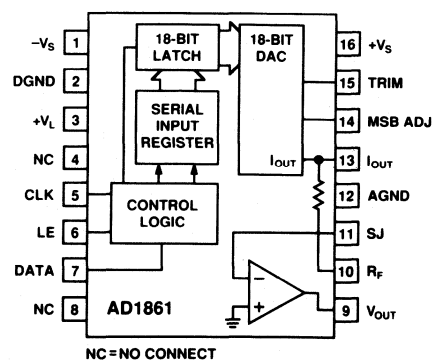
AD1851/AD1861 —SPECIFICATIONS (T_A @ +25°C and ±5 V supplies, unless otherwise noted)

	Min	Typ	Max	Units
DIGITAL INPUTS				
V_{IH}	2.0		$+V_L$	V
V_{IL}			0.8	V
I_{IH}, $V_{IH} = V_L$			**1.0**	μA
I_{IL}, $V_{IL} = 0.4$			**−10**	μA
ACCURACY				
Gain Error		±1		%
Midscale Output Voltage		±10		mV
DRIFT (0°C to +70°C)				
Total Drift		±25		ppm of FSR/°C
Bipolar Zero Drift		±4		ppm of FSR/°C
SETTLING TIME (To ±0.0015% of FSR)				
Voltage Output				
6 V Step		1.5		μs
1 LSB Step		1.0		μs
Slew Rate		9		V/μs
Current Output				
1 mA Step 10 Ω to 100 Ω Load		350		ns
1 kΩ Load		350		ns
OUTPUT				
Voltage Output Configuration				
Bipolar Range	**±2.88**	±3.0	**±3.12**	V
Output Current	±8			mA
Output Impedance		0.1		Ω
Short Circuit Duration		Indefinite to Common		
Current Output Configuration				
Bipolar Range (±30%)		±1.0		mA
Output Impedance (±30%)		1.7		kΩ
POWER SUPPLY				
Voltage				
$+V_L$ and $+V_S$	4.75		5.25	V
$-V_S$	−5.25		−4.75	V
TEMPERATURE RANGE				
Specification	0	+25	+70	°C
Operation	−25		+70	°C
Storage	−60		+100	°C
WARMUP TIME	1			min

Specifications subject to change without notice.



AD1851 Functional Block Diagram



AD1861 Functional Block Diagram

AD1851

	Min	Typ	Max	Units
RESOLUTION			16	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1851N-J, R-J		0.003	0.004	%
AD1851N, R		0.004	0.008	%
−20 dB, 990.5 Hz				
AD1851N-J, R-J		0.009	0.016	%
AD1851N, R		0.009	0.040	%
−60 dB, 990.5 Hz				
AD1851N-J, R-J		0.9	1.6	%
AD1851N, R		0.9	4.0	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1851N, R	88			dB
AD185IN-J, R-J	96			dB
SIGNAL-TO-NOISE RATIO	107	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	12.5			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		14		Bits
POWER SUPPLY				
Current				
+I		10.0	13.0	mA
−I		−10.0	−15.0	mA
Power Dissipation		100		mW

AD1861

	Min	Typ	Max	Units
RESOLUTION			18	Bits
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz				
AD1861N-J, R-J		0.003	0.004	%
AD1861N, R		0.004	0.008	%
−20 dB, 990.5 Hz				
AD1861N-J, R-J		0.009	0.016	%
AD1861N, R		0.009	0.040	%
−60 dB, 990.5 Hz				
AD1861N-J, R-J		0.9	1.6	%
AD1861N, R		0.9	4.0	%
D-RANGE* (With A-Weight Filter)				
−60 dB, 990.5 Hz AD1861N, R	88			dB
AD186IN-J, R-J	96			dB
SIGNAL-TO-NOISE RATIO	107	110		dB
MAXIMUM CLOCK INPUT FREQUENCY	13.5			MHz
ACCURACY				
Differential Linearity Error		±0.001		% of FSR
MONOTONICITY		15		Bits
POWER SUPPLY				
Current				
+I		10.0	13.0	mA
−I		−10.0	−15.0	mA
Power Dissipation		100		mW

*Tested in accordance with EIAJ Test Standard CP-307.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 V to 6.50 V
V_S to AGND . . . . . 0 V to 6.50 V
$-V_S$ to AGND . . . . . −6.50 V to 0 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
AGND to DGND . . . . . ±0.3 V
Short Circuit . . . . . Indefinite Short to Ground
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENTS

1	$-V_S$	ANALOG NEGATIVE POWER SUPPLY
2	DGND	LOGIC GROUND
3	V_L	LOGIC POSITIVE POWER SUPPLY
4	NC	NO CONNECTION
5	CLK	CLOCK INPUT
6	LE	LATCH ENABLE INPUT
7	DATA	SERIAL DATA INPUT
8	NC	NO INTERNAL CONNECTION*
9	V_{OUT}	VOLTAGE OUTPUT
10	R_F	FEEDBACK RESISTOR
11	SJ	SUMMING JUNCTION
12	AGND	ANALOG GROUND
13	I_{OUT}	CURRENT OUTPUT
14	MSB ADJ	MSB ADJUSTMENT TERMINAL
15	TRIM	MSB TRIMMING POTENTIOMETER TERMINAL
16	V_S	ANALOG POSITIVE POWER SUPPLY

*PIN 8 HAS NO INTERNAL CONNECTION; $-V_L$ FROM AD1856 OR AD1860 SOCKET CAN BE SAFELY APPLIED.

CAUTION

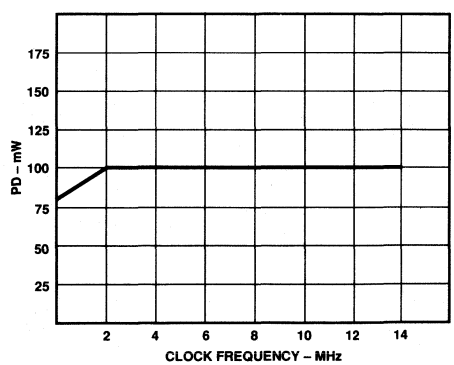
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

ORDERING GUIDE

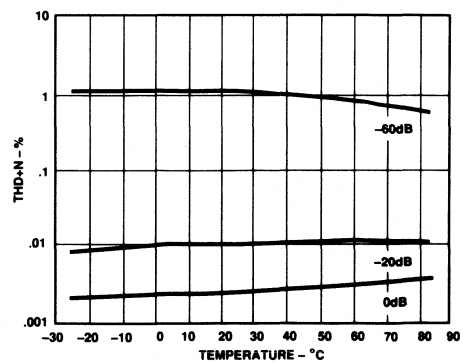
Model	Resolution	THD+N	Package Option*
AD1851N	16 Bits	0.008%	N-16
AD1851N-J	16 Bits	0.004%	N-16
AD1851R	16 Bits	0.008%	R-16
AD1851R-J	16 Bits	0.004%	R-16
AD1861N	18 Bits	0.008%	N-16
AD1861N-J	18 Bits	0.004%	N-16
AD1861R	18 Bits	0.008%	R-16
AD1861R-J	18 Bits	0.004%	R-16

*N = Plastic DIP Package; R = Small Outline (SOIC) Package.
For outline information see Package Information section.

Typical Performance



Power Dissipation vs. Clock Frequency



THD vs. Temperature

Stereo, Single-Supply 18-Bit Integrated ΣΔ DAC

AD1859

FEATURES

- Complete, Low Cost Stereo DAC System in a Single Die Package
- Variable Rate Oversampling Interpolation Filter
- Multibit ΣΔ Modulator with Triangular PDF Dither
- Discrete and Continuous Time Analog Reconstruction Filters
- 64 Step (1 dB/Step) Attenuator with Mute
- Buffered Outputs with 2 kΩ Output Load Drive
- Rejects Sample Clock Jitter
- 96 dB Dynamic Range, –90 dB THD+N Performance Targets
- Option for Analog De-emphasis Processing with External Passive Components
- ±0.1° Maximum Phase Linearity Deviation
- Continuously Variable Sample Rate Support
- Digital Phase Lock Loop Based Asynchronous Master Clock
- On-Chip Master Clock Oscillator, Only External Crystal Is Required
- Power-Down Mode
- Single +5 V Supply, 28-Pin Package
- Flexible Serial Data Port (I^2S-Justified, Left-Justified, Right-Justified and DSP Serial Port Modes)
- SPI* Compatible Serial Control Port
- Single +5 V Supply
- 28-Pin SOIC Package

APPLICATIONS

- Digital Cable TV and Direct Broadcast Satellite Set-Top Decoder Boxes
- Video Laser Disk, Video CD and CD-I Players
- High Definition Televisions, Digital Audio Broadcast Receivers
- CD, CD-R, DAT, DCC and MD Players
- Digital Audio Workstations, Computer Multimedia Products

This is a preliminary data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

PRODUCT OVERVIEW

The AD1859 is a complete single-chip stereo audio subsystem. It comprises a variable rate digital interpolation filter, a revolutionary multibit sigma delta (ΣΔ) modulator with dither, a jitter-tolerant DAC, switched capacitor and continuous time analog filters, and analog output drive circuitry. Other features include an on-chip stereo attenuator and mute, programmed through an SPI-compatible serial control port. The key differentiating feature of the AD1859 is an asynchronous master clock capability. Previous ΣΔ audio DACs required a high frequency master clock which is 256 or 384 times the intended audio sample rate. The generation and management of this high frequency synchronous clock is burdensome to the board level designer. The analog performance of conventional single bit ΣΔ DACs is also dependent on the purity of the sample and master clocks. The AD1859 has a digital Phase Lock Loop (PLL) which allows the master clock to be asynchronous, and which also strongly rejects jitter on the sample clock (left/right clock). The digital PLL allows the AD1859 to be clocked with a single frequency (27 MHz for example) while the sample frequency (as determined from the left/right clock) can vary over a wide range. The digital PLL will lock to the new sample rate in approximately 100 ms. Jitter components 15 Hz and below the sample frequency are rejected by 6 dB per octave.

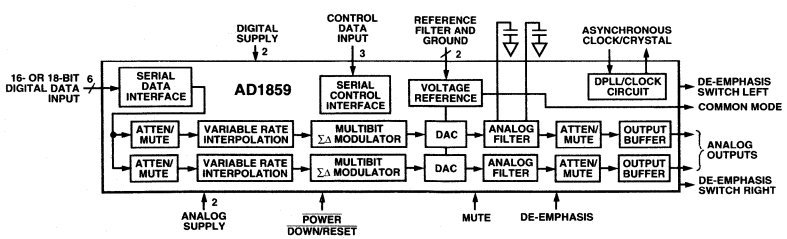
The AD1859 has a simple but very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSP chips, AES/EBU receivers and sample rate converters. The serial data input port can be configured in left-justified, I^2S-justified, right-justified and DSP serial port compatible modes. The AD1859 accepts 16- or 18-bit serial audio data in MSB-first, twos-complement format. A power-down mode is offered to minimize power consumption when the device is inactive. The AD1859 operates from a single +5 V power supply.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1859JR	0°C to +70°C	SOIC	R-28

*For outline information see Package Information section.

FUNCTIONAL BLOCK DIAGRAM



*SPI is a registered trademark of Motorola, Inc.

ANALOG DEVICES

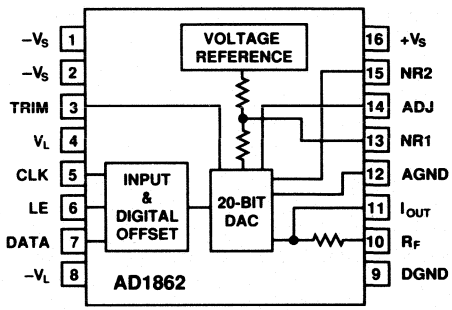
Ultralow Noise 20-Bit Audio DAC

AD1862*

FEATURES
119 dB Signal-to-Noise Ratio
102 dB D-Range Performance
±1 dB Gain Linearity
±1 mA Output Current
16-Pin DIP Package
0.0012% THD + N

APPLICATIONS
High-Performance Compact Disc Players
Digital Audio Amplifiers
Synthesizer Keyboards
Digital Mixing Consoles
High-Resolution Signal Processing

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT DESCRIPTION

The AD1862 is a monolithic 20-bit digital audio DAC. Each device provides a 20-bit DAC, 20-bit serial-to-parallel input register and voltage reference. The digital portion of the AD1862 is fabricated with CMOS logic elements that are provided by Analog Devices' BiMOS II process. The analog portion of the AD1862 is fabricated with bipolar and MOS devices as well as thin-film resistors.

New design, layout and packaging techniques all combine to produce extremely high-performance audio playback. The design of the AD1862 incorporates a digital offset circuit which improves low-level distortion performance. Low-stress packaging techniques are used to minimize stress-induced parametric shifts. Stress-sensitive circuit elements are located in die areas which are least affected by packaging stress. Laser-trimming of initial linearity error affords extremely low total harmonic distortion. Output glitch is also small, contributing to the overall high level of performance.

The noise performance of the AD1862 is excellent. When used with the recommended two external noise-reduction capacitors, it achieves 119 dB signal-to-noise ratio.

The serial input port consists of the clock, data and latch enable pins. A serial 20-bit, 2s complement data word is clocked into the DAC, MSB first, by the external data clock. A latch-enable signal transfers the input word from the internal serial input register to the DAC input register. The data clock can function at 17 MHz, allowing 16 × F_S operation. The serial input port is compatible with second-generation digital filter chips for consumer audio products such as the NPC SM5813 and SM5818.

The AD1862 operates with ±5 V to ±12 V supplies for the digital power supplies and ±12 V supplies for the analog supplies. The digital and analog supplies can be separated for reduced digital crosstalk. Separate analog and digital common pins are also provided. The AD1862 typically dissipates less than 300 mW.

The AD1862 is packaged in a 16-pin plastic DIP. The operating range is guaranteed to be −25°C to +70°C.

PRODUCT HIGHLIGHTS

1. 119 dB signal-to-noise ratio (typical)
2. 102 dB D-Range performance (minimum)
3. ±1 dB gain linearity @ −90 dB amplitude
4. 20-bit resolution provides 120 dB of dynamic range
5. 16×F_S operation
6. 0.0012% THD+N @ 0 dB signal amplitude (typical)
7. Space saving 16-pin DIP package
8. ±1 mA output current

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1862—SPECIFICATIONS (T_A at +25°C and ±12 V supplies, see Figure 10 for test circuit schematic)

	Min	Typ	Max	Units
RESOLUTION	20			Bits
DIGITAL INPUTS V_{IH}	2.0	**4.0**		V
V_{IL}		**0.4**	0.8	V
I_{IH} @ V_{IH} = 4.0 V			**1.0**	μA
I_{IL} @ V_{IL} = 0.4 V			**−10**	μA
Maximum Clock Input Frequency	**17**			MHz
ACCURACY				
Gain Error			**±2**	%
Midscale Output Error		±2	**±5**	μA
TOTAL HARMONIC DISTORTION + NOISE (EIAJ)[1]				
0 dB, 990.5 Hz AD1862N-J		−98 (0.0012)	**−96 (0.0016)**	dB (%)
AD1862N		−94 (0.0019)	**−92 (0.0025)**	dB (%)
−20 dB, 990.5 Hz AD1862N, N-J		−84 (0.0063)	**−80 (0.01)**	dB (%)
−60 dB, 990.5 Hz AD1862N, N-J		−45 (0.56)	**−42 (0.8)**	dB (%)
D-Range, −60 dB, A-Weight Filter	**102**			dB
SIGNAL-TO-NOISE RATIO[2] (EIAJ)[1]				
A-Weight Filter AD1862N-J	**113**	119		dB
AD1862N	**110**	119		dB
GAIN LINEARITY				
@ −90 dB AD1862N-J		±1		dB
AD1862N		±1		dB
OUTPUT CURRENT				
Bipolar Range		±1		mA
Tolerance		±1	**±2**	%
Output Impedance (±30%)		2.1		kΩ
Settling Time		350		ns
FEEDBACK RESISTOR				
Value		3		kΩ
Tolerance		±1	**±2**	%
POWER SUPPLY				
Voltage V_L and $-V_L$	4.75	**12.0**	13.2	±V
Voltage V_S and $-V_S$	10.8	**12.0**	13.2	±V
Current +I, V_L and V_S = 12 V, 17 MHz Clock		11	**15**	mA
−I, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		13	**16**	mA
POWER DISSIPATION				
V_L and V_S = 12 V, $-V_L$ and $-V_S$ = −12 V, 17 MHz Clock		288	372	mW
TEMPERATURE RANGE				
Specification		**+25**		°C
Operation	−25		+70	°C
Storage	−60		+100	°C

NOTES

[1]Test Method complies with EIAJ Standard CP-307.

[2]The signal-to-noise measurement includes noise contributed by the SE5534A op amp used in the test fixture but does not include the noise contributed by the low pass filter used in the test fixture.

Specifications in **boldface** are tested on all production units at final electrical test.

Specifications subject to change without notice.

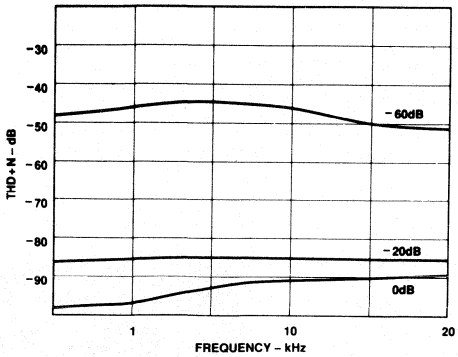


Figure 1. THD+N vs. Frequency

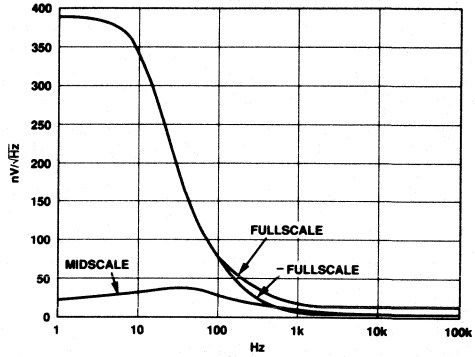


Figure 2. Noise Density

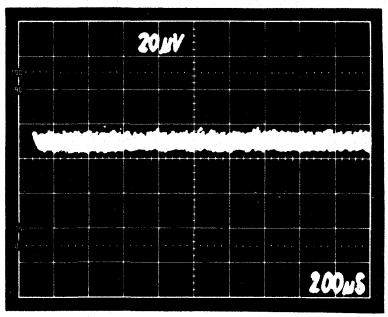


Figure 3. Broadband Noise (20 kHz Bandwidth, Midscale)

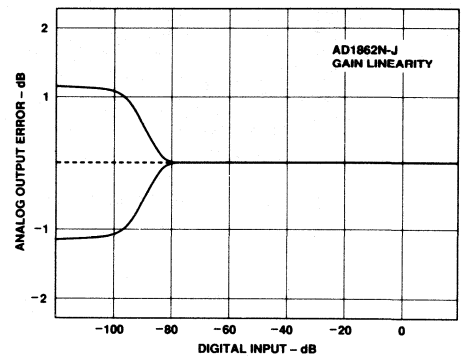


Figure 4. Gain Linearity

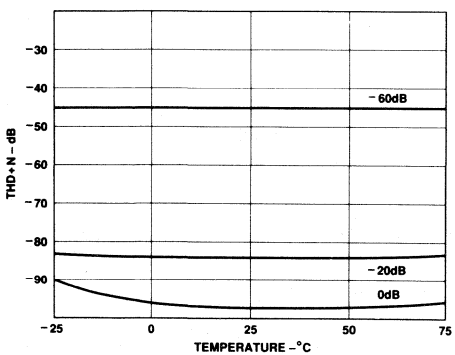


Figure 5. THD+N vs. Temperature (1 kHz)

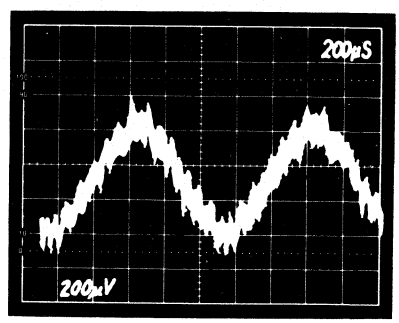


Figure 6. Midscale Differential Linearity

ABSOLUTE MAXIMUM RATINGS*

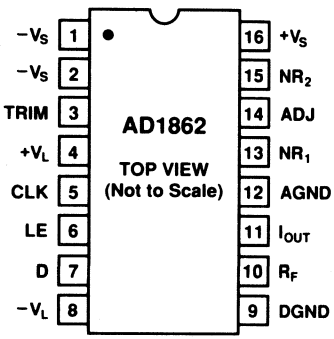
V_L to DGND . . . . . 0 to +13.2 V
$-V_L$ to DGND . . . . . $-V_S$ to 0 V
V_S to AGND . . . . . 0 to +13.2 V
$-V_S$ to AGND . . . . . −13.2 to 0 V
AGND to DGND . . . . . −0.3 to +0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Soldering . . . . . +300°C, 10 sec
Storage Temperature . . . . . −60°C to +100°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

PIN CONFIGURATION



PIN DESIGNATIONS

Pin	Function	Description
1	$-V_S$	Bias Capacitor
2	$-V_S$	Analog Negative Supply
3	TRIM	Trim Pot Connection
4	$+V_L$	Positive Logic Supply
5	CLK	External Clock Input
6	LE	Latch Enable Input
7	D	Data Input
8	$-V_L$	Negative Logic Supply
9	DGND	Digital Ground
10	R_F	Feedback Resistor
11	I_{OUT}	Output Current
12	AGND	Analog Ground
13	NR_1	Reference Capacitor
14	ADJ	Midscale Adjust
15	NR_2	Bias Capacitor
16	$+V_S$	Positive Analog Supply

ORDERING GUIDE

Model	Operating Temperature Range	THD+N @ FS	SNR	Package Option*
AD1862N	−25°C to +70°C	−92 dB, 0.0025%	110 dB	N-16
AD1862N-J	−25°C to +70°C	−96 dB, 0.0016%	113 dB	N-16

*N = Plastic DIP. For outline information see Package Information section.

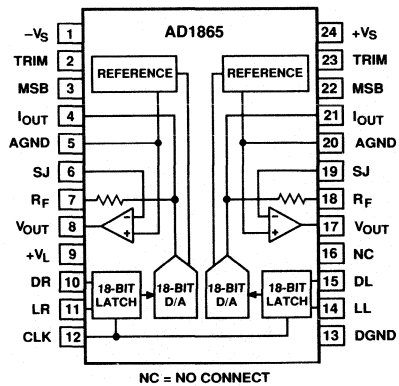
Complete Dual 18-Bit 16 × F_S Audio DAC

AD1865*

FEATURES
Dual Serial Input, Voltage Output DACs
No External Components Required
110 dB SNR
0.003% THD+N
Operates at 16 × Oversampling per Channel
±5 Volt Operation
Cophased Outputs
116 dB Channel Separation
Pin Compatible with AD1864
DIP or SOIC Packaging

APPLICATIONS
Multichannel Audio Applications:
Compact Disc Players
Multivoice Keyboard Instruments
DAT Players and Recorders
Digital Mixing Consoles
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM
(DIP Package)



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD1865 is a complete, dual 18-bit DAC offering excellent THD+N and SNR while requiring no external components. Two complete signal channels are included. This results in cophased voltage or current output signals and eliminates the need for output demultiplexing circuitry. The monolithic AD1865 chip includes CMOS logic elements, bipolar and MOS linear elements and laser-trimmed thin-film resistor elements, all fabricated on Analog Devices' ABCMOS process.

The DACs on the AD1865 chip employ a partially segmented architecture. The first four MSBs of each DAC are segmented into 15 elements. The 14 LSBs are produced using standard R-2R techniques. Segment and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. This architecture minimizes errors at major code transitions resulting in low output glitch and eliminating the need for an external deglitcher. When used in the current output mode, the AD1865 provides two ±1 mA output signals.

Each channel is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±3 V signals at load currents up to 8 mA. Each output amplifier is short-circuit protected and can withstand indefinite short circuits to ground.

The AD1865 was designed to balance two sets of opposing requirements, channel separation and DAC matching. High channel separation is the result of careful layout. At the same time, both channels of the AD1865 have been designed to ensure matched gain and linearity as well as tracking over time and temperature. This assures optimum performance when used in stereo and multi-DAC per channel applications.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

A versatile digital interface allows the AD1865 to be directly connected to standard digital filter chips. This interface employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR) and Clock (CLK). DL and DR are the serial input pins for the left and right DAC input registers. Input data bits are clocked into the input register on the rising edge of CLK. A low-going latch edge updates the respective DAC output. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together.

The AD1865 operates with ±5 V power supplies. The digital supply, V_L, can be separated from the analog supplies, V_S and $-V_S$, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. The AD1865 typically dissipates only 225 mW, with a maximum power dissipation of 260 mW.

The AD1865 is packaged in both a 24-pin plastic DIP and a 28-pin SOIC package. Operation is guaranteed over the temperature range of −25°C to +70°C and over the voltage supply range of ±4.75 V to ±5.25 V.

PRODUCT HIGHLIGHTS

1. The AD1865 is a Complete Dual 18-Bit Audio DAC.
2. 110 dB Signal-To-Noise Ratio for low noise operation.
3. THD+N is typically 0.003%.
4. Interchannel gain and midscale matching.
5. Output voltages and currents are cophased.
6. Low glitch for improved sound quality.
7. Both channels are 100% tested at 16 × F_S.
8. Low Power—only 225 mW typ, 260 mW max.
9. Five-wire interface for individual DAC control.
10. 24-pin DIP or 28-pin SOIC packages available.

AD1865—SPECIFICATIONS (T_A = +25°C, $+V_L$ = $+V_S$ = +5 V and $-V_S$ = −5 V, F_S = 705.6 kHz, no MSB adjustment or deglitcher)

Parameter		Min	Typ	Max	Unit
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.0		$+V_L$	V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = $+V_L$			**1.0**	μA
	I_{IL}, V_{IL} = 0.4 V			**−10**	μA
Clock Input Frequency		**13.5**			MHz
ACCURACY					
Gain Error			0.2	**1.0**	% of FSR
Interchannel Gain Matching			0.3	**0.8**	% of FSR
Midscale Error			4		mV
Interchannel Midscale Matching			5		mV
Gain Linearity (0 dB to −90 dB)			<2		dB
DRIFT (0°C to +70°C)					
Gain Drift			±25		ppm of FSR/°C
Midscale Drift			±4		ppm of FSR/°C
TOTAL HARMONIC DISTORTION + NOISE*					
0 dB, 990.5 Hz	AD1865N, R		0.004	**0.006**	%
	AD1865N-J, R-J		0.003	**0.004**	%
−20 dB, 990.5 Hz	AD1865N, R		0.010	**0.040**	%
	AD1865N-J, R-J		0.010	**0.020**	%
−60 dB, 990.5 Hz	AD1865N, R		1.0	**4.0**	%
	AD1865N-J, R-J		1.0	**2.0**	%
CHANNEL SEPARATION*					
0 dB, 990.5 Hz		**110**	116		dB
SIGNAL-TO-NOISE RATIO* (20 Hz to 30 kHz)		**107**	110		dB
D-RANGE* (with A-Weight Filter)					
−60 dB, 990.5 Hz	AD1865N, R	**88**	100		dB
	AD1865N-J, R-J	**94**	100		dB
OUTPUT					
Voltage Output Configuration					
Output Range (±1%)		**±2.94**	±3.0	**±3.06**	V
Output Impedance			0.1		Ω
Load Current		±8			mA
Short Circuit Duration			Indefinite to Common		
Current Output Configuration					
Bipolar Output Range (±30%)			±1		mA
Output Impedance (±30%)			1.7		kΩ
POWER SUPPLY					
$+V_L$ and $+V_S$		4.75	**5.0**	5.25	V
$-V_S$		−5.25	**−5.0**	−4.75	V
+I, $+V_L$ and $+V_S$ = +5 V			22	**26**	mA
−I, $-V_S$ = −5 V			−23	**−26**	mA
POWER DISSIPATION, $+V_L$ = $+V_S$ = +5 V, $-V_S$ = −5 V			225	**260**	mW
TEMPERATURE RANGE					
Specification		0	**+25**	+70	°C
Operation		−25		+70	°C
Storage		−60		+100	°C
WARMUP TIME		1			min

Specifications shown in **boldface** are tested on production units at final test without optional MSB adjustment.
*Tested in accordance with EIAJ Test Standard CP-307 with 18-bit data.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6.0 V
V_S to AGND . . . . . 0 to 6.0 V
$-V_S$ to AGND . . . . . −6.0 to 0 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Short Circuit Protection . . . . . Indefinite Short to Ground
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

ORDERING GUIDE

Model	Temperature Range	THD+N @ FS	Package Option*
AD1865N	−25°C to +70°C	0.006%	N-24A
AD1865N-J	−25°C to +70°C	0.004%	N-24A
AD1865R	−25°C to +70°C	0.006%	R-28
AD1865R-J	−25°C to +70°C	0.004%	R-28

*N = Plastic DIP, R = Small Outline IC Package. For outline information see Package Information section.

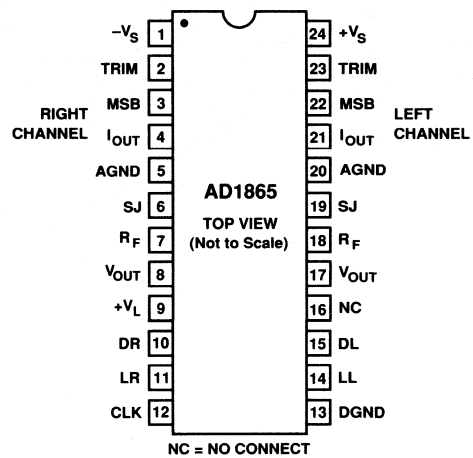
PIN DESIGNATIONS

DIP	SOIC		
1	22	$-V_S$	Negative Analog Supply
2	23	TRIM	Right Channel Trim Network Connection
3	24	MSB	Right Channel Trim Potentiometer Wiper Connection
4	26	I_{OUT}	Right Channel Output Current
5	28	AGND	Analog Common Pin
6	1	SJ	Right Channel Amplifier Summing Junction
7	2	R_F	Right Channel Feedback Resistor
8	3	V_{OUT}	Right Channel Output Voltage
9	4	$+V_L$	Positive Digital Supply
10	5	DR	Right Channel Data Input Pin
11	6	LR	Right Channel Latch Pin
12	7	CLK	Clock Input Pin
13	8	DGND	Digital Common Pin
14	9	LL	Left Channel Latch Pin
15	10	DL	Left Channel Data Input Pin
16	11, 16, 18 25, 27	NC	No Internal Connection*
17	12	V_{OUT}	Left Channel Output Voltage
18	13	R_F	Left Channel Feedback Resistor
19	14	SJ	Left Channel Amplifier Summing Junction
20	15	AGND	Analog Common Pin
21	17	I_{OUT}	Left Channel Output Current
22	19	MSB	Left Channel Trim Potentiometer Wiper Connection
23	20	TRIM	Left Channel Trim Network Connection
24	21	$+V_S$	Positive Analog Supply

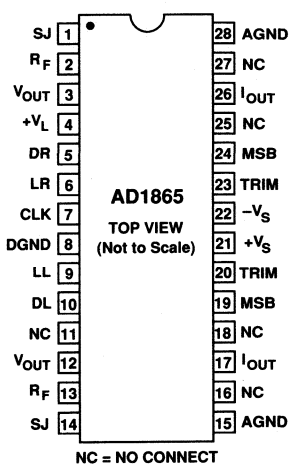
*Pin 16 has no internal connection; $-V_L$ from AD1864 DIP socket can be safely applied.

PINOUT

(24-Pin DIP Package)



(28-Pin SOIC Package)



4

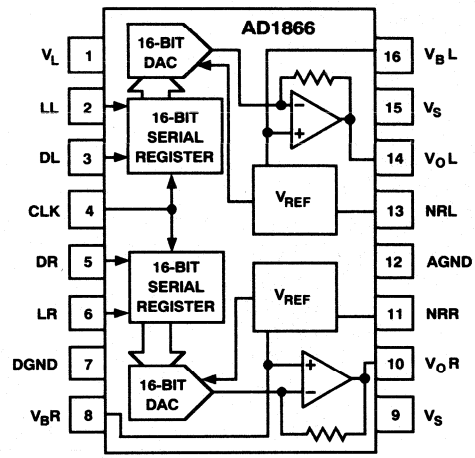
Single-Supply Dual 16-Bit Audio DAC

AD1866*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 Volt Supply
0.005% THD+N
Low Power—50 mW
115 dB Channel Separation
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Multimedia Workstations
PC Audio Add-In Boards
Portable CD and DAT Players
Automotive CD and DAT Players
Noise Cancellation

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1866 is a complete dual 16-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements and laser trimmed, thin film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation and low power dissipation.

The DACs on the AD1866 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into 7 elements. The 13 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1866 requires no deglitcher or trimming circuitry.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. The 2.5 V reference voltages eliminate the need for "false ground" networks.

A versatile digital interface allows the AD1866 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 16 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency (where F_S = 44.1 kHz) for each channel. The digital input pins of the AD1866 are TTL and +5 V CMOS compatible.

The AD1866 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1866 dissipates 50 mW.

The AD1866 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single supply operation @ +5 V.
2. 50 mW power dissipation.
3. THD+N is 0.005% (typical).
4. Signal-to-Noise Ratio is 95 dB (typical).
5. 115 dB channel separation (typical).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

AD1866—SPECIFICATIONS (T_A = +25°C and +5 V supplies unless otherwise noted)

	Min	Typ	Max	Unit
RESOLUTION		16		Bits
DIGITAL INPUTS V_{IH}	**2.4**			V
V_{IL}			**0.8**	V
I_{IH}, V_{IH} = V_L		1.0		μA
I_{IL}, V_{IL} = DGND		−10.0		μA
Maximum Clock Input Frequency	**13.5**			MHz
ACCURACY				
Gain Error		±3		% of FSR
Gain Matching		±3		% of FSR
Midscale Error		±30		mV
Midscale Error Matching		±10		mV
Gain Linearity Error		±3		dB
DRIFT (0°C to 70°C)				
Gain Drift		±100		ppm/°C
Midscale Drift		−130		μV/°C
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz AD1866N		0.005	**0.01**	%
AD1866R		0.005	**0.01**	%
−20 dB, 990.5 Hz AD1866N		0.02		%
AD1866R		0.02		%
−60 dB, 990.5 Hz AD1866N		2.0		%
AD1866R		2.0		%
CHANNEL SEPARATION (1 kHz, 0 dB)	**108**	115		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95		dB
D-RANGE (with A-Weight Filter)		90		dB
OUTPUT				
Voltage Output Pins (V_{OL}, V_{OR})				
Output Range (±3%)		±1		V
Output Impedance		0.1		Ω
Load Current		±1		mA
Bias Voltage Pins (V_{BL}, V_{BR})				
Output Range		+2.5		V
Output Impedance		350		Ω
POWER SUPPLY				
Specification, V_L and V_S	**4.75**	5	**5.25**	V
Operation, V_L and V_S	**3.5**		**5.25**	V
+I, V_L and V_S = 5 V		10	**14**	mA
POWER DISSIPATION		50	70	mW
TEMPERATURE RANGE				
Operation	−35		**85**	°C
Storage	−60		**100**	°C

Specifications subject to change without notice.
Specifications in **boldface** are tested on all production units at final electrical test.

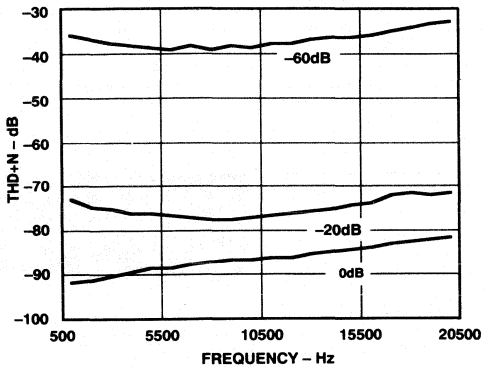


Figure 1. THD+N vs. Frequency

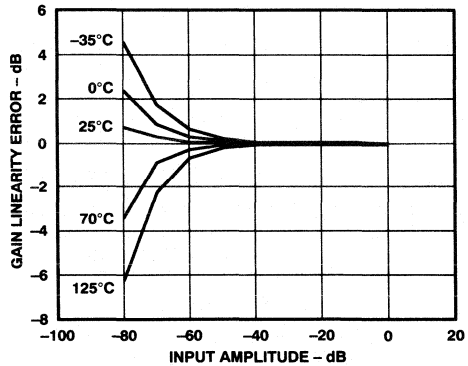


Figure 4. Gain Linearity Error vs. Input Amplitude

4

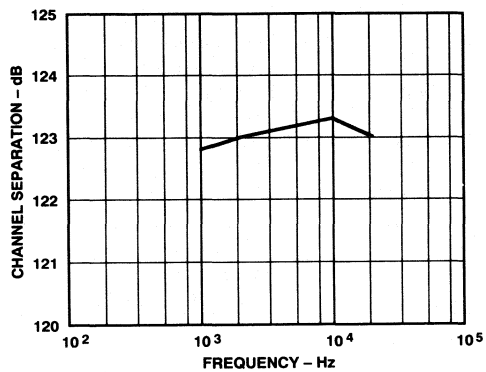


Figure 2. Channel Separation vs. Frequency

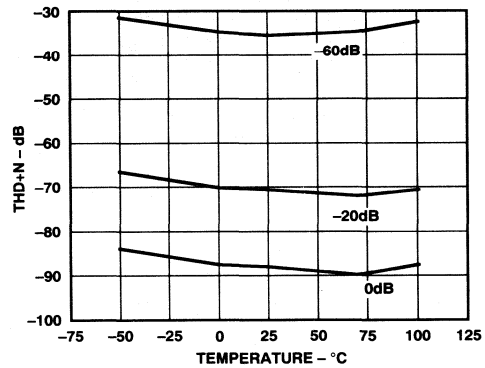


Figure 5. THD+N vs. Temperature

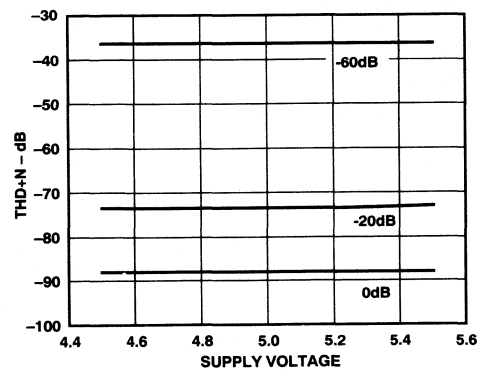


Figure 3. THD+N vs. Supply Voltage

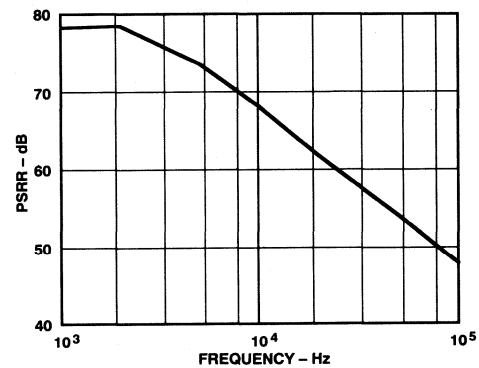


Figure 6. Power Supply Rejection Ratio vs. Frequency (Supply Modulation Amplitude at 500 mV p–p)

ABSOLUTE MAXIMUM RATINGS*

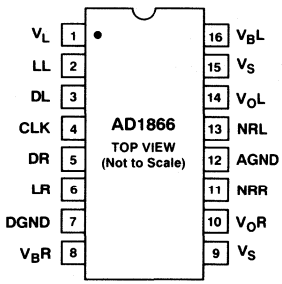
V_L to DGND . . . . . 0 V to 6 V
V_S to AGND . . . . . 0 V to 6 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 V to V_L
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

PIN CONFIGURATION



PIN DESIGNATIONS

Pin	Mnemonic	Description
1	V_L	Digital Supply (+5 V)
2	LL	Left Channel Latch Enable Pin
3	DL	Left Channel Data Input Pin
4	CLK	Clock Input Pin
5	DR	Right Channel Data Input Pin
6	LR	Right Channel Latch Enable Pin
7	DGND	Digital Common Pin
8	V_BR	Right Channel Bias Pin
9	V_S	Analog Supply (+5 V)
10	V_OR	Right Channel Output Pin
11	NRR	Right Channel Noise Reduction Pin
12	AGND	Analog Common Pin
13	NRL	Left Channel Noise Reduction Pin
14	V_OL	Left Channel Output Pin
15	V_S	Analog Supply (+5 V)
16	V_BL	Left Channel Bias Pin

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1866N	−35°C to +85°C	Plastic DIP	N-16
AD1866R	−35°C to +85°C	SOIC	R-16
AD1866R-REEL	−35°C to +85°C	SOIC	R-16

*For outline information see Package Information section.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-RANGE DISTORTION (EIAJ SPECIFICATION)

D-Range distortion is the ratio of the amplitude of the signal at an amplitude of −60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

SIGNAL-TO-NOISE RATIO

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

GAIN LINEARITY

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

MIDSCALE ERROR

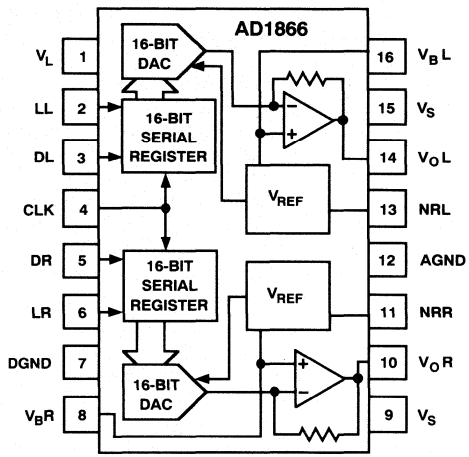
Midscale error, or bipolar zero error, is the deviation of the actual analog output from a voltage at the bias pin when the twos complement input code representing midscale is loaded in the DAC. Midscale error is expressed in mV.

FUNCTIONAL DESCRIPTION

The AD1866 is a complete, monolithic dual 16-bit digital audio DAC which runs off a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference, a 16-bit serial-to-parallel input register, a 16-bit input latch, a 16-bit DAC, and an output amplifier.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The input registers are fabricated with CMOS logic gates. These gates allow high switching speeds and low power consumption, contributing to the fast digital timing, the low glitch and low power dissipation of the AD1866.



AD1866 Functional Block Diagram

The 16-bit DAC uses a combination of segmentation and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error, resulting in low output distortion.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

AD1866—Analog Circuit Considerations

GROUNDING RECOMMENDATIONS

The AD1866 has two ground pins, designated as AGND (Pin 12) and DGND (Pin 7). The analog ground, AGND, serves as the "high quality" reference ground for analog signals and as a return path for the supply current from the analog portion of the device. The system analog common should be located as close as possible to Pin 12 to minimize any voltage drop which may develop between these two points, although the internal circuit is designed to minimize signal dependence of the analog return current.

The digital ground, DGND, returns ground current from the digital logic portion of the device. This pin should be connected to the digital common node in the system. As shown in Figure 7, the analog and digital grounds should be joined at one point in a system. When these two grounds are connected such as at the power supply ground, care should be taken to minimize the voltage difference between the DGND and AGND pins in order to ensure the specified performance.

POWER SUPPLIES AND DECOUPLING

The AD1866 has three power supply input pins. V_S (Pins 9 & 15) provide the supply voltages which operate the analog portion of the device including the 16-bit DACs, the voltage references, and the output amplifiers. The V_S supplies are designed to operate from a +5 V supply. These pins should be decoupled to the analog ground using a 0.1 μF capacitor. Good engineering practice suggests that the bypass capacitor be placed as close as possible to the package pins. This minimizes the inherent inductive effects of printed circuit board traces.

V_L (Pin 1) operates the digital portions of the chip including the input shift registers and the input latching circuitry. V_L is also designed to operate from a +5 V supply. This pin should be bypassed to digital common using a 0.1 μF capacitor, again placed as close as possible to the package pins. Figure 7 illustrates the correct connection of the digital and analog supply bypass capacitors.

An important feature of the AD1866 audio DAC is its ability to operate at diminished power supply voltages. This feature is very important in portable battery operated systems. As the batteries discharge, the supply voltage drops. Unlike any other audio DAC, the AD1866 can continue to function at supply voltages as low as 3.5 V. Because of its unique design, the power requirements of the AD1866 diminish as the battery voltage drops, further extending the operating time of the system.

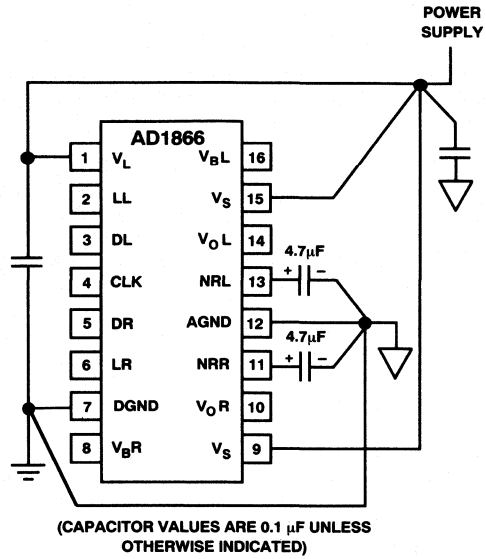


Figure 7. Recommended Circuit Schematic

NOISE REDUCTION CAPACITORS

The AD1866 has two noise reduction pins, designated as NRL (Pin 13) and NRR (Pin 11). In order to meet specifications, it is required that external noise reduction capacitors be connected from these pins to AGND to reduce the output noise contributed by the voltage reference circuitry. As shown in Figure 7, each of these pins should be bypassed to AGND with a 4.7 μF or larger capacitor. The connections between the capacitors, package pins and AGND should be as short as possible to achieve the lowest noise.

USING V_BL AND V_BR

The AD1866 has two bias voltage reference pins, designated as V_BR (Pin 8) and V_BL (Pin 16). Each of these pins supplies a dc reference voltage equal to the center of the output voltage swing. These bias voltages replace "false ground" networks previously required in single supply audio systems. At the same time, they allow dc coupled systems, improving audio performance.

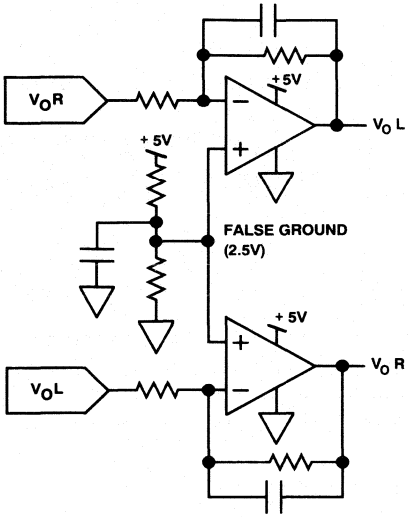


Figure 8a. Schematic Using False Ground

Figure 8a illustrates the traditional approach used to generate false ground voltages in single supply audio systems. This circuit requires additional power and circuit board space.

The AD1866 eliminates the need for "false ground" circuitry. V_BR and V_BL generate the required bias voltages previously generated by the "false ground." As shown in Figure 8b, V_BR and V_BL may be used as the reference point in each output channel. This permits a dc coupled output signal path. This eliminates ac coupling capacitors and improves low frequency performance. It should be noted that these bias outputs have relatively high output impedance and will not drive output currents larger than 100 μA without degrading the specified performance.

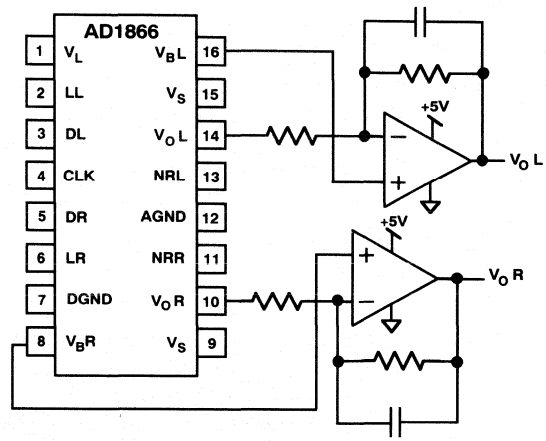


Figure 8b. Circuitry Using Voltage Biases

4

DISTORTION PERFORMANCE AND TESTING

The THD+N figure of an audio DAC represents the amount of undesirable signal produced during reconstruction and playback of an audio waveform. Therefore, the THD+N specification provides a direct measure to classify and choose an audio DAC for a desired level of performance. Figure 1 illustrates the typical THD+N versus frequency performance of the AD1866. It is evident that the THD+N performance of the AD1866 remains stable at all three amplitude levels through a wide range of frequencies. A load impedance of at least 2 kΩ is recommended for best THD+N performance.

Analog Devices tests all AD1866s on the basis of THD+N performance. During the distortion test, a high speed digital pattern generator transmits digital data to each channel of the device under test. Sixteen-bit data is latched into the DAC at 352.8 kHz ($8 \times F_S$). The test input code is a digitally encoded 990.5 Hz sine wave with 0 dB, −20 dB, and −60 dB amplitudes. A 4096 point FFT calculates total harmonic distortion + noise, signal-to-noise ratio, and D-range. No deglitchers or external adjustments are used.

AD1866—Digital Circuit Considerations

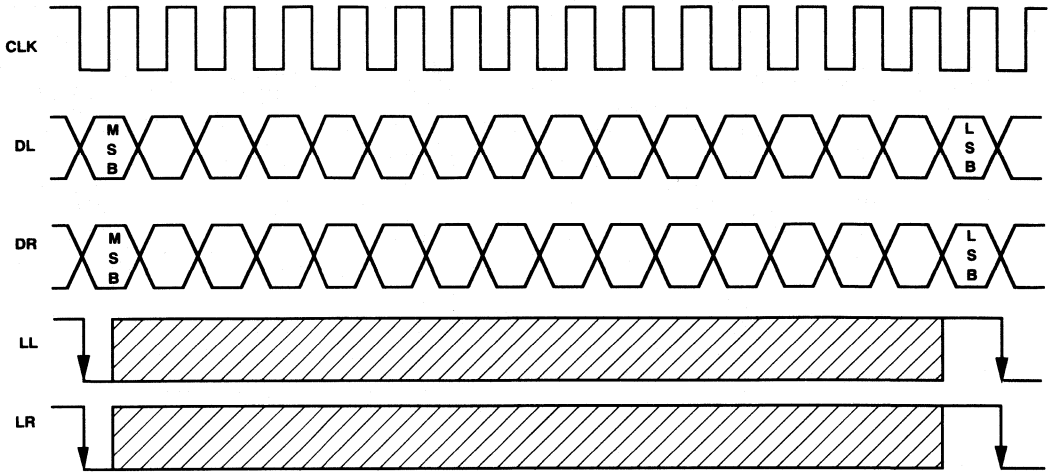


Figure 9. AD1866 Control Signals

INPUT DATA

The digital input port of the AD1866 employs five signals: Data Left (DL), Data Right (DR), Latch Left (LL), Latch Right (LR), and Clock (CLK). DL and DR are the serial inputs for the left and right DACs, respectively. Input data bits are clocked into the input register on the rising edge of CLK. The falling edges of LL and LR cause the last 16 bits which were clocked into the serial registers to be shifted into the DACs, thereby updating the respective DAC outputs. For systems using only a single latch signal, LL and LR may be connected together. For systems using only one DATA signal, DR and DL may be connected together. Data is transmitted to the AD1866 in a bit stream composed of 16-bit words with a serial, twos complement, MSB first format. Left and right channels share the Clock (CLK) signal.

Figure 9 illustrates the general signal requirements for data transfer for the AD1866.

TIMING

Figure 10 illustrates the specific timing requirements that must be met in order for the data transfer to be accomplished properly. The input pins of the AD1866 are both TTL and +5 V CMOS compatible.

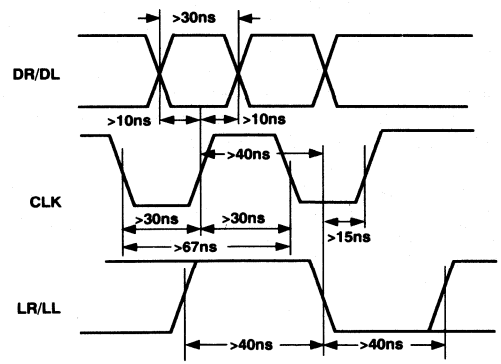


Figure 10. AD1866 Input Signal Timing

The maximum clock rate of the AD1866 is specified to be at least 13.5 MHz. This clock rate allows data transfer rates of 2×, 4×, 8×, and 16× F_S (where F_S equals 44.1 kHz). The applications section of this data sheet contains additional guidelines for using the AD1866.

APPLICATIONS OF THE AD1866

The AD1866 is a high performance audio DAC specifically designed for portable and automotive digital audio applications. These market segments have technical requirements fundamentally different than those found in the high-end or home use market segment. Portable equipment must rely on components which require low amounts of power to offer reasonable playback times. Also, battery voltage tends to diminish as the end of the discharge cycle is approached. The AD1866's ability to operate from a single +5 V supply makes it a good choice for battery operated gear. And, as the battery voltage drops, the power dissipation of the AD1866 drops. This extends the usable battery life. Finally, as the battery supply voltage drops, the bias voltages and signal swings also drop, preventing signal clipping and abrupt degradation of distortion. Figure 3 illustrates how the THD+N performance of the AD1866 remains constant through a wide supply voltage range.

Automotive equipment relies on components which are able to consistently perform over a wide range of temperatures. In addition, due to the limited space available in automotive applications, small size is essential. The AD1866 has guaranteed operation between −35°C and +85°C, and the 16-pin DIP or 16-pin SOIC package is particularly attractive where overall size is important.

Since the AD1866 provides dc bias voltages, the entire signal chain can be dc coupled. This eliminates ac coupling capacitors from the signal path, improving low frequency performance and lowering system cost and size.

In summary, the AD1866 is an excellent choice for multimedia, battery operated portable or automotive digital audio systems. In the following sections, some examples of high performance audio applications featuring the AD1866 are described.

AD1866 with the Sony CXD2550P Digital Filter

Figure 11 illustrates a 16-bit CD player design incorporating an AD1866 DAC, a Sony CXD2550P digital filter, and 2-pole antialias filters. This high performance, single supply design operates at 8× F_S and is suitable for portable and automotive applications. In this design, the CXD2550P filter transmits left and right channel digital data to the AD1866. The left and right latch signals, LL and LR, are both provided by the word clock signal (LRCKO) of the digital filter. The digital data is converted to low distortion output voltages by the output amplifiers on the AD1866. Also, no deglitching circuitry or external adjustments are required. Bypass capacitors, noise reduction capacitors and the antialias filter details are omitted for clarity.

ADDITIONAL APPLICATIONS

In addition to CD player designs, the AD1866 is suited for similar applications such as DAT, portable musical instruments, laptop and notebook personal computers, and PC audio I/O boards. The circuit techniques illustrated here are directly applicable in those applications. Figures 12, 13, 14, and 15 show connection diagrams for the AD1866 and several popular digital filter chips from NPC and Yamaha. Each application operates at 8× F_S operation. Please refer to the appropriate sections of this data sheet for additional information.

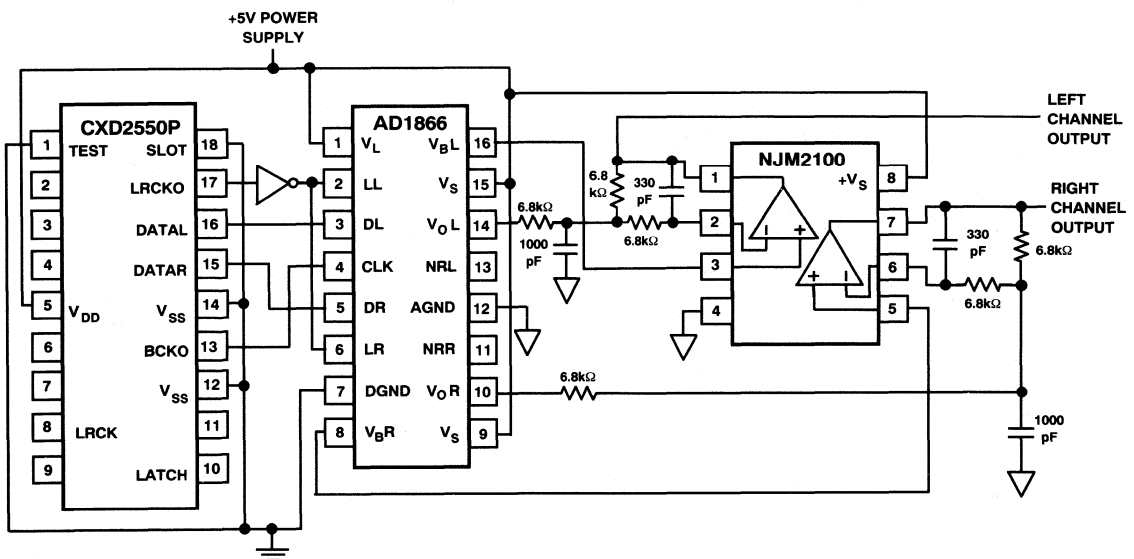


Figure 11. AD1866 with Sony CXD255P Digital Filter

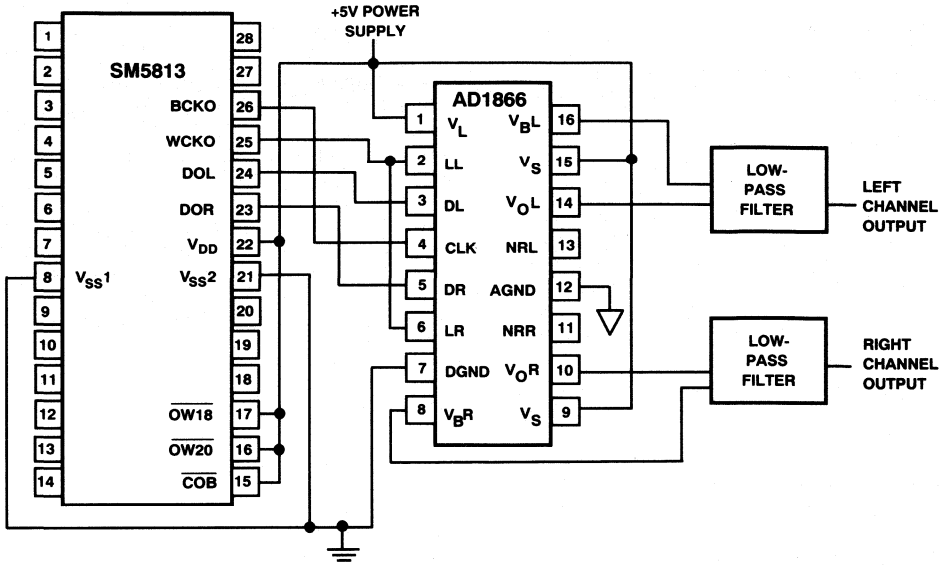


Figure 12. AD1866 with NPC SM5813 Digital Filter

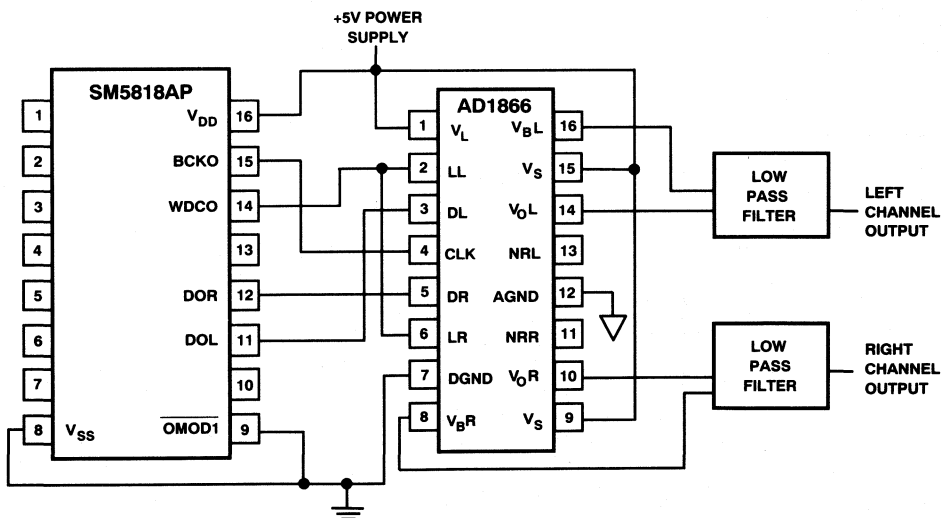


Figure 13. AD1866 with NPC SM5818AP Digital Filter

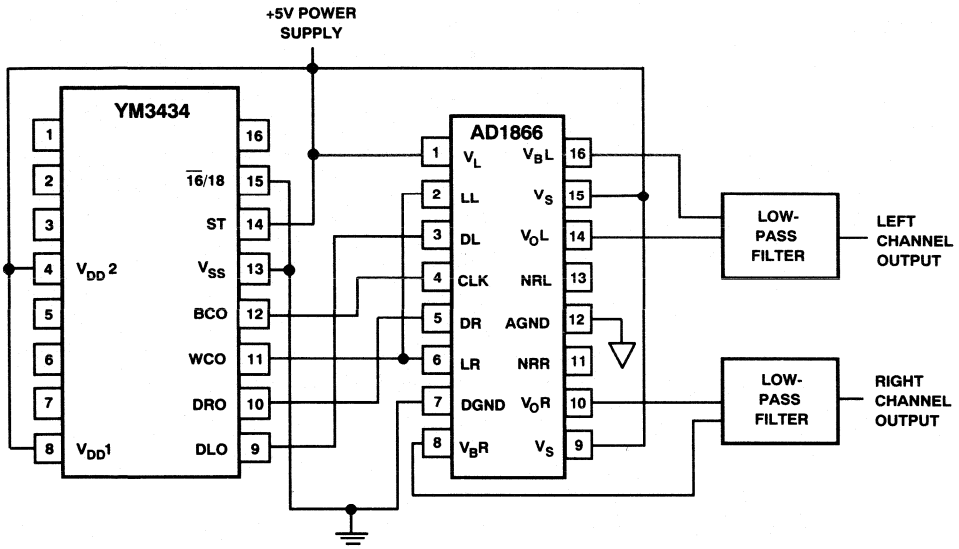


Figure 14. AD1866 with Yamaha YM3434 Digital Filter

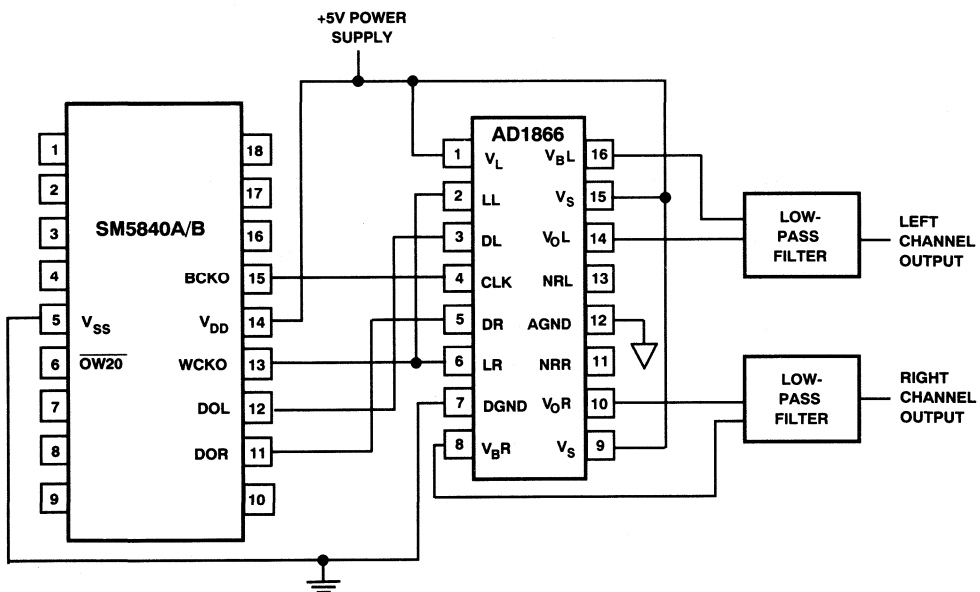


Figure 15. AD1866 with NPC SM5840C Digital Filter

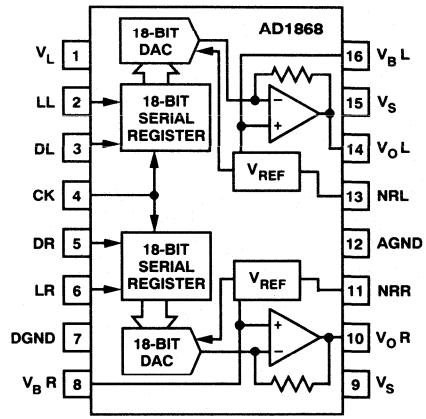
Single-Supply Dual 18-Bit Audio DAC

AD1868*

FEATURES
Dual Serial Input, Voltage Output DACs
Single +5 V Supply
0.004% THD+N (typical)
Low Power: 50 mW (typical)
108 dB Channel Separation (minimum)
Operates at 8× Oversampling
16-Pin Plastic DIP or SOIC Package

APPLICATIONS
Portable Compact Disc Players
Portable DAT Players and Recorders
Automotive Compact Disc Players
Automotive DAT Players
Multimedia Workstations

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry. Low noise is achieved through the use of two noise-reduction capacitors.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ±1 V signals at load currents up to ±1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

The AD1868 operates on +5 V power supplies. The digital supply, V_L, can be separated from the analog supply, V_S, for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of −35°C to +85°C and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation @ +5 V.
2. 50 mW power dissipation (typical).
3. THD+N is 0.004% (typical).
4. Signal-to-Noise Ratio is 97.5 dB (typical).
5. 108 dB channel separation (minimum).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1868—SPECIFICATIONS (typical at T_A = +25°C and +5 V supplies unless otherwise noted)

		Min	Typ	Max	Units
RESOLUTION			18		Bits
DIGITAL INPUTS	V_{IH}	2.4			V
	V_{IL}			0.8	V
	I_{IH}, V_{IH} = V_L		1.0		μA
	I_{IL}, V_{IL} = DGND		1.0		μA
Maximum Clock Input Frequency		13.5			MHz
ACCURACY					
Gain Error			±1		% of FSR
Gain Matching			±1		% of FSR
Midscale Error			±15		mV
Midscale Error Matching			±10		mV
Gain Linearity Error			±3		dB
DRIFT (0°C to +70°C)					
Gain Drift			±100		ppm/°C
Midscale Drift			±100		μV/°C
TOTAL HARMONIC DISTORTION + NOISE					
0 dB, 990.5 Hz	AD1868N		0.004	0.008	%
	AD1868N-J		0.004	0.006	%
−20 dB, 990.5 Hz	AD1868N		0.020	0.08	%
	AD1868N-J		0.020	0.08	%
−60 dB, 990.5 Hz	AD1868N		2.0	5.0	%
	AD1868N-J		2.0	5.0	%
CHANNEL SEPARATION 1 kHz, 0 dB		108	NIL*		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)		95	97.5		dB
D-RANGE (with A-Weight Filter)		86	92		dB
OUTPUT					
Voltage Output Pins (V_OL, V_OR)					
Output Range (±3%)			±1		V
Output Impedance			0.1		Ω
Load Current			±1		mA
Bias Voltage Pins (V_BL, V_BR)					
Output Voltage			+2.5		V
Output Impedance			350		Ω
POWER SUPPLY					
Specification, V_L and V_S		4.75	5	5.25	V
Operation, V_L and V_S		3.5		5.25	V
+I, V_L and V_S = 5 V			10	14	mA
POWER DISSIPATION			50	70	mW
TEMPERATURE RANGE					
Specification		0	25	70	°C
Operation		−35		85	°C
Storage		−60		100	°C

*Above 115 dB.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_L to DGND . . . . . 0 to 6 V
V_S to AGND . . . . . 0 to 6 V
AGND to DGND . . . . . ±0.3 V
Digital Inputs to DGND . . . . . −0.3 to V_L
Soldering . . . . . 300°C, 10 sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

Typical Performance of the AD1868

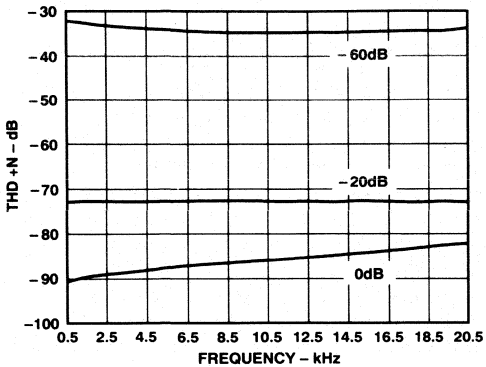


Figure 1. THD+N vs. Frequency

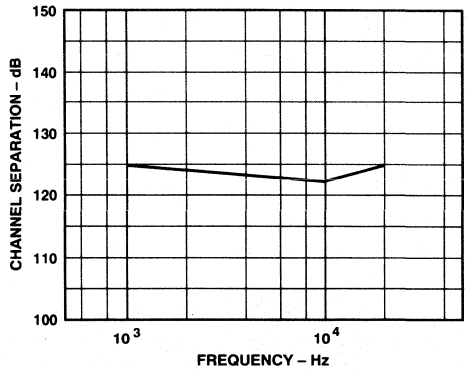


Figure 2. Channel Separation vs. Frequency

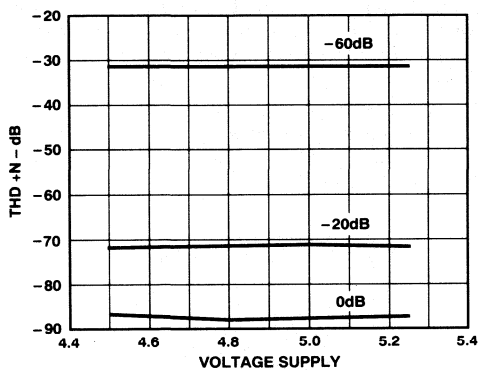


Figure 3. THD+N vs. Supply Voltage

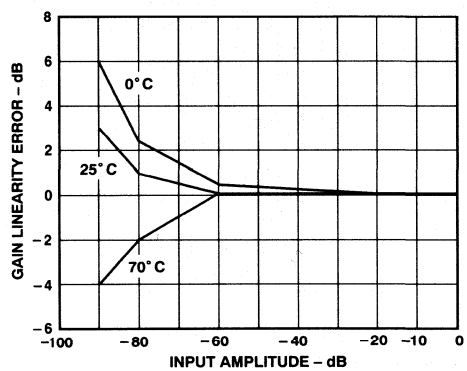


Figure 4. Gain Linearity Error vs. Input Amplitude

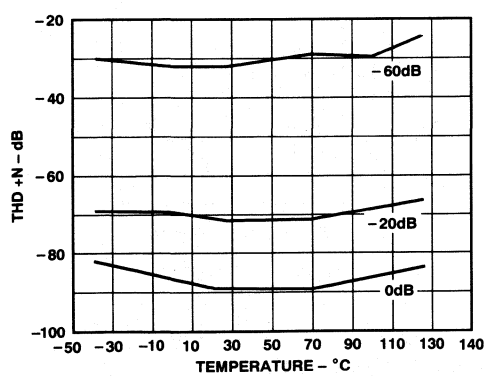


Figure 5. THD+N vs. Temperature

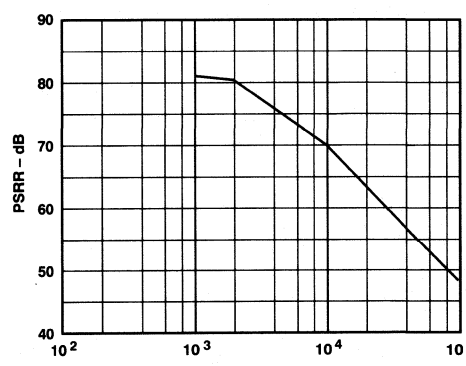
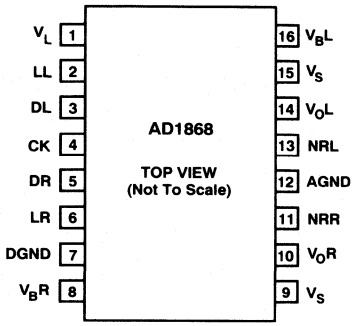


Figure 6. Power Supply Rejection Ratio vs. Frequency

AD1868 PIN CONFIGURATION



PIN DESIGNATIONS

1	V_L	DIGITAL SUPPLY (+5 VOLTS)
2	LL	LEFT CHANNEL LATCH ENABLE
3	DL	LEFT CHANNEL DATA INPUT
4	CK	CLOCK INPUT
5	DR	RIGHT CHANNEL DATA INPUT
6	LR	RIGHT CHANNEL LATCH ENABLE
7	DGND	DIGITAL COMMON
8	V_BR	RIGHT CHANNEL BIAS
9	V_S	ANALOG SUPPLY (+5 VOLTS)
10	V_OR	RIGHT CHANNEL OUTPUT
11	NRR	RIGHT CHANNEL NOISE REDUCTION
12	AGND	ANALOG COMMON
13	NRL	LEFT CHANNEL NOISE REDUCTION
14	V_OL	LEFT CHANNEL OUTPUT
15	V_S	ANALOG SUPPLY (+5 VOLTS)
16	V_BL	LEFT CHANNEL BIAS

DEFINITION OF SPECIFICATIONS

Total Harmonic Distortion + Noise

Total harmonic distortion plus noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the amplitudes of the harmonics and noise to the amplitude of the fundamental input frequency. It is usually expressed in percent (%) or decibels (dB).

D-Range Distortion

D-range distortion is the ratio of the amplitude of the signal at an amplitude of −60 dB to the amplitude of the distortion plus noise. In this case, an A-weight filter is used. The value specified for D-range performance is the ratio measured plus 60 dB.

Signal-to-Noise Ratio

The signal-to-noise ratio is defined as the ratio of the amplitude of the output when a full-scale output is present to the amplitude of the output with no signal present. It is expressed in decibels (dB) and measured using an A-weight filter.

Gain Linearity

Gain linearity is a measure of the deviation of the actual output amplitude from the ideal output amplitude. It is determined by measuring the amplitude of the output signal as the amplitude of that output signal is digitally reduced to a lower level. A perfect D/A converter exhibits no difference between the ideal and actual amplitudes. Gain linearity is expressed in decibels (dB).

Midscale Error

Midscale error is the difference between the analog output and the bias when the twos complement input code representing midscale is loaded in the input register. Midscale error is expressed in mV.

FUNCTIONAL DESCRIPTION

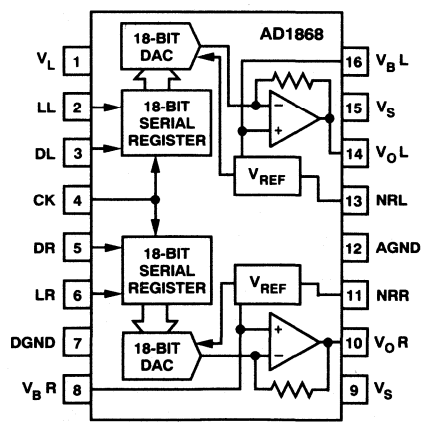
The AD1868 is a complete, voltage output dual 18-bit digital audio DAC which operates with a single +5 volt supply. As shown in the block diagram, each channel contains a voltage reference, an 18-bit DAC, an output amplifier, an 18-bit input latch, and an 18-bit serial-to-parallel input register.

The voltage reference section provides a reference voltage and a false ground voltage for each channel. The low noise bandgap circuits produce reference voltages that are unaffected by changes in temperature, time, and power supply.

The output amplifier uses both MOS and bipolar devices and incorporates an NPN class-A output stage. It is designed to produce high slew rate, low noise, low distortion, and optimal frequency response.

Each 18-bit DAC uses a combination of segmented decoder and R-2R architecture to achieve good integral and differential linearity. The resistors which form the ladder structure are fabricated with silicon-chromium thin film. Laser trimming of these resistors further reduces linearity error, resulting in low output distortion.

The input registers are fabricated with CMOS logic gates. These gates allow fast switching speeds and low power consumption, contributing to the fast digital timing, low glitch, and low power dissipation of the AD1868.



AD1868 Functional Block Diagram

ORDERING GUIDE

Model	THD+N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.006%	95 dB	N-16
AD1868R-J	0.006%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.

Single-Supply 16-Bit ΣΔ Stereo ADC

AD1877*

FEATURES

Single +5 V Power Supply
Single-Ended Dual-Channel Analog Inputs
92 dB (typ) Dynamic Range
90 dB (typ) S/(THD+N)
0.006 dB Decimator Passband Ripple
Fourth-Order, 64-Times Oversampling ΣΔ Modulator
Three-Stage, Linear-Phase Decimator
256 × F_S or 384 × F_S Input Clock
Less than 100 μW (typ) Power-Down Mode
Input Overrange Indication
On-Chip Voltage Reference
Flexible Serial Output Interface
28-Pin SOIC Package

APPLICATIONS

Consumer Digital Audio Receivers
Digital Audio Recorders, Including Portables
CD-R, DCC, MD and DAT
Multimedia and Consumer Electronic Equipment
Sampling Music Synthesizers
Digital Karaoke Systems

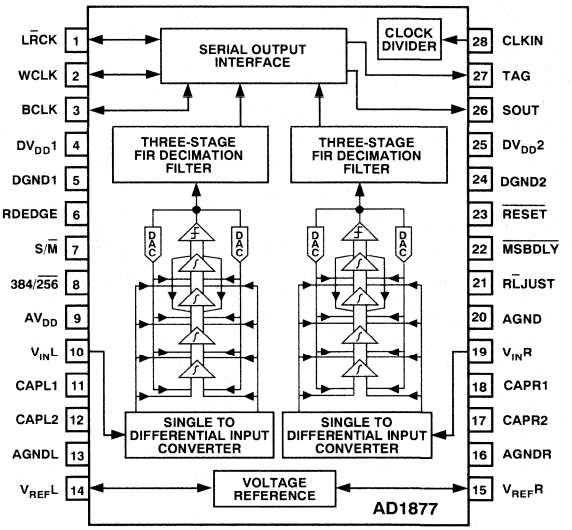
PRODUCT OVERVIEW

The AD1877 is a stereo, 16-bit oversampling ADC based on Sigma Delta (ΣΔ) technology intended primarily for digital audio bandwidth applications requiring a single +5 V power supply. Each single-ended channel consists of a fourth-order one-bit noise shaping modulator and a digital decimation filter. An on-chip voltage reference, stable over temperature and time, defines the full-scale range for both channels. Digital output data from both channels are time-multiplexed to a single, flexible serial interface. The AD1877 accepts a 256 × F_S or a 384 × F_S input clock (F_S is the sampling frequency) and operates in both serial port "master" and "slave" modes. In slave mode, all clocks must be externally derived from a common source.

Input signals are sampled at 64 × F_S onto internally buffered switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The on-chip single-ended to differential signal converters save the board designer from having to provide them externally. The AD1877's internal differential architecture provides increased dynamic range and excellent power supply rejection characteristics. The AD1877's proprietary fourth-order differential switched-capacitor ΣΔ modulator architecture shapes the one-bit comparator's quantization noise out of the audio passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the AD1877 to very low levels. Because its modulator is single-bit, AD1877 is inherently monotonic and has no mechanism for producing differential linearity errors.

*Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.

FUNCTIONAL BLOCK DIAGRAM



The input section of the AD1877 uses autocalibration to correct any dc offset voltage present in the circuit, provided that the inputs are ac coupled. The single-ended dc input voltage can swing between 0.7 V and 3.8 V typically. The AD1877 antialias input circuit requires four external 470 pF NPO ceramic chip filter capacitors, two for each channel. No active electronics are needed. Decoupling capacitors for the supply and reference pins are also required.

The dual digital decimation filters are triple-stage, finite impulse response filters for effectively removing the modulator's high frequency quantization noise and reducing the 64 × F_S single-bit output data rate to an F_S word rate. They provide linear phase and a narrow transition band that properly digitizes 20 kHz signals at a 44.1 kHz sampling frequency. Passband ripple is less than 0.006 dB, and stopband attenuation exceeds 90 dB.

The flexible serial output port produces data in twos-complement, MSB-first format. The input and output signals are TTL compatible. The port is configured by pin selections. Each 16-bit output word of a stereo pair can be formatted within a 32-bit field of a 64-bit frame as either right-justified, I²S-compatible, Word Clock controlled or left-justified positions. Both 16-bit samples can also be packed into a 32-bit frame, in left-justified and I²S-compatible positions.

AD1877—SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	+5.0	V
Ambient Temperature	25	°C
Input Clock (F_{CLKIN}) [256 × F_S]	12.288	MHz
Input Signal	991.768	Hz
	−0.5	dB Full Scale
Measurement Bandwidth	23.2 Hz to 19.998 kHz	
Load Capacitance on Digital Outputs	50	pF
Input Voltage HI (V_{IH})	2.4	V
Input Voltage LO (V_{IL})	0.8	V

Master Mode, Data I^2S-Justified (ref. Figure 21).
Device Under Test (DUT) bypassed and decoupled as shown in Figure 3.
DUT is antialiased and ac coupled as shown in Figure 2. DUT is calibrated.
Values in bold typeface are tested, all others are guaranteed but not tested.

ANALOG PERFORMANCE

	Min	Typ	Max	Units
Resolution		16		Bits
Dynamic Range (20 Hz to 20 kHz, −60 dB Input)				
Without A-Weight Filter	90	92		dB
With A-Weight Filter	92	94		dB
Signal to (THD + Noise)	88	90		dB
Signal to THD	92	94		dB
Analog Inputs				
Single-Ended Input Range (± Full Scale)*	V_{REF} − 1.55	V_{REF}	V_{REF} + 1.55	V
Input Impedance at Each Input Pin		32		kΩ
V_{REF}	**2.05**	2.25	**2.55**	V
DC Accuracy				
Gain Error		±0.5	**±2.5**	%
Interchannel Gain Mismatch		0.01		dB
Gain Drift		115		ppm/°C
Midscale Offset Error (After Calibration)		±3	**±20**	LSBs
Midscale Drift		15		ppm/°C
Crosstalk (EIAJ Method)	**−90**	−99		dB

*V_{IN} p-p = V_{REF} × 1.333.

DIGITAL I/O

	Min	Typ	Max	Units
Input Voltage HI (V_{IH})	2.4			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 5 V)			10	μA
Input Leakage (I_{IL} @ V_{IL} = 0 V)			10	μA
Output Voltage HI (V_{OH} @ I_{OH} = −2 mA)	2.4			V
Output Voltage LO (V_{OL} @ I_{OL} = 2 mA)			0.4	V
Input Capacitance			15	pF

DIGITAL TIMING (Guaranteed over 0°C to +70°C, DV_{DD} = AV_{DD} = +5 V ± 5%. Refer to Figures 24–26.)

		Min	Typ	Max	Units
t_{CLKIN}	CLKIN Period	48	81	780	ns
F_{CLKIN}	CLKIN Frequency ($1/t_{CLKIN}$)	1.28	12.288	20.48	MHz
t_{CPWL}	CLKIN LO Pulse Width	15			ns
t_{CPWH}	CLKIN HI Pulse Width	15			ns
t_{RPWL}	$\overline{\text{RESET}}$ LO Pulse Width	50			ns
t_{BPWL}	BCLK LO Pulse Width	15			ns
t_{BPWH}	BCLK HI Pulse Width	15			ns
t_{DLYCKB}	CLKIN Rise to BCLK Xmit (Master Mode)			15	ns
t_{DLYBLR}	BCLK Xmit to L$\overline{\text{R}}$CK Transition (Master Mode)			15	ns
t_{DLYBWR}	BCLK Xmit to WCLK Rise			10	ns
t_{DLYBWF}	BCLK Xmit to WCLK Fall			10	ns
t_{DLYDT}	BCLK Xmit to Data/Tag Valid (Master Mode)			10	ns
$t_{SETLRBS}$	L$\overline{\text{R}}$CK Setup to BCLK Sample (Slave Mode)	10			ns
$t_{DLYLRDT}$	L$\overline{\text{R}}$CK Transition to Data/TAG Valid (Slave Mode)				
	No MSB Delay Mode (for MSB Only)			40	ns
t_{SETWBS}	WCLK Setup to BCLK Sample (Slave Mode)				
	Data Position Controlled by WCLK Input Mode	10			ns
t_{DLYBDT}	BCLK Xmit to DATA/TAG Valid (Slave Mode)				
	All Bits Except MSB in No MSB Delay Mode				
	All Bits in MSB Delay Mode			10	ns

POWER

	Min	Typ	Max	Units
Supplies				
Voltage, Analog and Digital	4.75	5	5.25	V
Analog Current		35	43	mA
Analog Current — Power Down (CLKIN Running)		6	26	μA
Digital Current		16	20	mA
Digital Current — Power Down (CLKIN Running)		13	39	μA
Dissipation				
Operation — Both Supplies		255	315	mW
Operation — Analog Supply		175	215	mW
Operation — Digital Supply		80	100	mW
Power Down — Both Supplies (CLKIN Running)		95	325	μW
Power Down — Both Supplies (CLKIN Not Running)		5		μW
Power Supply Rejection (See Figure 11)				
1 kHz 300 mV p-p Signal at Analog Supply Pins		76		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		71		dB
Stopband (≥0.55 × F_S) — any 300 mV p-p Signal		80		dB

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	0		70	°C
Storage	−60		100	°C

DIGITAL FILTER CHARACTERISTICS

	Min	Typ	Max	Units
Decimation Factor		64		
Passband Ripple			0.006	dB
Stopband[1] Attenuation	90			dB
48 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		21.6	kHz
Stopband	26.4			kHz
44.1 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		20	kHz
Stopband	24.25			kHz
32 kHz F_S (at Recommended Crystal Frequencies)				
Passband	0		14.4	kHz
Stopband	17.6			kHz
Other F_S				
Passband	0		0.45	F_S
Stopband	0.55			F_S
Group Delay			$36/F_S$	s
Group Delay Variation			0	μs

NOTES
[1]Stopband repeats itself at multiples of 64 × F_S, where F_S is the output word rate. Thus the digital filter will attenuate to 0 dB across the frequency spectrum except for a range ±0.55 × F_S wide at multiples of 64 × F_S.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
$DV_{DD}1$ to DGND1 and $DV_{DD}2$ to DGND2	0		6	V
AV_{DD} to AGND/AGNDL/AGNDR	0		6	V
Digital Inputs	DGND − 0.3		DV_{DD} + 0.3	V
Analog Inputs	AGND − 0.3		AV_{DD} + 0.3	V
AGND to DGND	−0.3		0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering (10 sec)			+300	°C

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1877 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1877JR	0°C to +70°C	SOIC	R-28

*For outline information see Package Information section.

PIN DESCRIPTION

Pin	Input/ Output	Pin Name	Description
1	I/O	LRCK	Left/Right Clock
2	I/O	WCLK	Word Clock
3	I/O	BCLK	Bit Clock
4	I	$DV_{DD}1$	+5 V Digital Supply
5	I	DGND1	Digital Ground
6	I	RDEDGE	Read Edge Polarity Select
7	I	S/M	Slave/Master Select
8	I	384/256	Clock Mode
9	I	AV_{DD}	+5 V Analog Supply
10	I	$V_{IN}L$	Left Channel Input
11	O	CAPL1	Left External Filter Capacitor 1
12	O	CAPL2	Left External Filter Capacitor 2
13	I	AGNDL	Left Analog Ground
14	O	$V_{REF}L$	Left Reference Voltage Output
15	O	$V_{REF}R$	Right Reference Voltage Output
16	I	AGNDR	Right Analog Ground
17	O	CAPR2	Right External Filter Capacitor 2
18	O	CAPR1	Right External Filter Capacitor 1
19	I	$V_{IN}R$	Right Channel Input
20	I	AGND	Analog Ground
21	I	R/LJUST	Right/Left Justify
22	I	MSBDLY	Delay MSB One BCLK Period
23	I	RESET	Reset
24	I	DGND2	Digital Ground
25	I	$DV_{DD}2$	+5 V Digital Supply
26	O	SOUT	Serial Data Output
27	O	TAG	Serial Overrange Output
28	I	CLKIN	Master Clock

DEFINITIONS

Dynamic Range
The ratio of a full-scale output signal to the integrated output noise in the passband (20 Hz to 20 kHz), expressed in decibels (dB). Dynamic range is measured with a −60 dB input signal and is equal to (S/[THD+N]) +60 dB. Note that spurious harmonics are below the noise with a −60 dB input, so the noise level establishes the dynamic range. The dynamic range is specified with and without an A-Weight filter applied.

Signal to (Total Harmonic Distortion + Noise) (S/(THD + N))
The ratio of the root-mean-square (rms) value of the fundamental input signal to the rms sum of all other spectral components in the passband, expressed in decibels (dB).

Signal to Total Harmonic Distortion (S/THD)
The ratio of the rms value of the fundamental input signal to the rms sum of all harmonically related spectral components in the passband, expressed in decibels.

Passband
The region of the frequency spectrum unaffected by the attenuation of the digital decimator's filter.

Passband Ripple
The peak-to-peak variation in amplitude response from equal-amplitude input signal frequencies within the passband, expressed in decibels.

Stopband
The region of the frequency spectrum attenuated by the digital decimator's filter to the degree specified by "stopband attenuation."

Gain Error
With a near full-scale input, the ratio of actual output to expected output, expressed as a percentage.

Interchannel Gain Mismatch
With identical near full-scale inputs, the ratio of outputs of the two stereo channels, expressed in decibels.

Gain Drift
Change in response to a near full-scale input with a change in temperature, expressed as parts-per-million (ppm) per °C.

Midscale Offset Error
Output response to a midscale dc input, expressed in least-significant bits (LSBs).

Midscale Drift
Change in midscale offset error with a change in temperature, expressed as parts-per-million (ppm) per °C.

Crosstalk (EIAJ method)
Ratio of response on one channel with a grounded input to a full-scale 1 kHz sine-wave input on the other channel, expressed in decibels.

Power Supply Rejection
With no analog input, signal present at the output when a 300 mV p-p signal is applied to power supply pins, expressed in decibels of full scale.

Group Delay
Intuitively, the time interval required for an input pulse to appear at the converter's output, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Group Delay Variation
The difference in group delays at different input frequencies. Specified as the difference between largest and the smallest group delays in the passband, expressed in microseconds (μs).

The AD1877 is fabricated on a single monolithic integrated circuit using a 0.8 μm CMOS double polysilicon, double metal process, and is offered in a plastic 28-pin SOIC package. Analog and digital supply connections are separated to isolate the analog circuitry from the digital supply and reduce digital crosstalk.

The AD1877 operates from a single +5 V power supply over the temperature range of 0°C to +70°C, and typically consumes less than 260 mW of power.

THEORY OF OPERATION

ΣΔ Modulator Noise-Shaping

The stereo, internally differential analog modulator of the AD1877 employs a proprietary feedforward and feedback architecture that passes input signals in the audio band with a unity transfer function yet simultaneously shapes the quantization noise generated by the one-bit comparator out of the audio band. See Figure 1. Without the ΣΔ architecture, this quantization noise would be spread uniformly from dc to one-half the oversampling frequency, 64 × F_S.

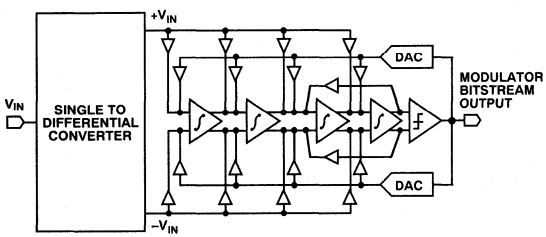


Figure 1. Modulator Noise-Shaper (One Channel)

ΣΔ architectures "shape" the quantization noise-transfer function in a nonuniform manner. Through careful design, this transfer function can be specified to high-pass filter the quantization noise out of the audio band into higher frequency regions. The AD1877 also incorporates a feedback resonator from the fourth integrator's output to the third integrator's input. This resonator does not affect the signal transfer function but allows the flexible placement of a zero in the noise transfer function for more effective noise shaping.

Oversampling by 64 simplifies the implementation of a high performance audio analog-to-digital conversion system. Antialias requirements are minimal; a single pole of filtering will usually suffice to eliminate inputs near F_S and its higher multiples.

A fourth-order architecture was chosen both to strongly shape the noise out of the audio band and to help break up the idle tones produced in all ΣΔ architectures. These architectures have a tendency to generate periodic patterns with a constant dc input, a response that looks like a tone in the frequency domain. These idle tones have a direct frequency dependence on the input dc offset and indirect dependence on temperature and time as it affects dc offset. The AD1877 suppresses idle tones 20 dB or better below the integrated noise floor.

The AD1877's modulator was designed, simulated, and exhaustively tested to remain stable for any input within a wide tolerance of its rated input range. The AD1877 is designed to internally reset itself should it ever be overdriven, to prevent it from going instable. It will reset itself within 5 μs at a 48 kHz sampling frequency after being overdriven. Overdriving the inputs will produce a waveform "clipped" to plus or minus full scale.

See Figures 7 through 12 for illustrations of the AD1877's typical analog performance as measured by an Audio Precision System One. Signal-to-(distortion + noise) is shown under a range of conditions. Note that there is a small variance between the AD1877 analog performance specifications and some of the performance plots. This is because the Audio Precision System One measures THD and noise over a 20 Hz to 24 kHz bandwidth, while the analog performance is specified over a 20 Hz to 20 kHz bandwidth (i.e., the AD1877 performs slightly better than the plots indicate). The power supply rejection (Figure 11) graph illustrates the benefits of the AD1877's internal differential architecture. The excellent channel separation shown in Figure 12 is the result of careful chip design and layout.

Digital Filter Characteristics

The digital decimator accepts the modulator's stereo bitstream and simultaneously performs two operations on it. First, the decimator low-pass filters the quantization noise that the modulator shaped to high frequencies and filters any other out-of-audio-band input signals. Second, it reduces the data rate to an output word rate equal to F_S. The high frequency bitstream is decimated to stereo 16-bit words at 48 kHz (or other desired F_S). The out-of-band one-bit quantization noise and other high frequency components of the bitstream are attenuated by at least 90 dB.

The AD1877 decimator implements a symmetric Finite Impulse Response (FIR) filter which possesses a linear phase response. This filter achieves a narrow transition band (0.1 × F_S), high stopband attenuation (> 90 dB), and low passband ripple (< 0.006 dB). The narrow transition band allows the unattenuated digitization of 20 kHz input signals with F_S as low as 44.1 kHz. The stopband attenuation is sufficient to eliminate modulator quantization noise from affecting the output. Low passband ripple prevents the digital filter from coloring the audio signal. See Figure 13 for the digital filter's characteristics. The output from the decimator is available as a single serial output, multiplexed between left and right channels.

Note that the digital filter itself is operating at 64 × F_S. As a consequence, Nyquist images of the passband, transition band, and stopband will be repeated in the frequency spectrum at multiples of 64 × F_S. Thus the digital filter will attenuate to greater than 90 dB across the frequency spectrum except for a window ±0.55 × F_S wide centered at multiples of 64 × F_S. Any input signals, clock noise, or digital noise in these frequency windows will not be attenuated to the full 90 dB. If the high frequency signals or noise appear within the passband images within these windows, they will not be attenuated at all, and therefore input antialias filtering should be applied.

Sample Delay

The sample delay or "group delay" of the AD1877 is dominated by the processing time of the digital decimation filter. FIR filters convolve a vector representing time samples of the input with an equal-sized vector of coefficients. After each convolution, the input vector is updated by adding a new sample at one end of the "pipeline" and discarding the oldest input sample at the other. For an FIR filter, the time at which a step input appears at the output will be when that step input is half way through the input sample vector pipeline. The input sample vec-

tor is updated every 64 × F_S. The equation which expresses the group delay for the AD1877 is:

Group Delay (sec) = 36/F_S (Hz)

For the most common sample rates this can be summarized as:

F_S	Group Delay
48 kHz	750 μs
44.1 kHz	816 μs
32 kHz	1125 μs

Due to the linear phase properties of FIR filters, the group delay variation, or differences in group delay at different frequencies is essentially zero.

OPERATING FEATURES

Voltage Reference and External Filter Capacitors

The AD1877 includes a +2.25 V on-board reference that determines the AD1877's input range. The left and right reference pins (14 and 15) should be bypassed with a 0.1 μF ceramic chip capacitor in parallel with a 4.7 μF tantalum as shown below in Figure 3. Note that the chip capacitor should be closest to the pin. The internal reference can be overpowered by applying an external reference voltage at the $V_{REF}L$ (Pin 14) and $V_{REF}R$ (Pin 15) pins, allowing multiple AD1877s to be calibrated to the same gain. It is not possible to overpower the left and right reference pins individually; the external reference voltage should be applied to both Pin 14 and Pin 15. Note that the reference pins must still be bypassed as shown in Figure 3.

It is possible to bypass each reference pin ($V_{REF}L$ and $V_{REF}R$) with a capacitor larger than the suggested 4.7 μF, however it is not recommended. A larger capacitor will have a longer charge-up time which may extend into the autocalibration period, yielding incorrect results.

The AD1877 requires four external filter capacitors on Pins 11, 12, 17 and 18. These capacitors are used to filter the single-to-differential converter outputs, and are too large for practical integration onto the die. They should be 470 pF NPO ceramic chip type capacitors as shown in Figure 3, placed as close to the AD1877 package as possible.

Sample Clock

An external master clock supplied to CLKIN (Pin 28) drives the AD1877 modulator, decimator, and digital interface. As with any analog-to-digital conversion system, the sampling clock must be low jitter to prevent conversion errors. If a crystal oscillator is used as the clock source, it should be bypassed with a 0.1 μF capacitor, as shown below in Figure 3.

For the AD1877, the input clock operates at either 256 × F_S or 384 × F_S as selected by the 384/$\overline{256}$ pin. When 384/$\overline{256}$ is HI, the 384 mode is selected and when 384/$\overline{256}$ is LO, the 256 mode is selected. In both cases, the clock is divided down to obtain the 64 × F_S clock required for the modulator. The output word rate itself will be at F_S. This relationship is illustrated for popular sample rates below:

256 Mode CLKIN	384 Mode CLKIN	Modulator Sample Rate	Output Word Rate
12.288 MHz	18.432 MHz	3.072 MHz	48 kHz
11.2896 MHz	16.9344 MHz	2.822 MHz	44.1 kHz
8.192 MHz	12.288 MHz	2.048 MHz	32 kHz

The AD1877 serial interface will support both master and slave modes. Note that in slave mode it is required that the serial interface clocks are externally derived from a common source. In master mode, the serial interface clock outputs are internally derived from CLKIN.

Reset, Autocalibration and Power Down

The active LO $\overline{RESET}$ pin (Pin 23) initializes the digital decimation filter and clears the output data buffer. While in the reset state, all digital pins defined as outputs of the AD1877 are driven to ground (except for BCLK, which is driven to the state defined by RDEDGE (Pin 6)). Analog Devices recommends resetting the AD1877 on initial power up so that the device is properly calibrated. The reset signal must remain LO for the minimum period specified in "Specifications" above. The reset pulse is asynchronous with respect to the master clock, CLKIN. If, however, multiple AD1877s are used in a system, and it is desired that they leave the reset state at the same time, the common reset pulse should be made synchronous to CLKIN (i.e., $\overline{RESET}$ should be brought HI on a CLKIN falling edge).

Multiple AD1877s can be synchronized to each other by using a single master clock and a single reset signal to initialize all devices. On coming out of reset, all AD1877s will begin sampling at the same time. Note that in slave mode, the AD1877 is inactive (and all outputs are static, including WCLK) until the first rising edge of $\overline{LRCK}$ after the first falling edge of $\overline{LRCK}$. This initial low going then high going edge of $\overline{LRCK}$ can be used to "skew" the sampling start-up time of one AD1877 relative to other AD1877s in a system. In the Data Position Controlled by WCLK Input mode, WCLK must be HI with $\overline{LRCK}$ HI, then WCLK HI with $\overline{LRCK}$ LO, then WCLK HI with $\overline{LRCK}$ HI before the AD1877 starts sampling.

The AD1877 achieves its specified performance without the need for user trims or adjustments. This is accomplished through the use of on-chip automatic offset calibration that takes place immediately following reset. This procedure nulls out any offsets in the single-to-differential converter, the analog modulator and the decimation filter. Autocalibration completes in approximately 8192 × (1/($F_{\overline{LRCK}}$) seconds, and need only be performed once at power-up in most applications. [In slave mode, the 8192 cycles required for autocalibration do not start until after the first rising edge of $\overline{LRCK}$ following the first falling edge of $\overline{LRCK}$.] The autocalibration scheme assumes that the inputs are ac coupled. DC coupled inputs will work with the AD1877, but the autocalibration algorithm will yield an incorrect offset compensation.

The AD1877 also features a power-down mode. It is enabled by the active LO $\overline{RESET}$ Pin 23 (i.e., the AD1877 is in power-down mode while $\overline{RESET}$ is held LO). The power savings are specified in the "Specifications" section above. The converter is shut down in the power-down state and will not perform conversions. The AD1877 will be reset upon leaving the power-down state, and autocalibration will commence after the $\overline{RESET}$ pin goes HI.

Power consumption can be further reduced by slowing down the master clock input (at the expense of input passband width). Note that a minimum clock frequency, F_{CLKIN}, is specified for the AD1877.

Tag Overrange Output

The AD1877 includes a TAG serial output (Pin 27) which is provided to indicate status on the level of the input voltage. The TAG output is at TTL compatible logic levels. A pair of unsigned binary bits are output, synchronous with $L\overline{R}CK$ (MSB then LSB), that indicate whether the current signal being converted is: more than 1 dB under full scale; within 1 dB under full scale; within 1 dB over full scale; or more than 1 dB over full scale. The timing for the TAG output is shown in Figures 14 through 23. Note that the TAG bits are not "sticky," i.e., they are not peak reading, but rather change with every sample. Decoding of these two bits is as follows:

TAG Bits MSB, LSB		Meaning
0	0	More Than 1 dB Under Full Scale
0	1	Within 1 dB Under Full Scale
1	0	Within 1 dB Over Full Scale
1	1	More Than 1 dB Over Full Scale

APPLICATIONS ISSUES

Recommended Input Structure

The AD1877 input structure is single-ended to allow the board designer to achieve a high level of functional integration. The very simple recommended input circuit is shown in Figure 2. Note the 1 μF ac coupling capacitor which allows input level shifting for +5 V only operation, and for autocalibration to properly null offsets. The 3 dB point of the single-pole antialias RC filter is 240 kHz, which results in essentially no attenuation at 20 kHz. Attenuation at 3 MHz is approximately 22 dB, which is adequate to suppress F_S noise modulation. If the analog inputs are externally ac coupled, then the 1 μF ac coupling capacitors shown in Figure 2 are not required.

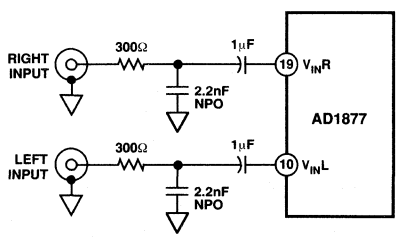


Figure 2. Recommended Input Structure for Externally DC Coupled Inputs

Analog Input Voltage Swing

The single-ended input range of the analog inputs is specified in relative terms in the "Specifications" section of this data sheet. The input level at which clipping occurs linearly tracks the voltage reference level, i.e., if the reference is high relative to the typical 2.25 V, the allowable input range without clipping is correspondingly wider; if the reference is low relative to the typical 2.25 V, the allowable input range is correspondingly narrower.

Thus the maximum input voltage swing can be computed using the following ratio:

$$\frac{2.25\ V\ (nominal\ reference\ voltage)}{3.1\ V\ p\text{-}p\ (nominal\ voltage\ swing)} = \frac{X\ Volts\ (measured\ reference\ voltage)}{Y\ Volts\ (maximum\ swing\ without\ clipping)}$$

Layout and Decoupling Considerations

Obtaining the best possible performance from the AD1877 requires close attention to board layout. Adhering to the following principles will produce typical values of 92 dB dynamic range and 90 dB S/(THD+N) in target systems. Schematics and layout artwork of the AD1877 Evaluation Board, which implement these recommendations, are available from Analog Devices.

The principles and their rationales are listed below. The first two pertain to bypassing and are illustrated in Figure 3.

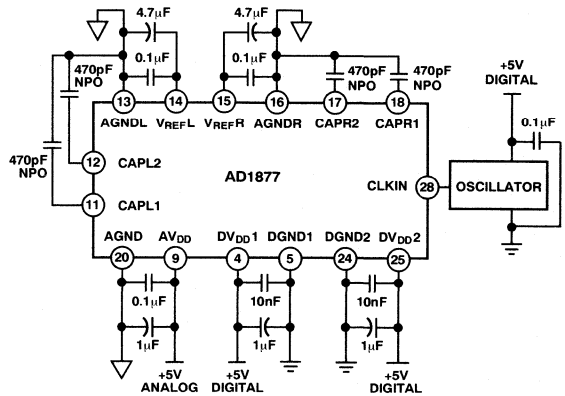


Figure 3. Recommended Bypassing and Oscillator Circuits

There are two pairs of digital supply pins on opposite sides of the part (Pins 4 & 5 and Pins 24 & 25). The user should tie a bypass chip capacitor (10 nF ceramic) in parallel with a decoupling capacitor (1 μF tantalum) on EACH pair of supply pins as close to the pins as possible. The traces between these package pins and the capacitors should be as short and as wide as possible. This will prevent digital supply current transients from being inductively transmitted to the inputs of the part.

Use a 0.1 μF chip analog capacitor in parallel with a 1.0 μF tantalum capacitor from the analog supply (Pin 9) to the analog ground plane. The trace between this package pin and the capacitor should be as short and as wide as possible.

The AD1877 should be placed on a split ground plane. The digital ground plane should be placed under the top end of the package, and the analog ground plane should be placed under the bottom end of the package as shown in Figure 4. The split should be between Pins 8 & 9 and between Pins 20 & 21. The ground planes should be tied together at one spot underneath the center of the package with an approximately 3 mm trace. This ground plane technique also minimizes RF transmission and reception.

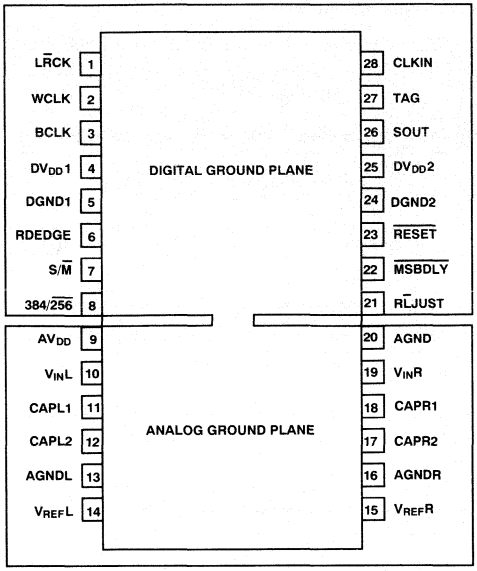


Figure 4. Recommended Ground Plane

Each reference pin (14 & 15) should be bypassed with a 0.1 μF ceramic chip capacitor in parallel with a 4.7 μF tantalum capacitor. The 0.1 μF chip cap should be placed as close to the package pin as possible, and the trace to it from the reference pin should be as short and as wide as possible. Keep this trace away from any analog traces (Pins 10, 11, 12, 17, 18, 19)! Coupling between input and reference traces will cause even order harmonic distortion. If the reference is needed somewhere else on the printed circuit board, it should be shielded from any signal dependent traces to prevent distortion.

Wherever possible, minimize the capacitive load on the digital outputs of the part. This will reduce the digital spike currents drawn from the digital supply pins and help keep the IC substrate quiet.

How to Extend SNR

A cost-effective method of improving the dynamic range and SNR of an analog-to-digital conversion system is to use multiple AD1877 channels in parallel with a common analog input. This technique makes use of the fact that the noise in independent modulator channels is uncorrelated. Thus every doubling of the number of AD1877 channels used will improve system dynamic range by 3 dB. The digital outputs from the corresponding decimator channels have to be arithmetically averaged to obtain the improved results in the correct data format. A microprocessor, either general-purpose or DSP, can easily perform the averaging operation.

Shown below in Figure 5 is a circuit for obtaining a 3 dB improvement in dynamic range by using both channels of a single AD1877 with a mono input. A stereo implementation would require using two AD1877s and using the recommended input structure shown above in Figure 2. Note that a single microprocessor would likely be able to handle the averaging requirements for both left and right channels.

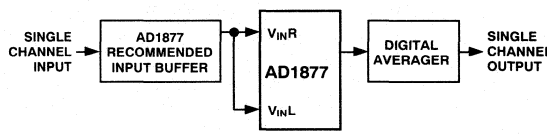


Figure 5. Increasing Dynamic Range By Using Two AD1877 Channels

DIGITAL INTERFACE

Modes of Operation

The AD1877's flexible serial output port produces data in twos-complement, MSB-first format. The input and output signals are TTL logic level compatible. Time multiplexed serial data is output on SOUT (Pin 26), left channel then right channel, as determined by the left/right clock signal LRCK (Pin 1). Note that there is no method for forcing the right channel to precede the left channel. The port is configured by pin selections. The AD1877 can operate in either master or slave mode, with the data in right-justified, I²S-compatible, Word Clock controlled or left-justified positions.

The various mode options are pin-programmed with the Slave/Master Pin (7), the Right/Left Justify Pin (21), and the MSB/Delay Pin (22). The function of these pins is summarized as follows:

S/$\overline{M}$	RLJUST	$\overline{MSBDLY}$	WCLK	BCLK	L$\overline{R}$CK	Serial Port Operation Mode
1	1	1	Output	Input	Input	Slave Mode. WCLK frames the data. The MSB is output on the 17th BCLK cycle. Provides right-justified data in slave mode with a 64 × F_S BCLK frequency. See Figure 14.
1	1	0	Input	Input	Input	Slave Mode. The MSB is output in the BCLK cycle after WCLK is detected HI. WCLK is sampled on the BCLK active edge, with the MSB valid on the next BCLK active edge. Tying WCLK HI results in I^2S-justified data. See Figure 15.
1	0	1	Output	Input	Input	Slave Mode. Data left-justified with WCLK framing the data. WCLK rises immediately after an L$\overline{R}$CK transition. The MSB is valid on the first BCLK active edge. See Figure 16.
1	0	0	Output	Input	Input	Slave Mode. Data I^2S-justified with WCLK framing the data. WCLK rises in the second BCLK cycle after an L$\overline{R}$CK transition. The MSB is valid on the second BCLK active edge. See Figure 17.
0	1	1	Output	Output	Output	Master Mode. Data right-justified. WCLK frames the data, going HI in the 17th BCLK cycle. BCLK frequency = 64 × F_S. See Figure 18.
0	1	0	Output	Output	Output	Master Mode. Data right-justified + 1. WCLK is pulsed in the 17th BCLK cycle, staying HI for only 1 BCLK cycle. BCLK frequency = 64 × F_S. See Figure 19.
0	0	1	Output	Output	Output	Master Mode. Data left-justified. WCLK frames the data. BCLK frequency = 64 × F_S. See Figure 20.
0	0	0	Output	Output	Output	Master Mode. Data I^2S-justified. WCLK frames the data. BCLK frequency = 64 × F_S. See Figure 21.

Serial Port Data Timing Sequences

The RDEDGE input (Pin 6) selects the bit clock (BCLK) polarity. RDEDGE HI causes data to be transmitted on the BCLK falling edge and valid on the BCLK rising edge; RDEDGE LO causes data to be transmitted on the BCLK rising edge and valid on the BCLK falling edge. This is shown in the serial data output timing diagrams. The term "sampling" is used generically to denote the BCLK edge (rising or falling) on which the serial data is valid. The term "transmitting" is used to denote the other BCLK edge. The S/$\overline{M}$ input (Pin 7) selects slave mode (S/$\overline{M}$ HI) or master mode (S/$\overline{M}$ LO). Note that in slave mode, BCLK may be continuous or gated (i.e., a stream of pulses during the data phase followed by periods of inactivity between channels).

In the master modes, the bit clock (BCLK), the left/right clock (L$\overline{R}$CK), and the word clock (WCLK) are always outputs, generated internally in the AD1877 from the master clock (CLKIN) input. In master mode, a L$\overline{R}$CK cycle defines a 64-bit "frame." L$\overline{R}$CK is HI for a 32-bit "field" and L$\overline{R}$CK is LO for a 32-bit "field."

In the slave modes, the bit clock (BCLK), and the left/right clock (L$\overline{R}$CK) are user-supplied inputs. The word clock (WCLK) is an internally generated output except when S/$\overline{M}$ is HI, RLJUST is HI, and $\overline{MSBDLY}$ is LO, when it is a user-supplied input which controls the data position. Note that the AD1877 does not support asynchronous operation in slave mode; the clocks (CLKIN, L$\overline{R}$CK, BCLK and WCLK) must be externally derived from a common source. In general, CLKIN should be divided down externally to create L$\overline{R}$CK, BCLK and WCLK.

In the slave modes, the relationship between L$\overline{R}$CK and BCLK is not fixed, to the extent that there can be an arbitrary number of BCLK cycles between the end of the data transmission and the next L$\overline{R}$CK transition. The slave mode timing diagrams are therefore simplified as they show precise 32-bit fields and 64-bit frames.

In two slave modes, it is possible to pack two 16-bit samples in a single 32-bit frame, as shown in Figure 22 and 23. BCLK, L$\overline{R}$CK, DATA and TAG operate at one half the frequency (twice the period) as in the 64-bit frame modes. This 32-bit frame mode is enabled by pulsing the L$\overline{R}$CK HI for a minimum of one BCLK period to a maximum of sixteen BCLK periods. The L$\overline{R}$CK HI for one BCLK period case is shown in Figures 22 and 23. With a one or two BCLK period HI pulse on L$\overline{R}$CK, note that both the left and right TAG bits are output immediately, back-to-back. With a three to sixteen BCLK period HI pulse on L$\overline{R}$CK, the left TAG bits are followed by one to fourteen "dead" cycles (i.e., zeros) followed by the right TAG bits. Also note that WCLK stays HI continuously when the AD1877 is in the 32-bit frame mode. Figure 22 illustrates the left-justified case, while Figure 23 illustrates the I^2S-justified case.

In all modes, the left and right channel data is updated with the next sample within the last 1/8 of the current conversion cycle (i.e., within the last 4 BCLK cycles in 32-bit frame mode, and within the last 8 BCLK cycles in 64-bit frame mode). The user must constrain the output timing such that the MSB of the right channel is read before the final 1/8 of the current conversion period.

Two modes deserve special discussion. The first special mode, "Slave Mode, Data Position Controlled by WCLK Input" (S/$\overline{M}$ = HI, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO), shown in Figure 15, is the only mode in which WCLK is an input. The 16-bit output data words can be placed at user-defined locations within 32-bit fields. The MSB will appear in the BCLK period after WCLK is detected HI by the BCLK sampling edge. If WCLK is HI during the first BCLK of the 32-bit field (if WCLK is tied HI for example), then the MSB of the output word will be valid on the sampling edge of the second BCLK. The effect is to delay the MSB for one bit clock cycle into the field, making the output data compatible at the data format level with the I^2S data format. Note that the relative placement of the WCLK input can vary from 32-bit field to 32-bit field, even within the same 64-bit frame. For example, within a single 64-bit frame, the left word could be right justified (by pulsing WCLK HI on the 16th BCLK) and the right word could be in an I^2S compatible data format (by having WCLK HI at the beginning of the second field).

In the second special mode "Master Mode, Right-Justified with MSB Delay, WCLK Pulsed in 17th Cycle" (S/$\overline{M}$ = LO, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO), shown in Figure 19, WCLK is an output and is pulsed for one cycle by the AD1877. The MSB is valid on the 18th BCLK sampling edge, and the LSB extends into the first BCLK period of the next 32-bit field.

Timing Parameters

For master modes, a BCLK transmitting edge (labeled "XMIT") will be delayed from a CLKIN rising edge by t_{DLYCKB}, as shown in Figure 24. A L$\overline{R}$CK transition will be delayed from a BCLK transmitting edge by t_{DLYBLR}. A WCLK rising edge will be delayed from a BCLK transmitting edge by t_{DLYBWR}, and a WCLK falling edge will be delayed from a BCLK transmitting edge by t_{DLYBWF}. The DATA and TAG outputs will be delayed from a transmitting edge of BCLK by t_{DLYDT}.

For slave modes, an L$\overline{R}$CK transition must be setup to a BCLK sampling edge (labeled "SAMPLE") by $t_{SETLRBS}$. The DATA and TAG outputs will be delayed from an L$\overline{R}$CK transition by $t_{DLYLRDT}$, and DATA and TAG outputs will be delayed from a BCLK transmitting edge by t_{DLYBDT}. For "Slave Mode, Data Position Controlled by WCLK Input," WCLK must be setup to a BCLK sampling edge by t_{SETWBS}.

For both master and slave modes, BCLK must have a minimum LO pulse width of t_{BPWL}, and a minimum HI pulse width of t_{BPWH}.

The AD1877 CLKIN and $\overline{RESET}$ timing is shown in Figure 26. CLKIN must have a minimum LO pulse width of t_{CPWL}, and a minimum HI pulse width of t_{CPWH}. The minimum period of CLKIN is given by t_{CLKIN}. $\overline{RESET}$ must have a minimum LO pulse width of t_{RPWL}. Note that there are no setup or hold time requirements for $\overline{RESET}$.

Synchronizing Multiple AD1877s

Multiple AD1877s can be synchronized by making all the AD1877s serial port slaves. This option is illustrated in Figure 6. See the "Reset, Autocalibration and Power Down" section above for additional information.

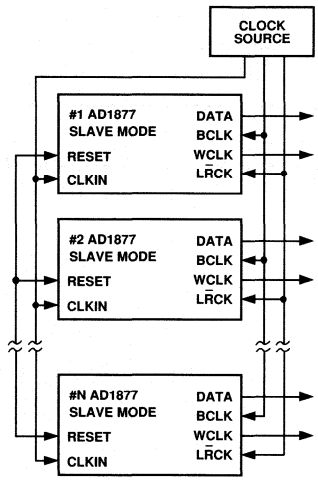


Figure 6. Synchronizing Multiple AD1877s

AD1877—Typical Performance

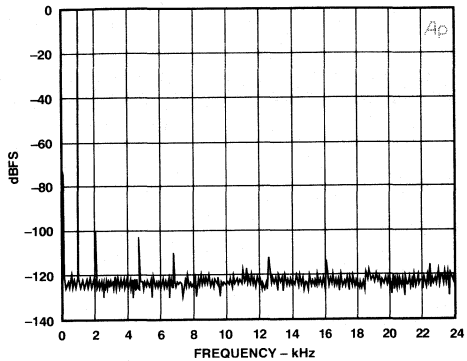


Figure 7. 1 kHz Tone at −0.5 dBFS (16k-Point FFT)

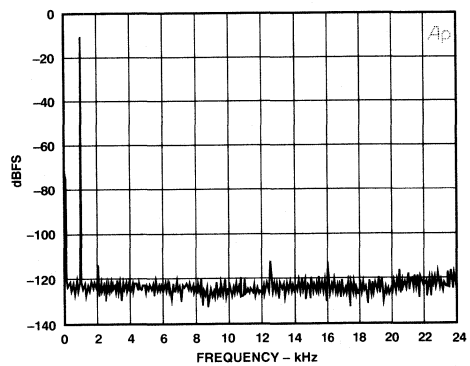


Figure 8. 1 kHz Tone at −10 dBFS (16k-Point FFT)

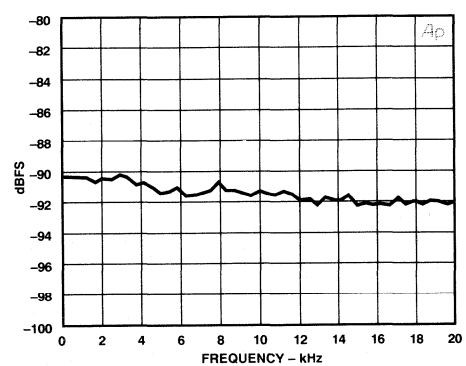


Figure 9. THD+N versus Frequency at −0.5 dBFS

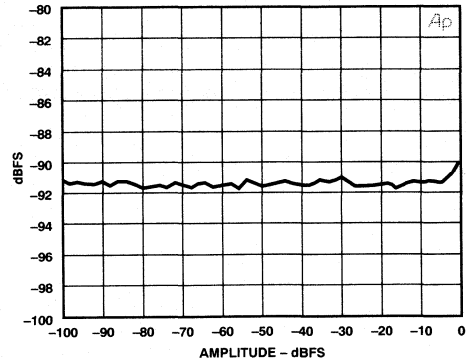


Figure 10. THD+N versus Amplitude at 1 kHz

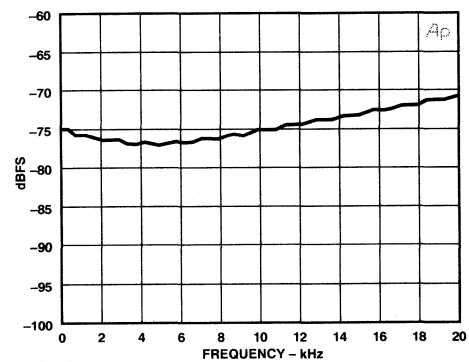


Figure 11. Power Supply Rejection to 300 mV p-p on AV_{DD}

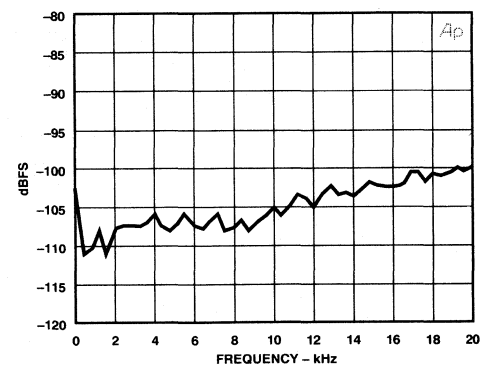


Figure 12. Channel Separation versus Frequency at −0.5 dBFS

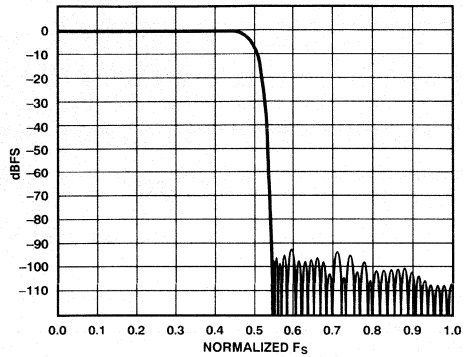


Figure 13. Digital Filter Signal Transfer Function to F_S

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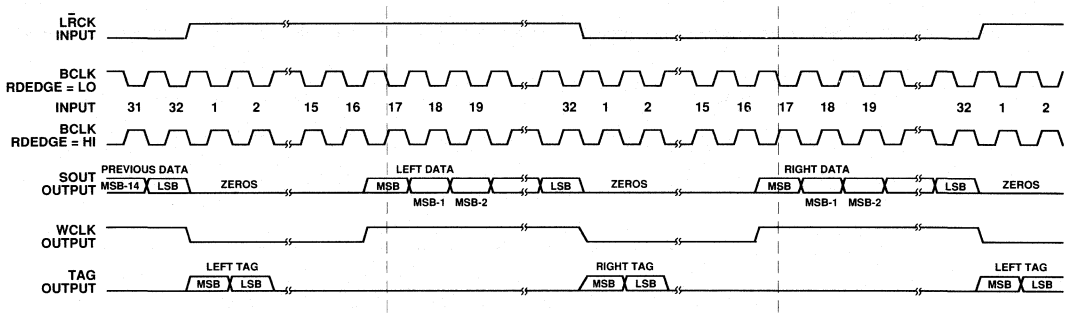


Figure 14. Serial Data Output Timing: Slave Mode, Right-Justified with No MSB Delay, $S/\overline{M}$ = HI, $R\overline{L}JUST$ = HI, $\overline{MSBDLY}$ = HI

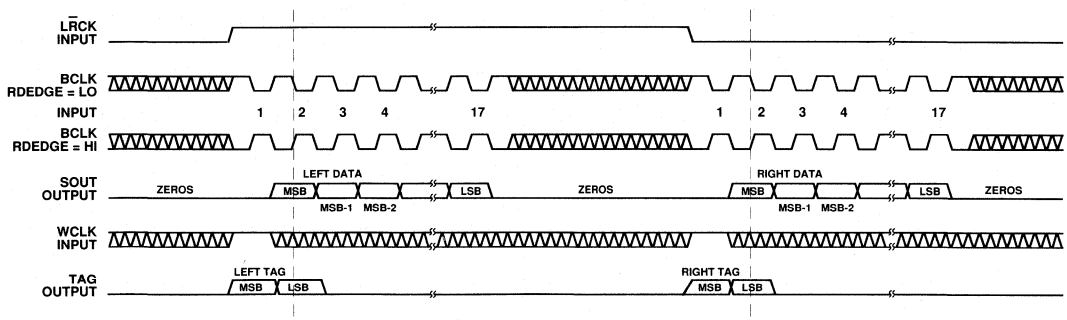


Figure 15. Serial Data Output Timing: Slave Mode, Data Position Controlled by WCLK Input, $S/\overline{M}$ = HI, $R\overline{L}JUST$ = HI, $\overline{MSBDLY}$ = LO

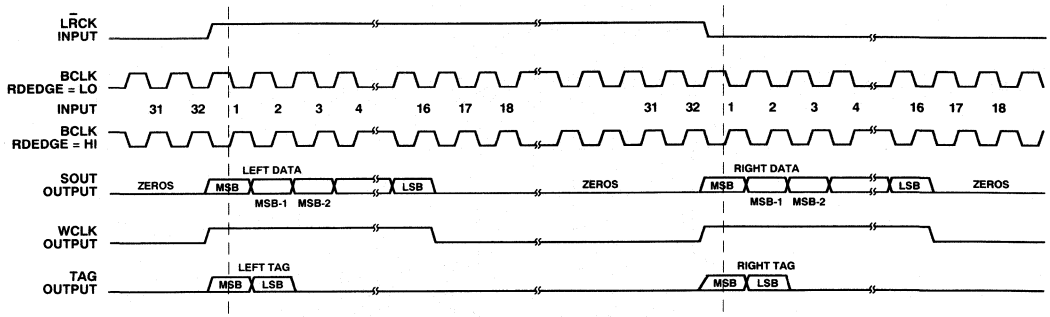


Figure 16. Serial Data Output Timing: Slave Mode, Left-Justified with No MSB Delay, S/$\overline{M}$ = HI, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = HI

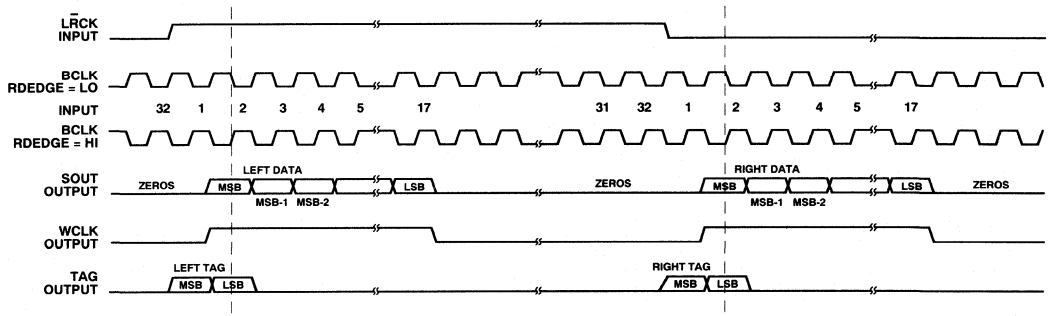


Figure 17. Serial Data Output Timing: Slave Mode, I²S-Justified, S/$\overline{M}$ = HI, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = LO

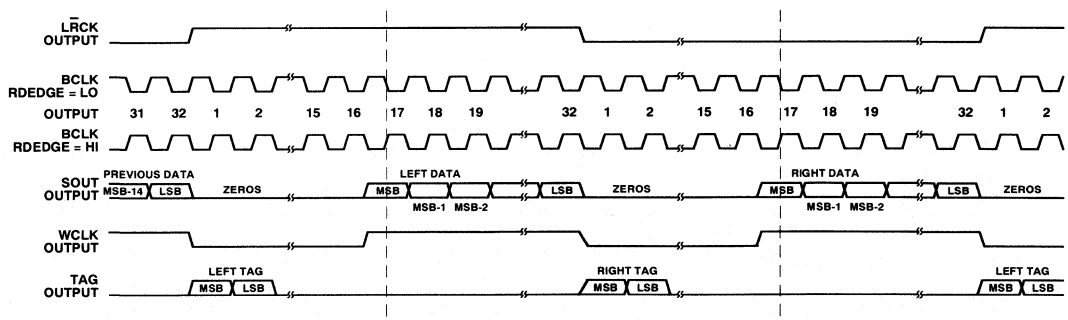


Figure 18. Serial Data Output Timing: Master Mode, Right-Justified with No MSB Delay, S/$\overline{M}$ = LO, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = HI

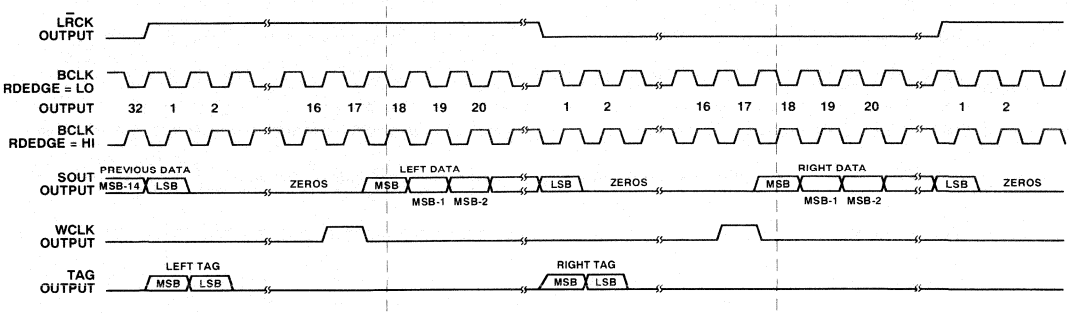


Figure 19. Serial Data Output Timing: Master Mode, Right-Justified with MSB Delay, WCLK Pulsed in 17th BCLK Cycle, S/$\overline{M}$ = LO, R$\overline{L}$JUST = HI, $\overline{MSBDLY}$ = LO

4

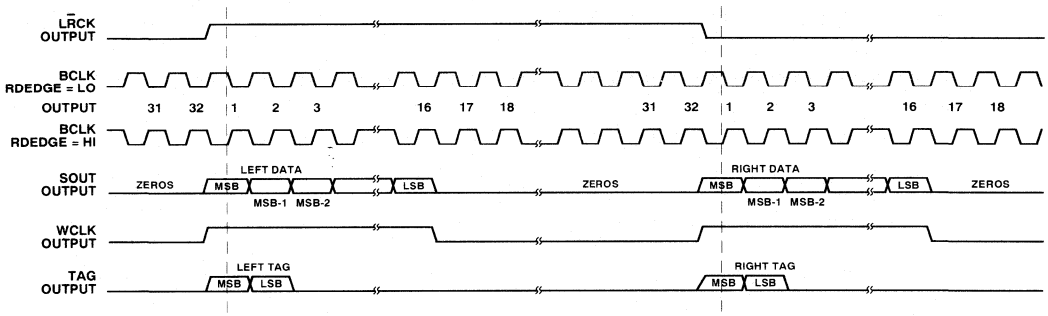


Figure 20. Serial Data Output Timing: Master Mode, Left-Justified with No MSB Delay, S/$\overline{M}$ = LO, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = HI

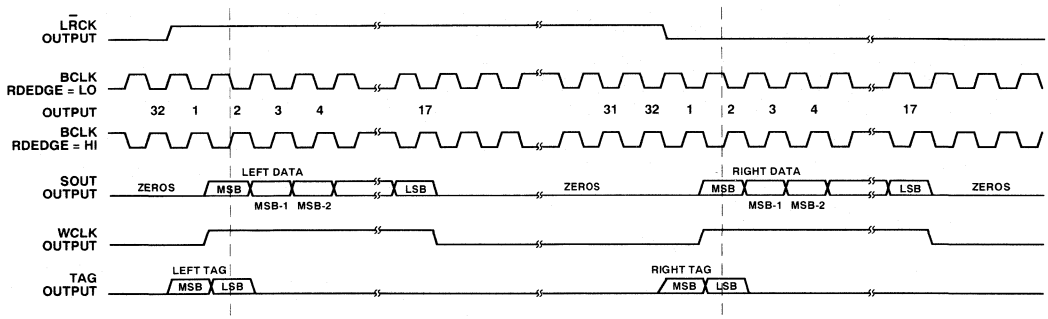


Figure 21. Serial Data Output Timing: Master Mode, I²S-Justified, S/$\overline{M}$ = LO, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = LO

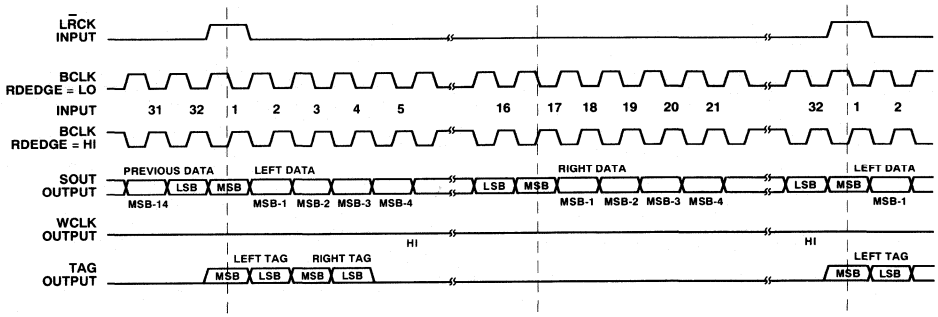


Figure 22. Serial Data Output Timing: Slave Mode, Left-Justified with No MSB Delay, 32-Bit Frame Mode, S/$\overline{M}$ = HI, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = HI

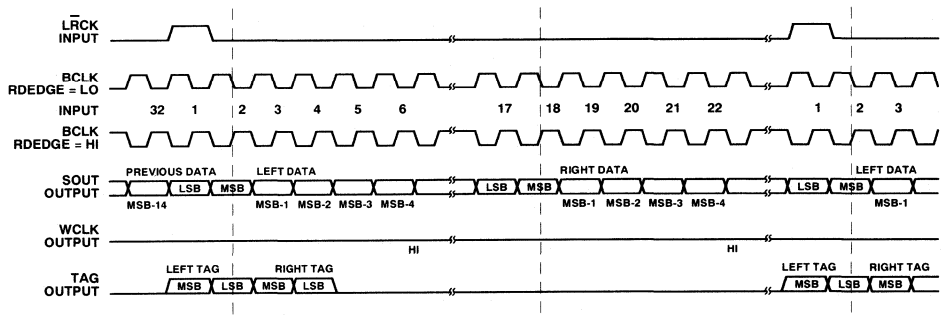


Figure 23. Serial Data Output Timing: Slave Mode, I²S-Justified, 32-Bit Frame Mode, S/$\overline{M}$ = HI, R$\overline{L}$JUST = LO, $\overline{MSBDLY}$ = LO

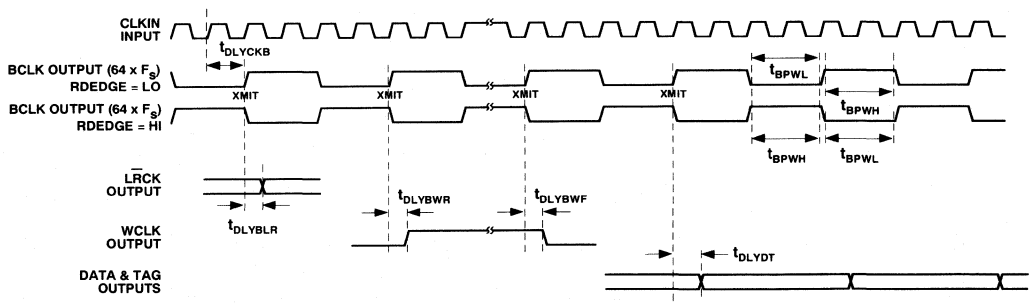


Figure 24. Master Mode Clock Timing

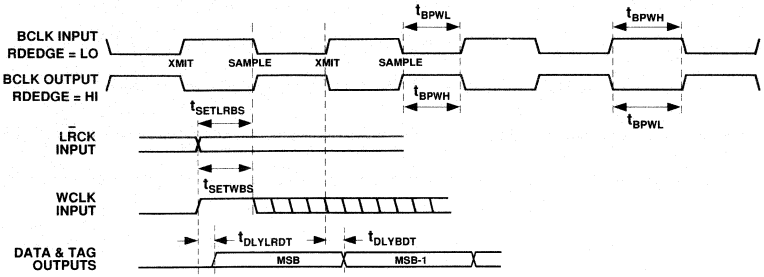


Figure 25. Slave Mode Clock Timing

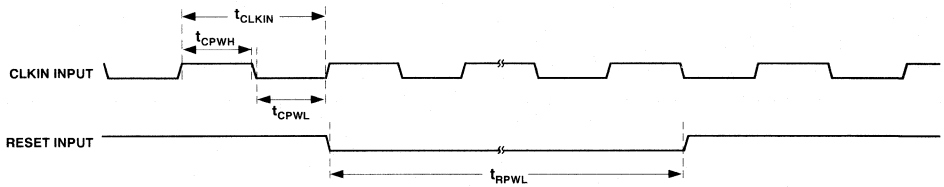


Figure 26. CLKIN and $\overline{\text{RESET}}$ Timing

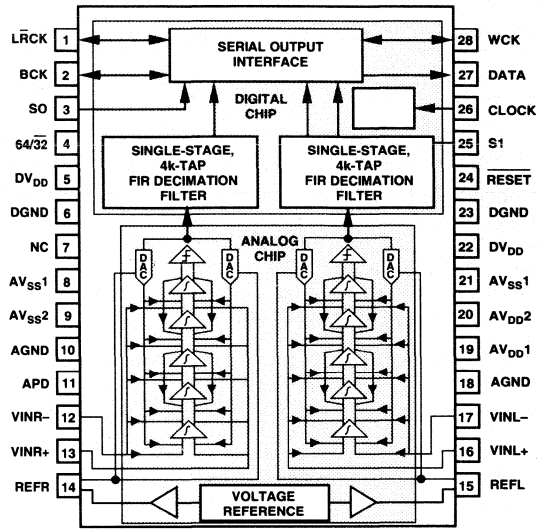
High Performance 16/18-Bit ΣΔ Stereo ADCs

AD1878/AD1879*

FEATURES
Fully Differential Dual Channel Analog Inputs
103 dB Signal-to-Noise (AD1879 typ)
−98 dB THD+N (AD1879 typ)
0.001 dB Passband Ripple and 115 dB Stopband Attenuation
Fifth-Order, 64 Times Oversampling ΣΔ Modulator
Single Stage, Linear Phase Decimator
256 × F_S Input Clock

APPLICATIONS
Digital Tape Recorders
Professional, DCC, and DAT
A/V Digital Amplifiers
CD-R
Sound Reinforcement

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT OVERVIEW

The AD1879 is a two-channel, 18-bit oversampling ADC based on ΣΔ technology and intended primarily for digital audio applications. The AD1878 is identical to the 18-bit AD1879 except that it outputs 16-bit data words. Statements in this data sheet should be read as applying to both parts unless otherwise noted.

Each input channel of these ADCs is fully differential. Each data conversion channel consists of a fifth order one-bit noise shaping modulator and a digital decimation filter. An on-chip voltage reference provides a voltage source to both channels stable over temperature and time. Digital output data from both channels is time-multiplexed to a single, flexible serial interface. The AD1878/AD1879 accepts a 256 × F_S input master clock.

Input signals are sampled at 64 × F_S on switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The AD1878/AD1879's proprietary fifth-order differential switched-capacitor modulator architecture shapes the one-bit comparator's quantization noise out of the audio passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the AD1878/AD1879 to very low levels. The AD1878/AD1879's differential architecture provides increased dynamic range and excellent common-mode rejection characteristics. Because its modulator is single-bit, AD1878/AD1879 is inherently monotonic and has no mechanism for producing differential linearity errors.

The digital decimation filters are single-stage, 4095-tap finite impulse response filters for filtering the modulator's high frequency quantization noise and reducing the 64 × F_S single-bit output data rate to a F_S word rate. They provide linear phase and a narrow transition band that permits the digitization of 20 kHz signals while preventing aliasing into the passband even when using a 44.1 kHz sampling frequency. Passband ripple is less the 0.001 dB, and stopband attenuation exceeds 115 dB.

The flexible serial output port produces data in twos-complement, MSB-first format. Input and output signals are to TTL and CMOS-compatible logic levels. The port is configured by pin selections. The AD1878/AD1879 can operate in either master or slave mode. Each 16/18-bit output word of a stereo pair can be formatted within a 32-bit field as either right-justified, I^2S-compatible, or at user-selected positions. The output can also be truncated to 16-bits by formatting into a 16-bit field.

The AD1878/AD1879 consists of two integrated circuits in a single ceramic 28-pin DIP package. The modulators and reference are fabricated in a BiCMOS process; the decimator and output port, in a 1.0 μm CMOS process. Separating these functions reduces digital crosstalk to the analog circuitry. Analog and digital supply connections are separated to further isolate the analog circuitry from the digital supplies.

The AD1878/AD1879 operates from ±5 V power supplies over the temperature range of −25°C to +70°C.

*Protected by U.S. Patent Numbers 5055843, 5126653, and others pending.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

AD1878/AD1879—SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	±5	V
Ambient Temperature	25	°C
Input Clock (F_{CLOCK})	12.288	MHz
Input Signal	974	Hz
	−0.5	dB Full Scale

All minimums and maximums tested except as noted.

ANALOG PERFORMANCE

	Min	Typ	Max	Units
AD1879 Resolution		18		Bits
AD1878 Resolution		16		Bits
Clock Input Frequency Range				
CLOCK Input (F_{CLOCK})	0.01	12.288	14.286	MHz
Modulator Sample Rate ($F_{CLOCK}/4$)	0.0025	3.072	3.5715	MHz
Output Word Rate ($F_S = F_{CLOCK}/256$)	0.039	48	55.8	kHz
AD1879 Dynamic Range (0 kHz to 20 kHz, −60 dB input)				
Stereo Mode (No A-Weight Filter)	100	103		dB
Mono Mode[1] (No A-Weight Filter)		106		dB
Stereo Mode (with A-Weight Filter)		105		dB
AD1879 Trimmed[2] Signal to (Noise + Distortion)				
Full Scale	93	98		dB
−20 dB		83		dB
AD1879 Untrimmed[3] Signal to (Noise + Distortion)				
Full Scale	91	96		dB
−20 dB		83		dB
AD1879 Trimmed[2] Signal to Total Harmonic Distortion				
Full Scale		98		dB
−20 dB		100		dB
AD1878 Dynamic Range (0 kHz to 20 kHz, −60 dB 1.0936 kHz Input Dithered with a −10 dB 21.873 kHz Sine Wave)				
Stereo Mode (No A-Weight Filter)	95	97		dB
AD1878 Trimmed[2] Signal to (Noise + Distortion)				
Full Scale	93	95		dB
−20 dB		77		dB
AD1878 Untrimmed[3] Signal to (Noise + Distortion)				
Full Scale	91	94		dB
−20 dB		77		dB
AD1878 Trimmed[2] Signal to Total Harmonic Distortion				
Full Scale		98		dB
−20 dB		100		dB
Analog Inputs				
Differential Input Range[4]	±5.985	±6.3	±6.615	V
Input Impedance at Each Input Pin		7.0		kΩ
DC Accuracy				
Gain Error		±1	±5	%
Interchannel Gain Mismatch		0.05	0.15	dB
Gain Drift		150		ppm/°C
AD1879 Midscale Offset Error		±200	±750	18-Bit LSBs
AD1878 Midscale Offset Error		±50	±200	16-Bit LSBs
Midscale Drift		13		ppm/°C
Voltage Reference	2.4	2.86	3.2	V
Crosstalk (EIAJ Method)	100	105		dB
Interchannel Phase Deviation		±0.001		Degrees

NOTES

[1]Both channels connected together for mono operations as described below in "How to Extend SNR."

[2]Differential gain imbalance manually trimmed to eliminate second harmonic. See "Applications Issues" below.

[3]Test performed without part-to-part trimming.

[4]The differential input range is twice the range seen at each input pin. The input range corresponds to the full-scale digital output range.

Specifications subject to change without notice.

DIGITAL INPUTS

	Min	Max	Units
V_{IH}			V
V_{IL}		0.8	V
I_{IH} @ V_{IH} = 5 V		10	μA
I_{IL} @ V_{IL} = 0 V		10	μA
V_{OH} @ I_{OH} = 360 μA	4.0		V
V_{OL} @ I_{OL} = 1.6 mA		0.5	V

DIGITAL TIMING

		Min	Typ	Max	Units
CLOCK					
Period (T_{CLOCK} = $1/F_{CLOCK}$)		0.07		100	μs
LO Pulse Width		35			ns
HI Pulse Width		35			ns
BCK Pulse Width			2		CLOCK Periods
64-Bit Frame LRCK Pulse Width			32		BCK Periods
32-Bit Frame LRCK Pulse Width			16		BCK Periods
WCK Pulse Width		1			BCK Periods
t_{RSET}	$\overline{\text{RESET}}$ Setup to CLOCK Rising	5			ns
t_{RHLD}	$\overline{\text{RESET}}$ Hold from CLOCK Rising	20			ns
t_{RSLS}	$\overline{\text{RESET}}$ Pulse Width	4		10 μs	CLOCK Periods
t_{WSET}	WCK to CLOCK Rising	5			ns
t_{WHLD}	WCK Hold from CLOCK Rising	20			ns
t_{DLYCK}	CLOCK to BCK/WCK/LRCK Delay (Master Mode)			65	ns
t_{SET}	BCK/LRCK to CLOCK Falling (Slave Mode)	5			ns
t_{HLD}	BCK/LRCK Hold from CLOCK Falling (Slave Mode)	20			ns
$t_{DLYD, MSB}$	CLOCK Falling to MSB DATA Delay			65	ns
t_{DLYD}	CLOCK Rising to DATA Delay, Except MSB			70	ns

POWER

	Min	Typ	Max	Units
Supplies				
Voltage, $DV_{DD}/AV_{DD}1/AV_{DD}2$	4.75	5	5.25	V
Voltage, $AV_{SS}1/AV_{SS}2$	−5.25	−5	−4.75	V
Current, $AV_{DD}1/AV_{SS}1$		73	92	mA
Current, $AV_{DD}1/AV_{SS}1$—Power Down		13	23	mA
Current, $AV_{DD}2/AV_{SS}2$		8	10	mA
Current, DV_{DD}		64	70	mA
Dissipation				
Operation		1,130	1,370	mW
Operation—Analog Supplies		810	1,020	mW
Operation—Digital Supplies		320	350	mW
Power Down (All Supplies)		530	680	mW
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		102		dBFS
Passband—Any 300 mV p-p Signal		92		dBFS
Stopband—Any 300 mV p-p Signal		105		dBFS

TEMPERATURE RANGE

	Min	Typ	Max	Units
Specifications Guaranteed		25		°C
Functionality Guaranteed	−25		+70	°C
Storage	−60		+100	°C

ABSOLUTE MAXIMUM RATINGS

	Min	Typ	Max	Units
DV_{DD} to DGND and $AV_{DD}1/AV_{DD}2$ to AGND	0		6	V
$AV_{SS}1/AV_{SS}2$ to AGND	−6		0	V
$AV_{SS}2$ to $AV_{SS}1$	−0.3			V
Digital inputs to DGND	−0.3		DV_{DD} + 0.3	V
Analog inputs	$AV_{SS}1$ − 0.3		$AV_{DD}1$ + 0.3	V
AGND to DGND	−0.3		0.3	V
Reference Voltage		Indefinite Short Circuit to Ground		
Soldering			+300	°C
			10	sec

DIGITAL FILTER CHARACTERISTICS

	Min	Typ	Max	Units
Decimation Factor		64		
Passband Ripple			0.001	dB
Stopband[1] Attenuation	115			dB
48 kHz F_S (12.288 MHz CLOCK)				
Passband	0		21.7	kHz
Stopband	26.2		3,045	kHz
44.1 kHz F_S (11.2896 MHz CLOCK)				
Passband	0		20.0	kHz
Stopband	24.1		2,798	kHz
32 kHz F_S (8.192 MHz CLOCK)				
Passband	0		14.5	kHz
Stopband	17.5		2,030	kHz
Other F_S				
Passband	0		0.4535	F_S
Stopband	0.5458		63.4542	F_S
Group Delay ([4096/2]/[64 × F_S])		$32/F_S$		
Group Delay Variation			0	μs

NOTE

[1]Stopband repeats itself at multiples of 64 × F_S, where F_S is the output word rate. Thus the digital filter will attenuate to 115 dB across the frequency spectrum except for a range ±0.5458 × F_S wide at multiples of 64 × F_S.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1878JD	−25°C to +70°C	Ceramic DIP	D-28
AD1879JD	−25°C to +70°C	Ceramic DIP	D-28

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1878/AD1879 feature proprietary ESD protection circuitry, permanent damage may still occur on devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradations or loss of functionality.

SamplePort Stereo Asynchronous Sample Rate Converters

AD1890/AD1891

FEATURES

- Automatically Sense Sample Frequencies—No Programming Required
- Tolerant of Sample Clock Jitter
- Smooth Transition When Sample Clock Frequencies Cross
- Accommodate Dynamically Changing Asynchronous Sample Clocks
- 8 kHz to 56 kHz Sample Clock Frequency Range
- 1:2 to 2:1 Ratio Between Sample Clocks
- −106 dB THD+N at 1 kHz (AD1890)
- 120 dB Dynamic Range (AD1890)
- Optimal Clock Tracking Control
  - −Short/Long Group Delay Modes
  - −Slow/Fast Settling Modes
- Linear Phase in All Modes
- Equivalent of 4 Million 22-Bit FIR Filter Coefficients Stored On-Chip
- Automatic Output Mute
- Flexible Four Wire Serial Interfaces
- Low Power

APPLICATIONS

- Digital Mixing Consoles and Digital Audio Workstations
- CD-R, DAT, DCC and MD Recorders
- Multitrack Digital Audio and Video Tape Recorders
- Studio to Transmitter Links
- Digital Audio Signal Routers/Switches
- Digital Audio Broadcast Equipment
- High Quality D/A Converters
- Digital Tape Recorder Varispeed Applications
- Computer Communication and Multimedia Systems

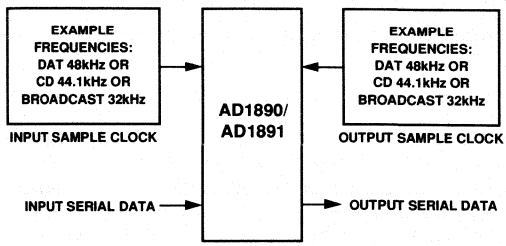
PRODUCT OVERVIEW

The AD1890 and AD1891 SamplePorts™ are fully digital, stereo Asynchronous Sample Rate Converters (ASRCs) that solve sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, these converters interpolate the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimate down to the desired output sample rate. The AD1890 is intended for 18- and 20-bit professional applications, and the AD1891 is intended for 16-bit lower cost applications where large dynamic sample-rate changes are not encountered. These devices are asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1890/AD1891 ASRCs) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1890/AD1891 automatically sense the relationship between the two clocks. The

SamplePort and SamplePorts are trademarks of Analog Devices, Inc.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

SYSTEM DIAGRAM



input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from 1:2 to 2:1.

The AD1890/AD1891 use multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 20 bits for the AD1890 or 4 to 16 bits for the AD1891. Shorter input words are automatically zero-filled in the LSBs. The output word width for both devices is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I^2S compatible devices. Input and output data can be independently justified to the left/right clock edge, or delayed by one bit clock from the left/right clock edge. Input and output data can also be independently justified to the word clock rising edge or delayed by one bit clock from the word clock rising edge. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1890/AD1891 SamplePort™ ASRCs have on-chip digital coefficients that correspond to a highly oversampled 0 kHz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered instantaneous ratio between the input sample clock ($L\overline{R}\_I$) and the output sample clock ($L\overline{R}\_O$), and these coefficients are used in an FIR convolver to perform the sample rate conversion. Refer to the "Theory of Operation" section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is

AD1890/AD1891—SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltage	+5.0	V
Ambient Temperature	25	°C
MCLK	20	MHz
Load Capacitance	100	pF

All minimums and maximums tested except as noted.

PERFORMANCE (Guaranteed over 0°C ≤ T_A ≤ 70°C, V_{DD} = 5.0 V ± 10%, 8 MHz ≤ MCLK ≤ 20 MHz)

	Min	Max	Units
AD1890 Dynamic Range (20 Hz to 20 kHz, −60 dB Input)†	120		dB
AD1891 Dynamic Range (20 Hz to 20 kHz, −60 dB Input)†	96		dB
Total Harmonic Distortion + Noise†			dB
AD1890 and AD1891 (20 Hz to 20 kHz, Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.5 and 2.0)		−94	dB
AD1890 (1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−106	dB
AD1890 (10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−100	dB
AD1891 (1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−96	dB
AD1891 (10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−95	dB
Interchannel Phase Deviation†		0	Degrees
Input and Output Sample Clock Jitter† (For ≤ 1 dB Degradation in THD+N with 10 kHz Full-Scale Input, Slow-Settling Mode)	10		ns

DIGITAL INPUTS (Guaranteed over 0°C ≤ T_A ≤ 70°C, V_{DD} = 5.0 V ± 10%, 8 MHz ≤ MCLK ≤ 20 MHz)

	Min	Max	Units
V_{IH}	2.2		V
V_{IL}		0.8	V
I_{IH} @ V_{IH} = +5 V		4	μA
I_{IL} @ V_{IL} = 0 V		4	μA
V_{OH} @ I_{OH} = −4 mA	3.6		V
V_{OL} @ I_{OL} = 4 mA		0.4	V
Input Capacitance†		15	pF

DIGITAL TIMING (Guaranteed over 0°C ≤ T_A ≤ 70°C, V_{DD} = 5.0 V ± 10%, 8 MHz ≤ MCLK ≤ 20 MHz)

		Min	Max	Units
t_{MCLK}	MCLK Period	50	125	ns
f_{MCLK}	MCLK Frequency ($1/t_{MCLK}$)	8	20	MHz
t_{MPWL}	MCLK LO Pulse Width	20		ns
t_{MPWH}	MCLK HI Pulse Width	20		ns
f_{LRI}	$\overline{LR}$_I Frequency with 20 MHz MCLK†	10	70	kHz
t_{RPWL}	$\overline{RESET}$ LO Pulse Width	100		ns
t_{RS}	$\overline{RESET}$ Setup to MCLK Falling	15		ns
t_{BCLK}	BCLK_I/O Period†	80		ns
f_{BCLK}	BCLK_I/O Frequency ($1/t_{BCLK}$)†		12.5	MHz
t_{BPWL}	BCLK_I/O LO Pulse Width	40		ns
t_{BPWH}	BCLK_I/O HI Pulse Width	40		ns
t_{WSI}	WCLK_I Setup to BCLK_I	15		ns
t_{WSO}	WCLK_O Setup to BCLK_O	30		ns
t_{LRSI}	$\overline{LR}$_I Setup to BCLK_I	15		ns
t_{LRSO}	$\overline{LR}$_O Setup to BCLK_O	30		ns
t_{DS}	Data Setup to BCLK_I	0		ns
t_{DH}	Data Hold from BCLK_I	25		ns
t_{DPD}	Data Propagation Delay from BCLK_O		40	ns
t_{DOH}	Data Output Hold from BCLK_O	5		ns

POWER (0°C ≤ T_A ≤ 70°C, MCLK = 16 MHz, F_{SIN} = 48 kHz, F_{SOUT} = 44.1 kHz)

	Min	Typ	Max	Units
Supplies				
Voltage, V_{DD}	2.7		5.5	V
Current, I_{DD} (V_{DD} = 5.0 V)		35	40	mA
Current, I_{DD} (V_{DD}= 3.0 V)		19		mA
Dissipation				
Operation (V_{DD} = 5.0 V)		175	200	mW
Operation (V_{DD} = 3.0 V)		57		mW

TEMPERATURE RANGE

	Min	Max	Units
Specifications Guaranteed	0	+70	°C
Operation Guaranteed	−40	+85	°C
Storage	−60	+100	°C

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
V_{DD} to GND	−0.3	7.0	V
DC Input Voltage	−0.3	V_{DD} + 0.3	V
Latch-Up Trigger Current	−1000	+1000	mA
Soldering		+300	°C
		10	sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DIGITAL FILTER CHARACTERISTICS†

	Min	Max	Units
Passband Ripple (0 to 20 kHz)		0.01	dB
Transition Band[1]		4.1	kHz
Stopband Attenuation	110		dB
Group Delay ($\overline{LR}$_I = 50 kHz)	700	3000	μs

†Guaranteed, Not Tested

[1]Valid only when $F_{SOUT} \geq F_{SIN}$ (i.e., upsampling), F_{SIN} = 44.1 kHz.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1890JN	0°C to +70°C	Plastic DIP	N-28
AD1890JP	0°C to +70°C	PLCC	P-28A
AD1891JN	0°C to +70°C	Plastic DIP	N-28
AD1891JP	0°C to +70°C	PLCC	P-28A

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1890/AD1891 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

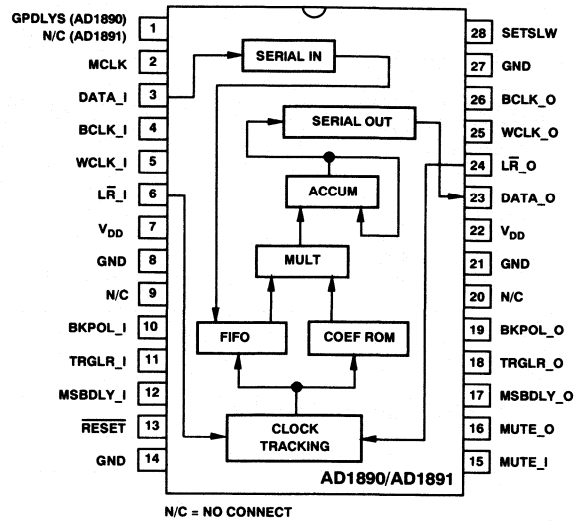
PRODUCT OVERVIEW (Continued)

automatically limited to avoid alias distortion on the output signal. The AD1890/AD1891 dynamically alter the low-pass filter cutoff frequency smoothly and slowly, so that real-time variations in the sample rate ratio are possible without degradation of the audio quality.

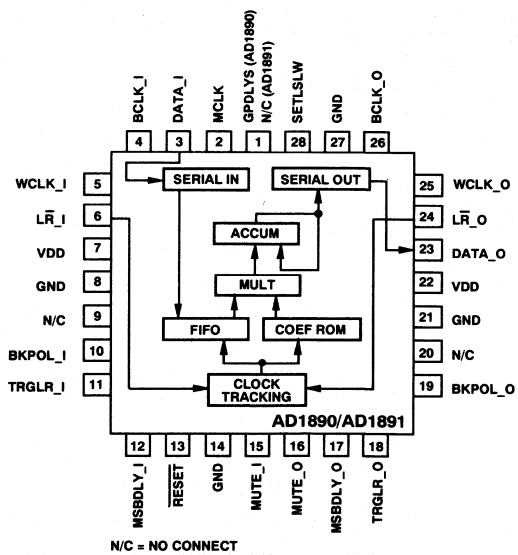
The AD1890/AD1891 have a pin selectable slow- or fast-settling mode. This mode determines how quickly the ASRCs adapt to a change in either the input sample clock frequency (F_{SIN}) or the output sample clock frequency (F_{SOUT}). In the slow-settling mode, the control loop which computes the ratio between F_{SIN} and F_{SOUT} settles in approximately 800 ms and begins to reject jitter above 3 Hz. The slow-settling mode offers the best signal quality and the greatest jitter rejection. In the fast-settling mode, the control loop settles in approximately 200 ms and begins to reject jitter above 12 Hz. The fast-settling mode allows rapid, real time sample rate changes to be tracked without error, at the expense of some narrow-band noise modulation products on the output signal.

The AD1890 also has a pin selectable, short or long group delay mode. This pin determines the depth of the First-In, First-Out (FIFO) memory which buffers the input data samples before they are processed by the FIR convolver. In the short mode, the group delay is approximately 700 μs. The ASRC is more sensitive to sample rate changes in this mode (i.e., the pointers which manage the FIFO are more likely to cross and become momentarily invalid during a sample rate step change), but the group delay is minimized. In the long mode, the group delay is approximately 3 ms. The ASRC is tolerant of large dynamic sample rate changes in this mode, and it should be used when the device is required to track fast sample rate changes, such as in varispeed applications. The AD1891 features the short group delay mode only. In either device, if the read and write pointers that manage the FIFO cross (indicating underflow or overflow), the ASRC asserts the mute output (MUTE_O) pin HI for 128 output clock cycles. If MUTE_O is connected to the mute input (MUTE_I) pin, as it normally should be, the serial output will be muted (i.e., all bits zero) during this transient event.

The AD1890/AD1891 are fabricated in a 0.8 μm single poly, double metal CMOS process and are packaged in a 0.6″ wide 28-pin plastic DIP and a 28-pin PLCC. The AD1890/AD1891 operate from a +5 V power supply over the temperature range of 0°C to +70°C.



AD1890/AD1891 DIP Pinout



AD1890/AD1891 PLCC Pinout

DEFINITIONS

Dynamic Range
The ratio of a near full-scale input signal to the integrated noise in the passband (0 to ≈20 kHz), expressed in decibels (dB). Dynamic range is measured with a −60 dB input signal and "60 dB" arithmetically added to the result.

Total Harmonic Distortion + Noise
Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the rms value of a sinusoidal input signal. It is usually expressed in percent (%) or decibels.

Interchannel Phase Deviation
Difference in input sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.

Group Delay
Intuitively, the time interval required for a full-level input pulse to appear at the converter's output, at full level, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Transport Delay
The time interval between when an impulse is applied to the converters input and when the output starts to be affected by this impulse, expressed in milliseconds (ms). Transport delay is independent of frequency.

AD1890/AD1891 PIN LIST

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Serial Input Interface

Pin Name	Number	I/O	Description
DATA_I	3	I	Serial input, MSB first, containing two channels of 4- to 20-bits of twos-complement data per channel. AD1891 ONLY: Maximum of 16 data bits per channel; additional bits ignored.
BCLK_I	4	I	Bit clock input for input data.
WCLK_I	5	I	Word clock input for input data. This input is rising edge sensitive. (Not required in $\overline{LR}$ input data clock triggered mode [TRGLR_I = HI].)
$\overline{LR}$_I	6	I	Left/$\overline{right}$ clock input for input data. Must run continuously.

Serial Output Interface

Pin Name	Number	I/O	Description
DATA_O	23	O	Serial output, MSB first, containing two channels of 4- to 24-bits of twos-complement data per channel.
BCLK_O	26	I	Bit clock input for output data.
WCLK_O	25	I	Word clock input for output data. This input is rising edge sensitive. (Not required in $\overline{LR}$ output data clock triggered mode [TRGLR_O = HI].)
$\overline{LR}$_O	24	I	Left/$\overline{right}$ clock input for output data. Must run continuously.

Input Control Signals

Pin Name	Number	I/O	Description
BKPOL_I	10	I	Bit clock polarity. LO: Normal mode. Input data is sampled on rising edges of BCLK_I. HI: Inverted mode. Input data is sampled on falling edges of BCLK_I.
TRGLR_I	11	I	Trigger on $\overline{LR}$_I. HI: Changes in $\overline{LR}$_I indicate beginning[1] of valid input data. LO: Rising edge of WCLK_I indicates beginning of valid input data.
MSBDLY_I	12	I	MSB delay. HI: Input data is delayed one BCLK_I after either $\overline{LR}$_I (TRGLR_I = HI) or WCLK_I (TRGLR_I = LO) indicates the beginning of valid input data. Included for I^2S data format compatibility. LO: No delay.

NOTE
[1]The beginning of valid data will be delayed by one BLCK_I if MSBDEL_I is selected (HI).

Output Control Signals

Pin Name	Number	I/O	Description
BKPOL_O	19	I	Bit clock polarity. LO: Normal mode. Output data is valid on rising edges of BCLK_O, changed on falling. HI: Inverted mode. Output data is valid on falling edges of BCLK_O, changed on rising.
TRGLR_O	18	I	Trigger on $\overline{LR}$_O. HI: Changes in $\overline{LR}$_O indicate beginning[1] of valid output data. LO: Rising edge of WCLK_O indicates beginning of valid output data.
MSBDLY_O	17	I	MSB delay. HI: Output data is delayed one BCLK_O after either $\overline{LR}$_O (TRGLR_O = HI) or WCLK_O (TRGLR_O = LO) indicates the beginning of valid output data. Included for I^2S data format compatibility. LO: No delay.

Miscellaneous

Pin Name	Number	I/O	Description
GPDLYS	1	I	AD1890 ONLY: Group delay—short. HI: Short group delay mode (≈700 μs). More sensitive to changes in sample rates ($\overline{LR}$ clocks). LO: Long group delay mode (≈3 ms). More tolerant of sample rate changes. This signal may be asynchronous with respect to MCLK, and dynamically changed, but is normally pulled up or pulled down on a static basis. AD1891: Short group delay mode only; this pin is a N/C.
MCLK	2	I	Master clock input. Nominally 16 MHz for sampling frequencies (F_S, word rates) from 8 kHz to 56 kHz. Exact frequency is not critical, and does not need to be synchronized to any other clock or possess low jitter.
$\overline{RESET}$	13	I	Active LO reset. Set HI for normal chip operation.
MUTE_O	16	O	Mute output. HI indicates that data is not currently valid due to read and write FIFO memory pointer overlap. LO indicates normal operation.
MUTE_I	15	I	Mute input. HI mutes the serial output to zeros (midscale). Normally connected to MUTE_O. Reset LO for normal operation.
SETLSLW	28	I	Settle slowly to changes in sample rates. HI: Slow-settling mode (≈800 ms). Less sensitive to sample clock jitter. LO: Fast-settling mode (≈200 ms). Some narrow-band noise modulation may result from jitter on $\overline{LR}$ clocks. This signal may be asynchronous with respect to MCLK, and dynamically changed, but is normally pulled up or pulled down on a static basis.
N/C	9, 20		No connect. Reserved. Do not connect.

Power Supply Connections

Pin Name	Number	I/O	Description
V_{DD}	7, 22	I	Positive digital voltage supply.
GND	8, 14, 21, 27	I	Digital ground. Pins 14 and 27 need not be decoupled.

NOTE
[1]The beginning of valid data will be delayed by one BCLK_O if MSBDEL_0 is selected (HI).

Performance Graphs

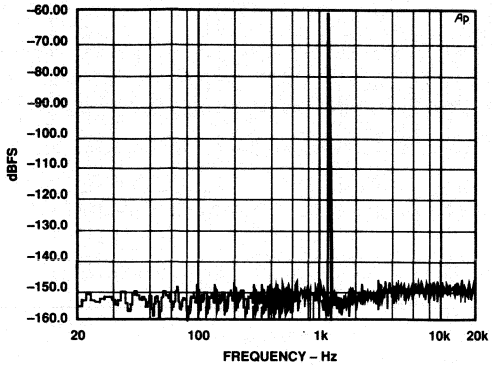

Figure 14a. AD1890—Dynamic Range from 20 Hz to 20 kHz, −60 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

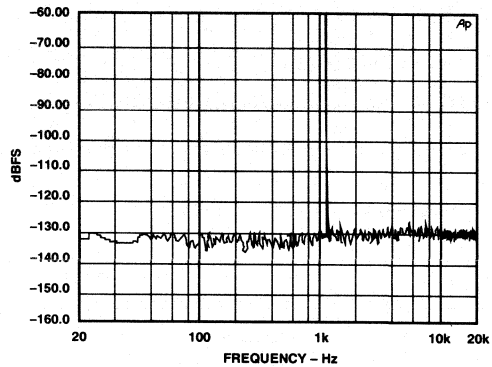

Figure 14b. AD1891—Dynamic Range from 20 Hz to 20 kHz, −60 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

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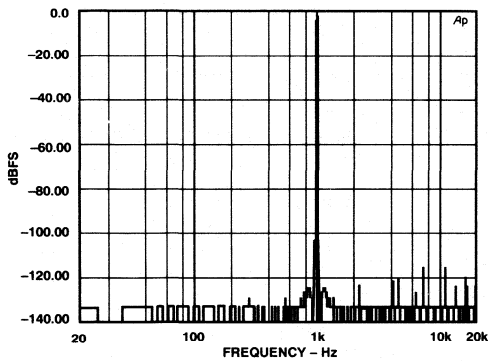

Figure 15a. AD1890—1 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

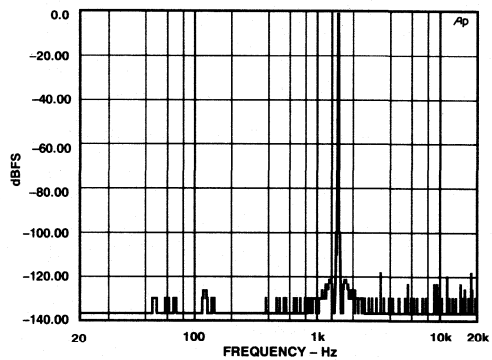

Figure 15b. AD1891—1 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

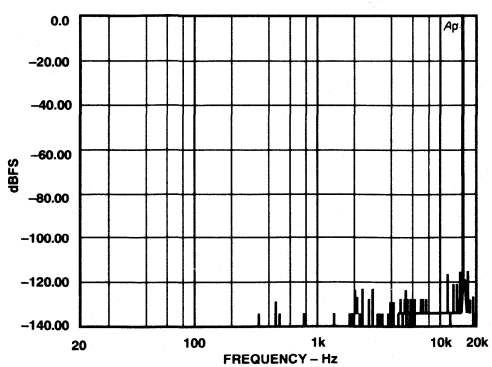

Figure 16a. AD1890—15 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

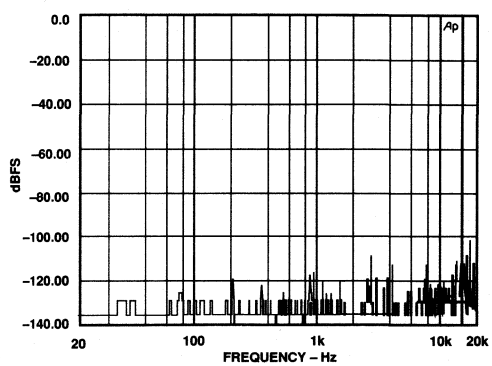

Figure 16b. AD1891—15 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

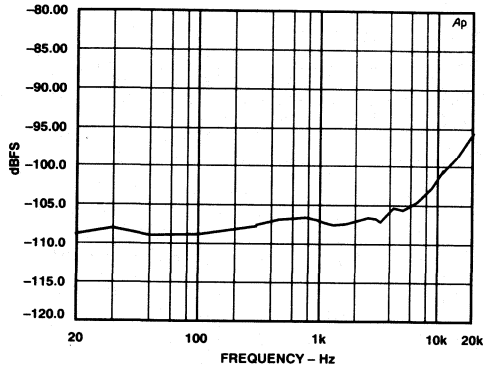

Figure 17a. AD1890—THD+N vs. Frequency, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, Full-Scale Input Signal

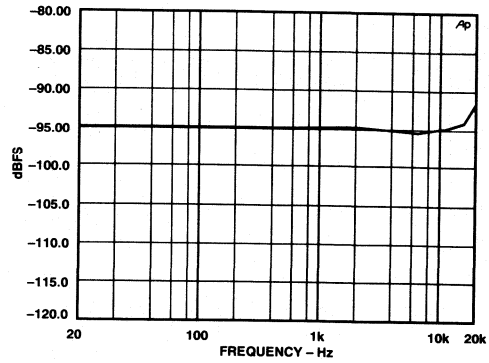

Figure 17b. AD1891—THD+N vs. Frequency, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, Full-Scale Input Signal

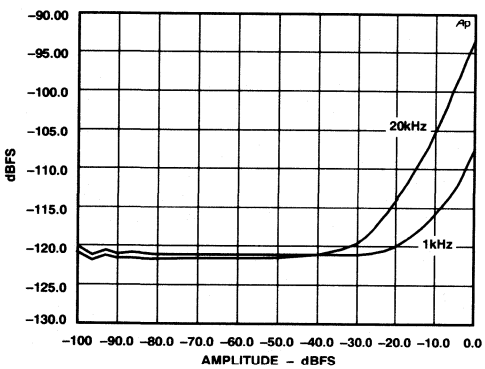

Figure 18a. AD1890—THD+N vs. Input Amplitude, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 1 kHz and 20 kHz Tones

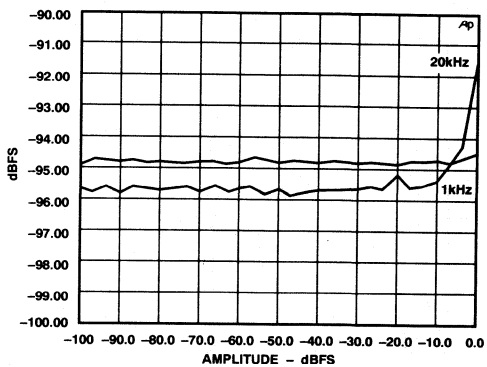

Figure 18b. AD1891—THD+N vs. Input Amplitude, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 1 kHz and 20 kHz Tones

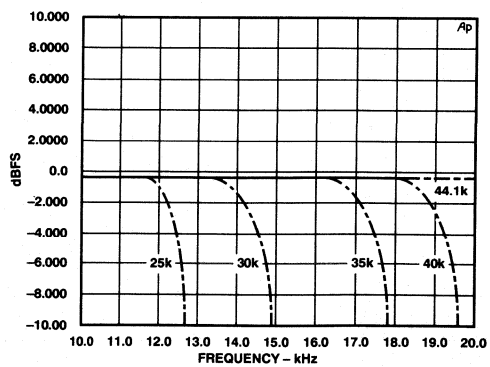

Figure 19. AD1890/AD1891 Digital Filter Signal Transfer Function, 10 kHz to 20 kHz, 44.1 kHz Input Sample Frequency, 44.1, 40, 35, 30 and 25 kHz Output Sample Frequencies

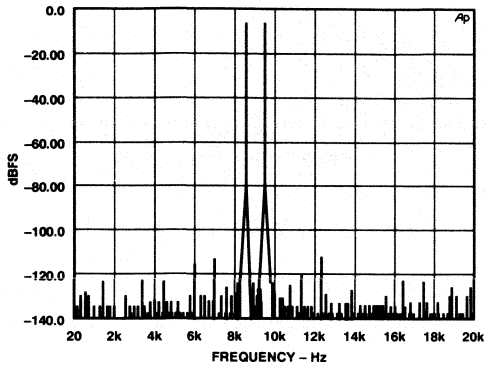

Figure 20a. AD1890—Twintone, 10 kHz and 11 kHz, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

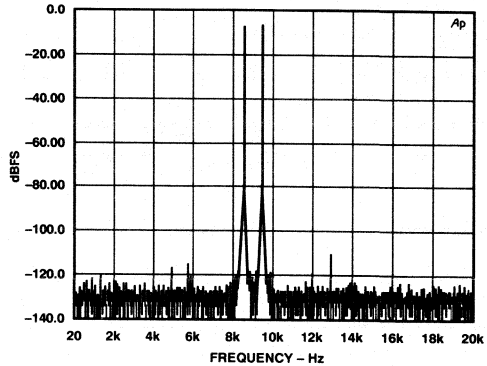

Figure 20b. AD1891—Twintone, 10 kHz and 11 kHz, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

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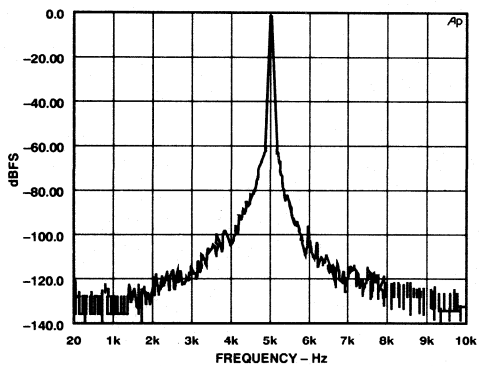


Figure 21. AD1890/AD1891—5 kHz Tone at 0 dBFS with 100 ns p-p Binomial Jitter on L/$\overline{R}$ Clocks, Fast Settling Mode, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

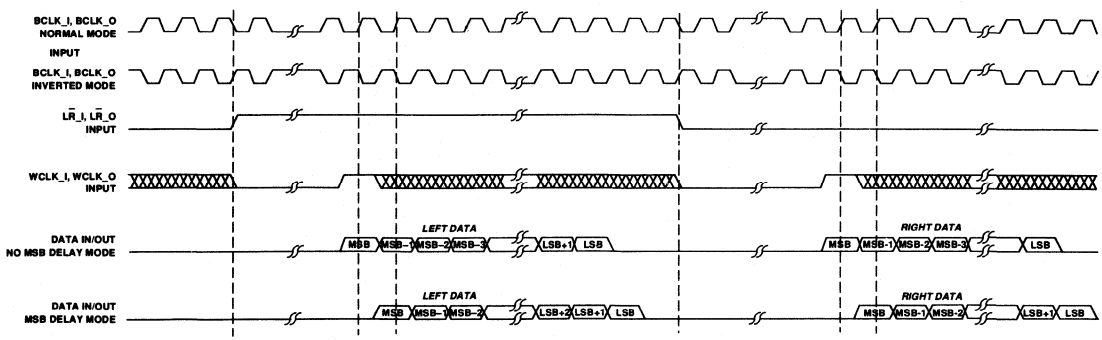


Figure 22. AD1890/AD1891 Serial Data Input and Output Timing, Word Clock Triggered Mode

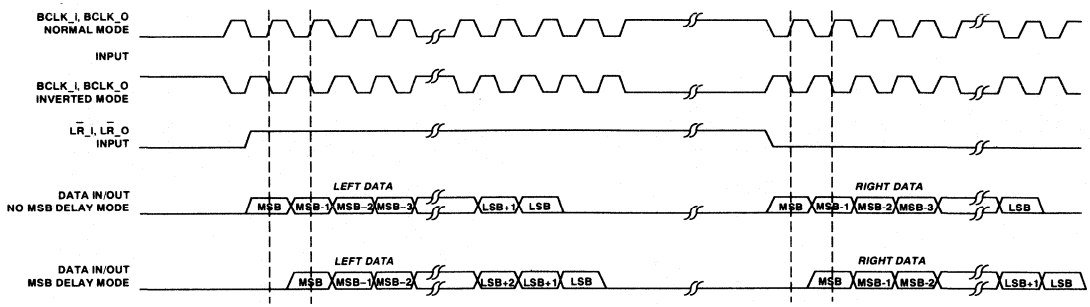


Figure 23. AD1890/AD1891 Serial Data Input and Output Timing, Left/Right Clock Triggered Mode

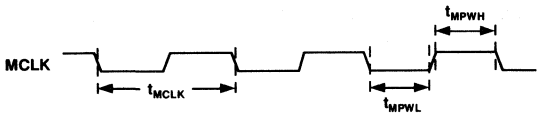


Figure 24. AD1890/AD1891 MCLK Timing

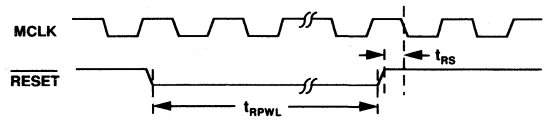


Figure 25. AD1890/AD1891 Reset Timing

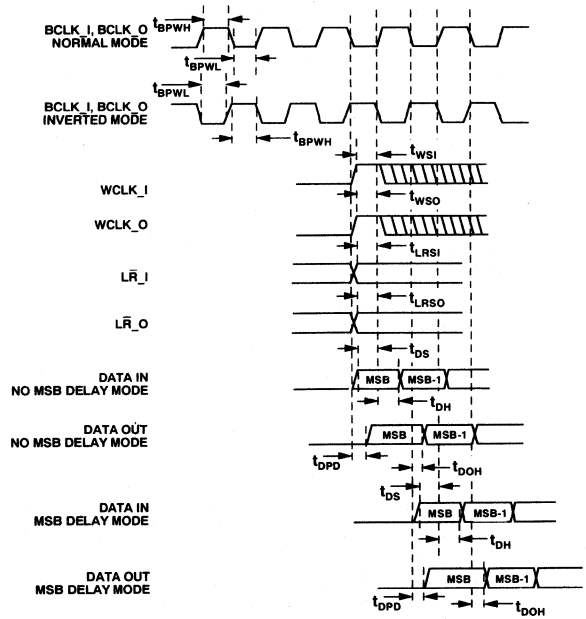


Figure 26. AD1890/AD1891 Bit Clock, Word Clock, Left/Right Clock and Data Timing

Low Cost SamplePort 16-Bit Stereo Asynchronous Sample Rate Converter

AD1893

FEATURES

- Low Cost
- TQFP and PDIP Packages
- 3 V Supply Performance Specified—Very Low Power
- Automatically Senses Sample Frequencies—No Programming Required
- Rejects Sample Clock Jitter
- Accommodates Dynamically Changing Asynchronous Sample Clocks
- 8 kHz to 56 kHz Sample Clock Frequency Range
- Approximately 1:2 to 2:1 Ratio Between Sample Clocks
- −96 dB THD+N at 1 kHz
- 96 dB Dynamic Range
- Optimal Clock Tracking Control —Slow/Fast Settling Modes
- Linear Phase in All Modes
- Automatic Output Mute
- Flexible Four Wire Serial Interfaces with Right-Justified Mode
- Power-Down Mode
- On-Chip Oscillator

APPLICATIONS

- Consumer CD-R, DAT, DCC, MD and 8 mm Video Tape Recorders Including Portables
- Digital Audio Communication/Network Systems
- Computer Multimedia Systems

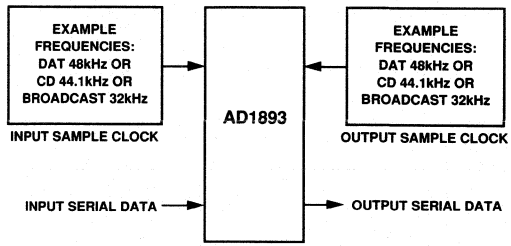
PRODUCT OVERVIEW

The AD1893 SamplePort® is a fully digital, stereo Asynchronous Sample Rate Converter (ASRC) that solves sample rate interfacing and compatibility problems in digital audio equipment. Conceptually, this converter interpolates the input data up to a very high internal sample rate with a time resolution of 300 ps, then decimates down to the desired output sample rate. The AD1893 is intended for 16-bit low cost, non-varispeed applications where low voltage, low power (i.e., battery-powered) operation is required. Refer to the AD1890/AD1891 data sheet for other products in the SamplePort family. This device is asynchronous because the frequency and phase relationships between the input and output sample clocks (both are inputs to the AD1893 ASRC) are arbitrary and need not be related by a simple integer ratio. There is no need to explicitly select or program the input and output sample clock frequencies, as the AD1893 automatically senses the relationship between the two clocks. The input and output sample clock frequencies can nominally range from 8 kHz to 56 kHz, and the ratio between them can vary from approximately 1:2 to 2:1.

SamplePort is a registered trademark of Analog Devices, Inc.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

SYSTEM DIAGRAM



4

The AD1893 uses multirate digital signal processing techniques to construct an output sample stream from the input sample stream. The input word width is 4 to 16 bits for the AD1893. Shorter input words are automatically zero-filled in the LSBs. The output word width is 24 bits. The user can receive as many of the output bits as desired. Internal arithmetic is performed with 22-bit coefficients and 27-bit accumulation. The digital samples are processed with unity gain.

The input and output control signals allow for considerable flexibility for interfacing to a variety of DSP chips, AES/EBU receivers and transmitters and for I^2S compatible devices. Input and output data can be independently right- or left- (with or without a one bit clock delay) justified to the left/right clock edge. In the right-justified mode, the MSB is delayed 16 bit clock periods from the left/right clock edge transition. Input and output data can also be independently justified to the word clock rising edge. The data justification options are encoded on two mode pins for both the input port and the output port. The bit clocks can also be independently configured for rising edge active or falling edge active operation.

The AD1893 SamplePort ASRC has on-chip digital coefficients that correspond to a highly oversampled 0 Hz to 20 kHz low-pass filter with a flat passband, a very narrow transition band, and a high degree of stopband attenuation. A subset of these filter coefficients are dynamically chosen on the basis of the filtered ratio between the input sample clock ($\overline{LR}$_I) and the output sample clock ($\overline{LR}$_O), and these coefficients are then used in an FIR convolver to perform the sample rate conversion. Refer to the "Theory of Operation" section of this data sheet for a more thorough functional description. The low-pass filter has been designed so that full 20 kHz bandwidth is maintained when the input and output sample clock frequencies are as low as 44.1 kHz. If the output sample rate drops below the input sample rate, the bandwidth of the input signal is automatically

AD1893—SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltage	+3.0	V
Ambient Temperature	25	°C
Crystal Frequency	16	MHz
Load Capacitance	100	pF

All minimums and maximums tested except as noted.

PERFORMANCE† (Guaranteed for V_{DD} = +3.3 V to +5.0 V ± 10%)

	Min	Max	Units
Dynamic Range (20 Hz to 20 kHz, −60 dB Input)	96		dB
Total Harmonic Distortion + Noise			dB
(20 Hz to 20 kHz, Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.51 and 1.99)		−94	dB
(1 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−96	dB
(10 kHz Full-Scale Input, F_{SOUT}/F_{SIN} Between 0.7 and 1.4)		−95	dB
Interchannel Phase Deviation		0	Degrees
Input and Output Sample Clock Jitter (For ≤ 1 dB Degradation in THD+N with 10 kHz Full-Scale Input, Slow-Settling Mode)	10		ns

DIGITAL INPUTS (Guaranteed for V_{DD} = +3.0 V to +5.0 V ± 10%)

	Min	Max	Units
V_{IH}	2.0		V
V_{IL} ($V_{DD} \geq$ +3.0 V)		0.8	V
V_{IL} (+2.7 V ≤ V_{DD} < +3.0 V)		0.7	V
I_{IH} @ V_{IH} = +5.0 V, All Pins Except XTAL_I		4	µA
I_{IH} @ V_{IH} = +5.0 V, XTAL_I Pin		6	µA
I_{IL} @ V_{IL} = 0 V, All Pins Except XTAL_I		4	µA
I_{IL} @ V_{IL} = 0 V, XTAL_I Pin		6	µA
V_{OH} @ I_{OH} = −4 mA ($V_{DD} \geq$ +3.0 V)	2.4		V
V_{OH} @ I_{OH} = −4 mA (+2.7 V ≤ V_{DD} < +3.0 V)	2.2		V
V_{OL} @ I_{OL} = 4 mA		0.4	V
Input Capacitance†		15	pF

DIGITAL TIMING (Guaranteed for V_{DD} = +3.0 V to +5.0 V + 10%) See Figures 26 through 28.

		Min	Max	Units
$t_{crystal}$	Crystal Period	62.5	125	ns
$F_{crystal}$	Crystal Frequency ($1/t_{crystal}$)		16	MHz
t_{PWL}	Crystal LO Pulse Width	20		ns
t_{PWH}	Crystal HI Pulse Width	20		ns
F_{LRI}	$\overline{LR}$_I Frequency with 16 MHz Crystal†	10	56	kHz
t_{RPWL}	$\overline{RESET}$ LO Pulse Width	125		ns
t_{RS}	$\overline{RESET}$ Setup to Crystal Falling	15		ns
t_{BCLK}	BCLK_I/O Period†	120		ns
F_{BCLK}	BCLK_I/O Frequency ($1/t_{BCLK}$)†		8.33	MHz
t_{BPWL}	BCLK_I/O LO Pulse Width	55		ns
t_{BPWH}	BCLK_I/O HI Pulse Width	55		ns
t_{WSI}	WCLK_I Setup to BCLK_I	15		ns
t_{WSO}	WCLK_O Setup to BCLK_O	40		ns
t_{LRSI}	$\overline{LR}$_I Setup to BCLK_I	15		ns
t_{LRSO}	$\overline{LR}$_O Setup to BCLK_O	55		ns
t_{DS}	Data Setup to BCLK_I	0		ns
t_{DH}	Data Hold from BCLK_I	35		ns
t_{DPD}	Data Propagation Delay from BCLK_O		90	ns
t_{DOH}	Data Output Hold from BCLK_O	15		ns

DIGITAL FILTER CHARACTERISTICS†

	Min	Max	Units
Passband Ripple (0 to 20 kHz)		0.01	dB
Transition Band[1]		4.1	kHz
Stopband Attenuation	110		dB
Group Delay ($L\overline{R}\_I$ = 50 kHz)	700	3000	µs

POWER (F_{SIN} = 48 kHz, F_{SOUT} = 44.1 kHz)

	Min	Typ	Max	Units
Supplies				
Voltage, V_{DD}	2.7		5.5	V
Operational Current, I_{DD} (V_{DD} = +5.0 V)		30	40	mA
Operational Current, I_{DD} (V_{DD} = +3.0 V)†		15	20	mA
Power-Down Current, I_{DD} (V_{DD} = +5.0 V)		1.5	2.5	mA
Power-Down Current, I_{DD} (V_{DD} = +3.0 V)†		0.5	1.0	mA
Dissipation†				
Operation (V_{DD} = +5.0 V)		150	200	mW
Operation (V_{DD} = +3.0 V)		45	60	mW
Power-Down (V_{DD} = +5.0 V)		7.5	12.5	mW
Power-Down (V_{DD} = +3.0 V)		1.5	3.0	mW

4

TEMPERATURE RANGE

	Min	Max	Units
Operation Guaranteed	−40	+85	°C
Storage	−60	+100	°C

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
V_{DD} to GND	−0.3	7.0	V
DC Input Voltage	−0.3	V_{DD} + 0.3	V
Latch-Up Trigger Current	−1000	+1000	mA
Soldering		+300	°C
		10	sec

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

†Guaranteed, Not Tested

[1]Valid only when $F_{SOUT} \geq F_{SIN}$ (i.e., upsampling), F_{SIN} = 44.1 kHz.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD1893JN	0°C to +70°C	Plastic DIP	N-28
AD1893JST	0°C to +70°C	TQFP	ST-44

*For outline information see Package Information section.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1893 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PRODUCT OVERVIEW (Continued)

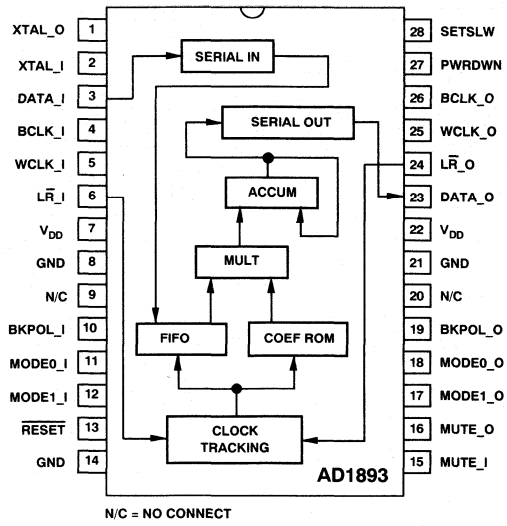
limited to avoid alias distortion on the output signal. The AD1893 dynamically alters the low-pass filter cutoff frequency smoothly and slowly, so that real-time variations in the sample rate ratio are possible without degradation of the audio quality.

The AD1893 has a pin selectable slow- or fast-settling mode. This mode determines how quickly the ASRC adapts to a change in either the input sample clock frequency (F_{SIN}) or the output sample clock frequency (F_{SOUT}). In the slow-settling mode, the control loop which computes the ratio between F_{SIN} and F_{SOUT} settles in approximately 800 ms and begins to reject jitter above 3 Hz. The slow-settling mode offers the best signal quality and the greatest jitter rejection. In the fast-settling mode, the control loop settles in approximately 200 ms and begins to reject jitter above 12 Hz. The fast-settling mode allows rapid, real time sample rate changes to be tracked without error, at the expense of some narrow-band noise modulation products on the output signal.

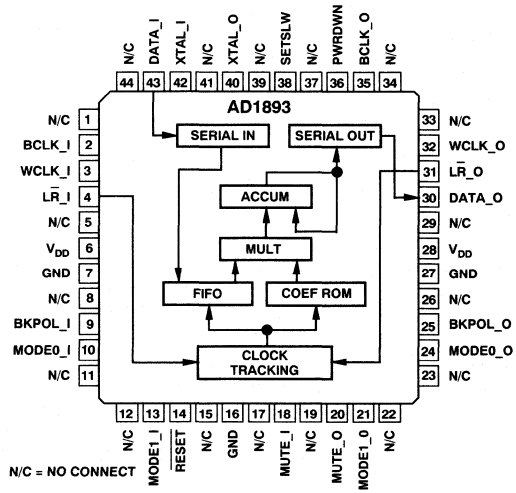
The AD1893 features short group delay processing. This feature relates to the depth of the First-In, First-Out (FIFO) memory which buffers the input data samples before they are processed by the FIR convolver. In the AD1893, the group delay is approximately 700 μs. If the read and write pointers that manage the FIFO cross (indicating underflow or overflow), the AD1893 asserts the mute output (MUTE_O) pin HI for 128 output clock cycles. If MUTE_O is connected to the mute input (MUTE_I) pin, as it normally should be, the serial output will be muted (i.e., all bits zero) during this transient event.

The AD1893 includes an on-chip oscillator which only requires that the user provide an external crystal. By removing the need for an external oscillator, the AD1893 lowers the total cost of ownership to the end user. The AD1893 also includes a power-down mode, which is invoked with the PWRDWN pin. Asserting this control signal HI will place the AD1893 into a very low power dissipation inactive and standby condition.

The AD1893 is fabricated in a 0.8 μm single poly, double metal CMOS process and are packaged in a 0.6″ wide 28-pin plastic DIP and a 10 mm by 10 mm body size 44-pin TQFP. The AD1893 operates from a +3 V to +5 V power supply over the temperature range of 0°C to +70°C.



AD1893 DIP Pinout



AD1893 TQFP Pinout

DEFINITIONS

Dynamic Range
The ratio of a near full-scale input signal to the integrated noise in the passband (0 to ≈20 kHz), expressed in decibels (dB). Dynamic range is measured with a −60 dB input signal and "60 dB" arithmetically added to the result.

Total Harmonic Distortion + Noise
Total Harmonic Distortion plus Noise (THD+N) is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the rms value of a sinusoidal input signal. It is usually expressed in percent (%) or decibels.

Interchannel Phase Deviation
Difference in input sampling times between stereo channels, expressed as a phase difference in degrees between 1 kHz inputs.

Group Delay
Intuitively, the time interval required for a full-level input pulse to appear at the converter's output, at full level, expressed in milliseconds (ms). More precisely, the derivative of radian phase with respect to radian frequency at a given frequency.

Transport Delay
The time interval between when an impulse is applied to the converter's input and when the output starts to be affected by this impulse, expressed in milliseconds (ms). Transport delay is independent of frequency.

AD1893 PIN LIST

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Serial Input Interface

Pin Name	DIP	TQFP	I/O	Description
DATA_I	3	43	I	Serial input, MSB first, containing two channels of 4 to 16 bits of twos-complement data per channel.
BCLK_I	4	2	I	Bit clock input for input data. Need not run continuously; may be gated or used in a burst fashion.
WCLK_I	5	3	I	Word clock input for input data. This input is rising edge sensitive. (Not required in $\overline{LR}$ input data clock triggered modes.)
$\overline{LR}$_I	6	4	I	Left/$\overline{right}$ clock input for input data. Must run continuously.

Serial Output Interface

Pin Name	DIP	TQFP	I/O	Description
DATA_O	23	30	O	Serial output, MSB first, containing two channels of 4- to 24-bits of twos-complement data per channel.
BCLK_O	26	35	I	Bit clock input for output data. Need not run continuously; may be gated or used in a burst fashion.
WCLK_O	25	32	I	Word clock input for output data. This input is rising edge sensitive. (Not required in $\overline{LR}$ output data clock triggered modes.)
$\overline{LR}$_O	24	31	I	Left/$\overline{right}$ clock input for output data. Must run continuously.

Input Control Signals

Pin Name	DIP	TQFP	I/O	Description
BKPOL_I	10	9	I	Bit clock polarity. LO: Normal mode. Input data is sampled on rising edges of BCLK_I. HI: Inverted mode. Input data is sampled on falling edges of BCLK_I.
MODE0_I	11	10	I	Serial mode zero control for input port.
MODE1_I	12	13	I	Serial mode one control for input port.

MODE0_I	MODE1_I	
0	0	Left-justified, no MSB delay, $\overline{LR}$_I clock triggered.
0	1	Left-justified, MSB delay, $\overline{LR}$_I clock triggered.
1	0	Right-justified, MSB delayed 16 bit clock periods from $\overline{LR}$_I transition.
1	1	WCLK_I triggered, no MSB delay.

Output Control Signals

Pin Name	DIP	I/O	TQFP	Description
BKPOL_O	19	I	25	Bit clock polarity. LO: Normal mode. Output data is valid on rising edges of BCLK_O, changed on falling. HI: Inverted mode. Output data is valid on falling edges of BCLK_O, changed on rising.
MODE0_O	18	I	24	Serial mode zero control for output port.
MODE1_O	17	I	21	Serial mode one control for output port.

MODE0_O	MODE1_O	
0	0	Left-justified, no MSB delay, $\overline{LR}$_O clock triggered.
0	1	Left-justified, MSB delay, $\overline{LR}$_O clock triggered.
1	0	Right-justified, MSB delayed 16 bit clock periods from $\overline{LR}$_O transition.
1	1	WCLK_O triggered, no MSB delay.

Miscellaneous

Pin Name	DIP	TQFP	I/O	Description
XTAL_O	1	40	O	Crystal output. Connect to one side of nominal 16 MHz crystal for sampling frequencies (F_S word rates) from 8 kHz to 56 kHz.
XTAL_I	2	42	I	Crystal input. Connect to other side of nominal 16 MHz crystal for sampling frequencies (F_S word rates) from 8 kHz to 56 kHz. Use this input to overdrive the on-chip oscillator with an external clock source.
$\overline{RESET}$	13	14	I	Active LO reset. Set HI for normal chip operation.
MUTE_O	16	20	O	Mute output. HI indicates that data is not currently valid due to read and write FIFO memory pointer overlap. LO indicates normal operation.
MUTE_I	15	18	I	Mute input. HI mutes the serial output to zeros (midscale). Normally connected to MUTE_O. Reset LO for normal operation.
SETLSLW	28	38	I	Settle slowly to changes in sample rates. HI: Slow-settling mode (≈800 ms). Less sensitive to sample clock jitter. LO: Fast-settling mode (≈200 ms). Some narrow-band noise modulation may result from jitter on the $\overline{LR}$ clocks. This signal may be asynchronous with respect to the crystal frequency, and dynamically changed, but is normally pulled up or pulled down on a static basis.
PWRDWN	27	36	I	Power-down input. Set HI for inactive, low power dissipation state. Reset LO for normal operation.
N/C	9, 20	1, 5, 8, 11, 12, 15, 17, 19, 22, 23, 26, 29, 33, 34, 37, 39, 41, 44		No connect. Reserved. Do not connect.

Power Supply Connections

Pin Name	DIP	I/O	TQFP	Description
V_{DD}	7, 22	I	6, 28	Positive digital voltage supply.
GND	8, 14, 21	I	7, 16, 27	Digital ground. Pin 14 (DIP) and Pin 16 (TQFP) need not be decoupled.

Performance Graphs

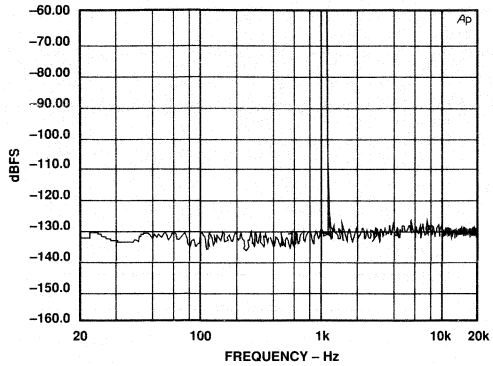


Figure 15. Dynamic Range from 20 Hz to 20 kHz, −60 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

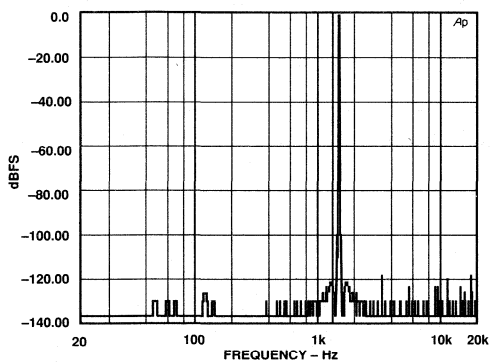


Figure 16. 1 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

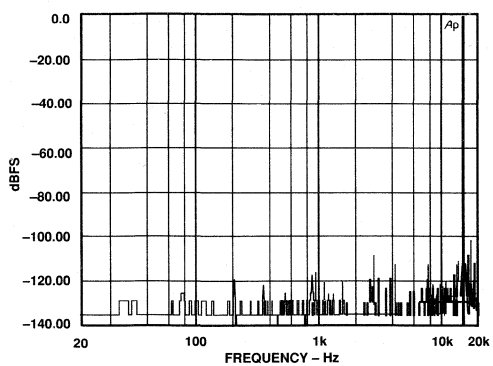


Figure 17. 15 kHz Tone at 0 dBFS, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

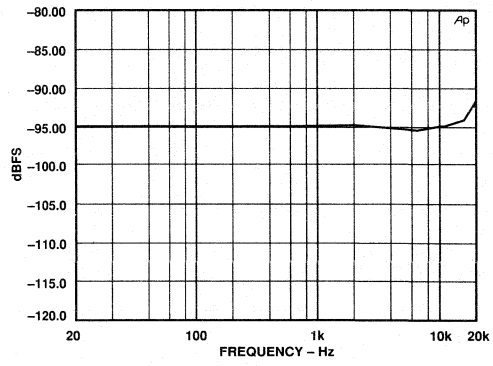


Figure 18. THD+N vs. Frequency, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, Full-Scale Input Signal

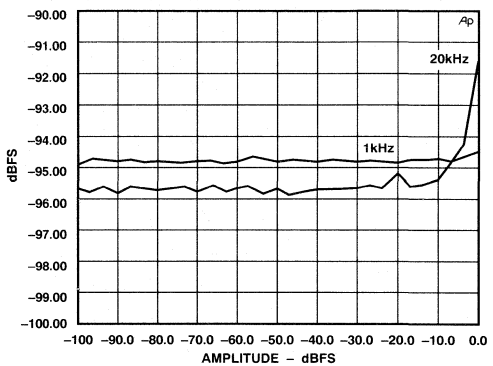


Figure 19. THD+N vs. Input Amplitude, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 1 kHz and 20 kHz Tones

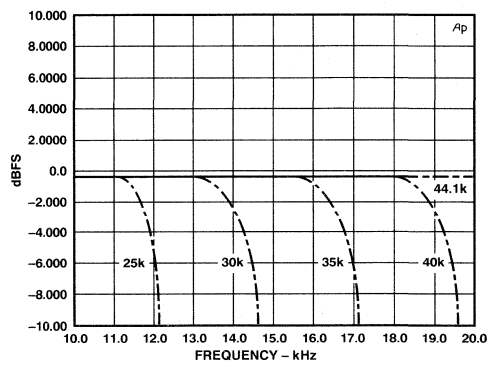


Figure 20. Digital Filter Signal Transfer Function, 10 kHz to 20 kHz, 44.1 kHz Input Sample Frequency, 44.1, 40, 35, 30 and 25 kHz Output Sample Frequencies

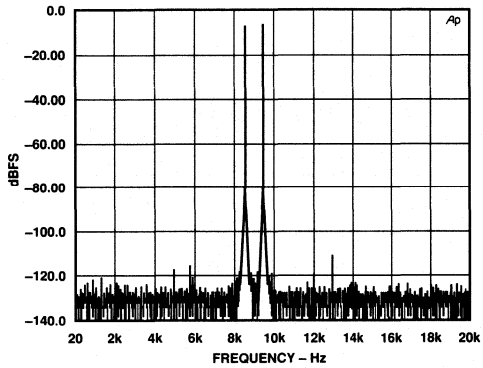


Figure 21. Twintone, 10 kHz and 11 kHz, 44.1 kHz Input Sample Frequency, 48 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

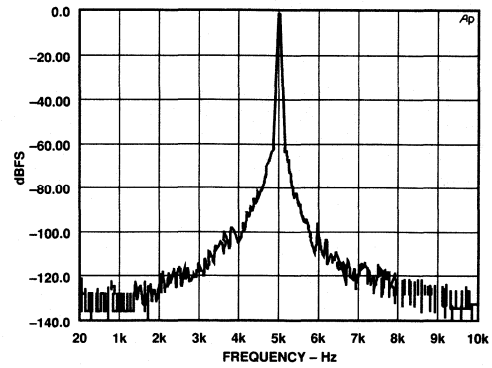


Figure 22. 5 kHz Tone at 0 dBFS with 100 ns p-p Binomial Jitter on L/$\overline{R}$ Clocks, Fast Settling Mode, 48 kHz Input Sample Frequency, 44.1 kHz Output Sample Frequency, 16k-Point FFT, BH4 Window

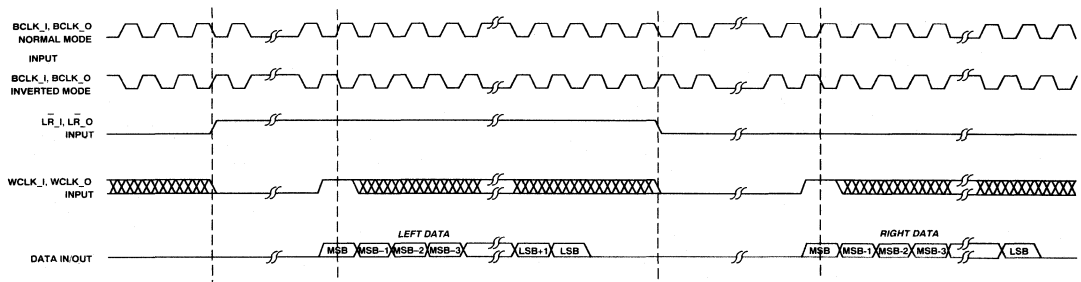


Figure 23. Serial Data Input and Output Timing, Word Clock Triggered Mode

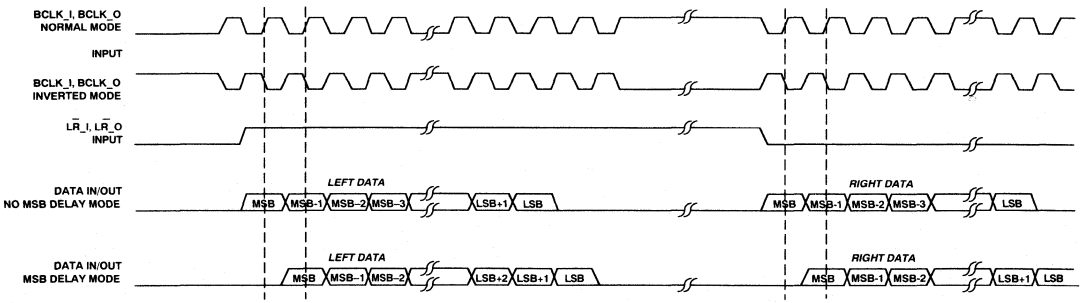


Figure 24. Serial Data Input and Output Timing, Left-Justified Left/$\overline{\text{Right}}$ Clock Triggered Modes

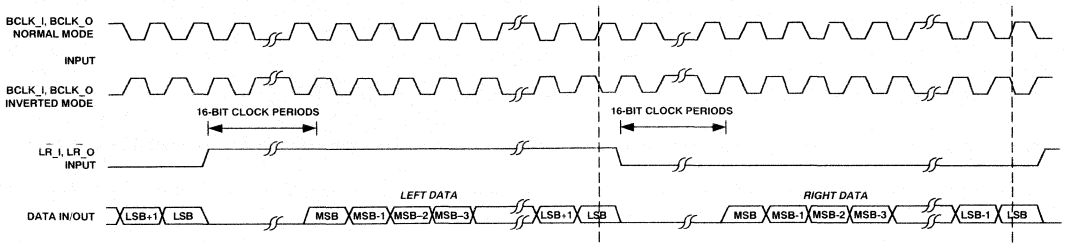


Figure 25. Serial Data Input and Output Timing, Right-Justified Left/Right Clock Triggered Mode

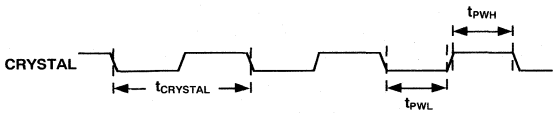


Figure 26. Clock Timing

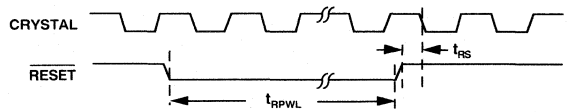


Figure 27. Reset Timing

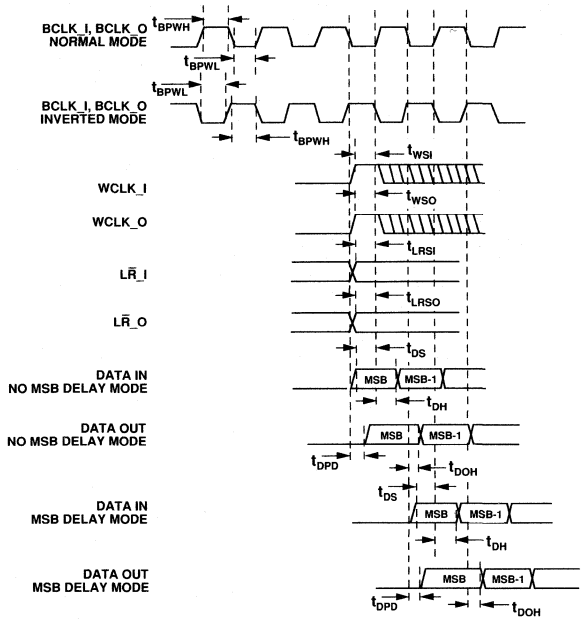


Figure 28. Bit Clock, Word Clock, Left/Right Clock and Data Timing

ANALOG DEVICES

Dual-Channel ΣΔ Modulator

ADMOD79*

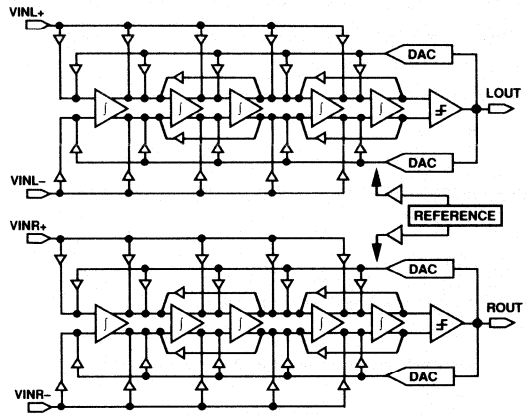
FEATURES

- High-Performance ΣΔ ADC Building Block
- Fifth-Order, 64 Times Oversampling Modulator with Patented Noise-Shaping
- Modulator Clock Rate to 3.57 MHz
- 103 dB Dynamic Range (for 20 kHz Input Bandwidth)
- Differential Architecture for Superior SNR and Dynamic Range
- Dual-Channel Differential Analog Inputs (±6.2 V Differential Input Voltage)
- On-Chip Voltage Reference

APPLICATIONS

- Digital Audio
- Medical Electronics
- Electronic Imaging
- Sonar Signal Processing
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT OVERVIEW

The ADMOD79 Sigma-Delta (ΣΔ) modulator is a building block which can be used to build a superior analog-to-digital conversion system customized to a particular application's requirement. The ADMOD79 is a two-channel, fully differential modulator. Each channel consists of a fifth-order one-bit noise shaping modulator. An on-chip voltage reference provides a voltage source to both channels that is stable over temperature and time. There are separate single-bit digital outputs for each channel. The ADMOD79 accepts a $64 \times F_S$ input master clock (SMPCLK) that can range from 2.5 kHz to 3.57 MHz.

Input signals are sampled at $64 \times F_S$ on switched-capacitors, eliminating external sample-and-hold amplifiers and minimizing the requirements for antialias filtering at the input. With simplified antialiasing, linear phase can be preserved across the passband. The ADMOD79's proprietary fifth-order differential switched-capacitor modulator architecture shapes the one-bit comparator's quantization noise out of the passband. The high order of the modulator randomizes the modulator output, reducing idle tones in the output spectrum to very low levels. The ADMOD79's differential architecture provides increased dynamic range and excellent common-mode rejection characteristics. Because its modulator is single-bit, the ADMOD79 is inherently monotonic and has no mechanism for producing differential linearity errors. Analog and digital supply connections are separated to isolate the analog circuitry from the digital supplies.

The ADMOD79 is fabricated in a BiCMOS process and is supplied in a 0.6" wide 28-lead cerdip package. The ADMOD79 operates from ±5 V power supplies over the temperature range of –25°C to +70°C.

This is an abridged data sheet. To obtain the most complete, current version, call our DSP Bulletin Board Service at 617-461-4258 (8 data bits, no parity, 1 stop bit, 300/1200/2400/9600/14400 baud).

ADMOD79–SPECIFICATIONS

TEST CONDITIONS UNLESS OTHERWISE NOTED

Supply Voltages	±5	V	Input Signal	974	Hz
Ambient Temperature	25	°C		–0.5	dB Full-Scale
Input Clock (SMPCLK)	3.072	MHz	Passband	0 to 20	kHz

	Min	Typ	Max	Units
ANALOG PERFORMANCE				
Dynamic Range (0 Hz to 20 kHz, –60 dB Input)				
No A-Weight Filter	100	103		dB
With A-Weight Filter		105		
Signal to (Distortion + Noise)				
Full-Scale Input	90	96		dB
–20 dB Input		83		
Trimmed[1] Signal to (Distortion + Noise)				
Full-Scale Input	93	98		dB
–20 dB Input		83		dB
Trimmed[1] Signal to Total Harmonic Distortion				
Full-Scale Input		98		dB
–20 dB Input		100		dB
Analog Inputs				
Differential Input Range[2]	±5.89	±6.2	±6.51	V
Input Impedance at Each Input Pin		7.0		kΩ
DC Accuracy				
Gain Error			±5	%
Interchannel Gain Mismatch			±0.15	dB
Gain Drift		±200		ppm/°C
Offset Error (Referrred to Input)		±0.057	±0.343	% of FS
Offset Drift (Referred to Input)		±13		ppm/°C
Voltage Reference*	2.4	2.8	3.2	V
Crosstalk (EIAJ Method)	100			dB
Interchannel Phase Deviation		±0.001		Degrees
DIGITAL TIMING (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = –5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
t_{SCP} SMPCLK Period	0.28		400	µs
t_{SCPWL} SMPCLK LO Pulse Width	140			ns
t_{SCPWH} SMPCLK HI Pulse Width	140			ns
t_{OPD} Propagation Delay, SMPCLK Falling Edge to ROUT, LOUT			100	ns
t_{RPD} Propagation Delay, SMPCLK Rising Edge to $\overline{\text{RRESET}}$, $\overline{\text{LRESET}}$			125	ns
DIGITAL I/O (Guaranteed over 0°C ≤ T_A ≤ 70°C, AV_{SS} = –5.0 V ± 5%, AV_{DD} = DV_{DD} = +5.0 V ± 5%)				
Input Voltage HI (V_{IH})	3.4			V
Input Voltage LO (V_{IL})			0.8	V
I_{IH} @ V_{IH} = 5 V			10	µA
I_{IL} @ V_{IL} = 0 V			10	µA
Output Voltage HI (V_{OH} @ I_{OH} = 360 µA)	4.0			V
Output Voltage LO (V_{OL} @ I_{OL} = 1.6 mA)			0.5	V
POWER SUPPLIES				
Current, DV_{DD}		1.0	1.5	mA
Current, $AV_{DD}1$, $AV_{SS}1$		76	95	mA
Current, $AV_{DD}2$, $AV_{SS}2$		8	12	mA
Current, $AV_{DD}1$, $AV_{SS}1$ – Power Down		14	20	mA
Dissipation				
Operation (All Supplies)		845	1078	mW
Power Down (All Supplies)		225	328	mW
Power Supply Rejection				
1 kHz 300 mV p-p Signal at Analog Supply Pins		102		dBFS
TEMPERATURE RANGE				
Specifications Guaranteed		+25		°C
Functionality Guaranteed	–25		+70	°C
Storage	–60		+100	°C

NOTES

[1]Differential gain imbalance manually trimmed to eliminate second harmonic. See "Application Issues" below.

[2]The differential input range is twice the range seen at each input pin. The input range corresponds to the full-scale digital output range.

*Guaranteed, not tested.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

	Min	Max	Units
DVDD to DGND and $AV_{DD}1/AV_{DD}2$ to AGND	0	6	V
$AV_{SS}1/AV_{SS}2$ to AGND	–6	0	V
$AV_{SS}2$ to $AV_{SS}1$	–0.3		V
Digital Input to DGND	–0.3	DV_{DD} + 0.3	V
Analog Inputs	$AV_{SS}1$ – 0.3	$AV_{SS}1$ + 0.3	V
AGND to DGND	–0.3	0.3	V
Reference Voltage	Indefinite Short Circuit to Ground		
Soldering		+300	°C
		10	sec

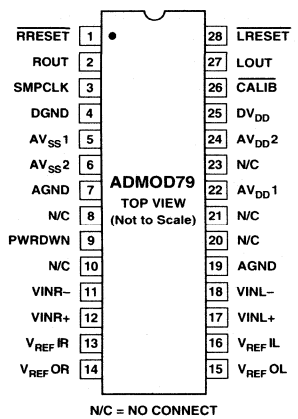
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
ADMOD79JQ	0°C to +70°C	Cerdip	Q-28

*For outline information see Package Information section.

PIN CONFIGURATIONS



N/C = NO CONNECT

PIN DESCRIPTIONS

Pin Number	Mnemonic	Input/ Output	Description
1	$\overline{\text{RRESET}}$	O	Right Modulator Reset
2	ROUT	O	Right Bitstream Modulator Output
3	SMPCLK	I	3.072 MHz (Nominal) Modulator Input Clock
4	DGND	I	Digital Ground
5	$AV_{SS}1$	I	–5 V Analog Supply
6	$AV_{SS}2$	I	–5 V Analog Logic Supply
7	AGND	I	Analog Ground
8	N/C		No Connect
9	PWRDWN	I	Power Down
10	N/C		No Connect
11	VINR–	I	Right Inverting Input
12	VINR+	I	Right Noninverting Input
13	$V_{REF}IR$	I	Right Reference Input
14	$V_{REF}OR$	O	Right Reference Output
15	$V_{REF}OL$	O	Left Reference Output
16	$V_{REF}IL$	I	Left Reference Input
17	VINL+	I	Left Noninverting Input
18	VINL–	I	Left Inverting Input
19	AGND	I	Analog Ground
20	N/C		No Connect
21	N/C		No Connect
22	$AV_{DD}1$	I	+5 V Analog Supply
23	N/C		No Connect
24	$AV_{DD}2$	I	+5 V Analog Logic Supply
25	DV_{DD}	I	+5 V Digital Supply
26	$\overline{\text{CALIB}}$	I	Calibration
27	LOUT	O	Left Bitstream Modulator Output
28	$\overline{\text{LRESET}}$	O	Left Modulator Reset Signal

4

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADMOD79 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Technical Support
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Bulletin Board System Guide

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

OVERVIEW

Analog Devices' DSP/Signal Computing BBS (Bulletin Board System) is a forum where people interested in DSP (digital signal processing) and signal computing technology can access information and exchange ideas. It provides instant gratification to its users by letting them access data and files almost immediately, keeping them on the cutting edge of this flourishing technology.

The BBS also acts as a communications medium through which users can e-mail questions and comments, including requests for particular information, to our applications engineers. It gives us at Analog Devices the opportunity to receive feedback directly from our customers so that we can improve the BBS to suit our customers' and users' needs.

In addition, Analog Devices offers complete codec support for the Microsoft Windows 3.1, Windows NT, Win95, and the IBM OS/2 environments. SoundPort drivers and demonstration applets that control full duplex capture and playback operation, data formatting, and mixing functions are available on the BBS.

This BBS Guide reflects the most recent enhancements—based on requests from our customers—to the BBS, which includes the following features:

- 24-Hour Automatic Return Fax Service
- E-mail Service to Other BBS Users and ADI Applications Engineers
- User Upload/Download Libraries
- Signal Computing Information and Upgrades
- ADI's *DSPatch*® "Q & A" Collections
- Discussion Groups (Forums) for BBS Users

If the BBS appears slightly different from how it is described in this guide, it is because we are trying to match the needs of our customers by continually upgrading and modifying the BBS to better serve our users.

Please e-mail recommendations, suggestions, or questions about the bulletin board to the Sysop or call the DSP Applications Assistance Line at (617) 461-3672.

GENERAL STRUCTURE & CONVENTIONS

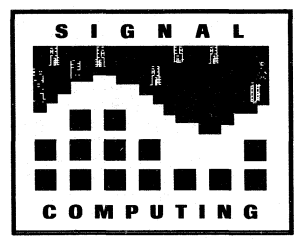
The BBS menu structure is arranged according to the logic of a tree configuration (see Figure 1). Users can navigate through the submenus by entering specific letters as prompted by the system.

COMMAND CONVENTIONS

- **Boldface** letters or numbers surrounded by brackets < > indicate commands entered by the user. (Do not type the brackets.)
- <**Return**> represents the Return key (or "Enter" key on some keyboards).
- `Courier` font represents on-screen messages.

All BBS commands consist of a single letter or a single number.

At the Main Menu, for example, enter your selection by typing the letter of the menu item at the prompt:



S) Signal Computing Information	M) Messages (Send/Read)
D) DSP Processor Information	H) Help (with this BBS)
P) SoundPort® Information	C) Comment to the Sysop
F) Forums (Discussion Groups)	X) Exit System (Log Off)

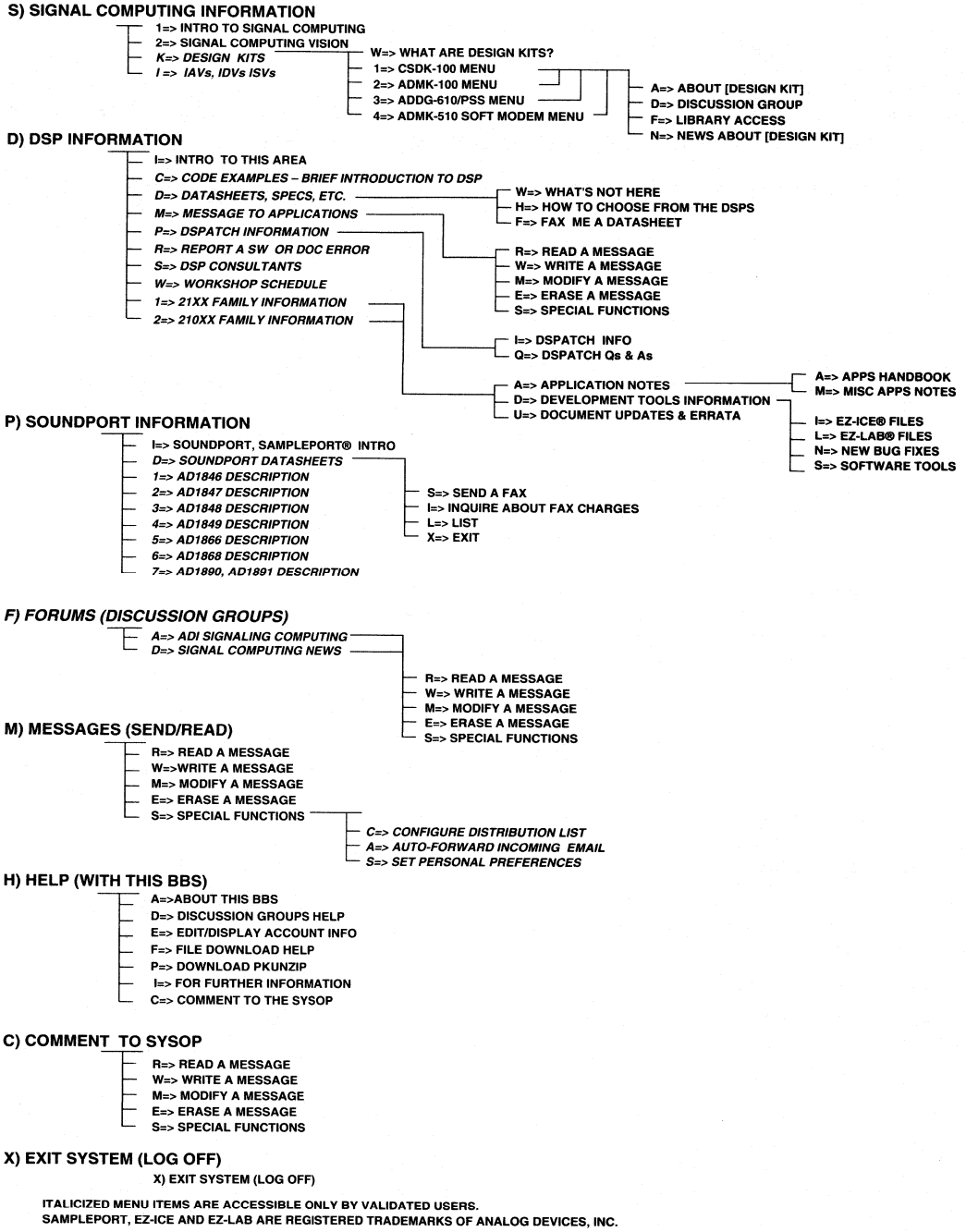


Figure 1. Bulletin Board Menu Structure

To return to the previous menu, type <**X**> then press <**Return**>. To return to the Main Menu from a submenu, type <**X**> at the prompt(s) until you reach the Main Menu. For help with a selection, type <**?**> then press <**Return**> at any prompt.

CALLING THE BBS

To access the BBS, you need a computer with a communications package, a modem, and a telephone line. Use the following settings to connect to the system:

BBS Telephone Number:	(617) 461-4258
Data Bits:	8 Bits
Stop Bits:	1 Stop Bit
Duplex:	Full Duplex
Parity:	None
Baud Rate:	9600, 2400, 1200, or 300

The host modem on the BBS has an autobaud feature that automatically adjusts to the speed of the incoming modem.

PKUNZIP: DATA COMPRESSION UTILITY

To save space and download time, we recommend that you download the data compression utility, PKUNZIP. This IBM PC utility compresses data using the ZIP format. (Note that PKUNZIP is not compatible with Macintosh systems.)

To download PKUNZIP, type <**H**> for *Help* (with this BBS) at the Main Menu to reach the following submenu:

A=> About this BBS Software
D=> Discussion Groups Help
E=> Edit/Display Account Information
F=> File Download Help
M=> Messages Help
P=> Download PKUNZIP.EXE

Type <**P**> for *Download PKUNZIP.EXE* to reach the next submenu:

F=> File Directory
D=> Download a file
U=> Upload a file
S=> Select a LIB
?=> More options

Type <**D**> for *Download a File*, then type <**PKUNZIP**> at the `Filename?` prompt. Choose a download option from the list and the BBS begins downloading the file.

Note: Type **Ctrl** <**Q**> at any time to abort the downloading process.

FIRST TIME USERS: GETTING VALIDATED

Before navigating through the BBS, new users must first create a BBS account by answering a series of questions that relate to personal identification, employment, and interests in signal computing and DSP.

After typing <**new**> at the prompt, the system responds with questions like these for you:

`Please enter your first and last name:`

Chris Smith `then press` <**Enter**>

`Now enter your company name:`

Computers International `then press` <**Enter**>

These questions should take approximately 10 minutes to answer.

After completing the questions, the BBS prompts you to choose a user-id, which can be your real name or a different one, and a password. Once the BBS receives this information, the following message appears on the screen: *Your account has now been created!*

VALIDATING YOUR ACCOUNT

After completing the "New User" questions to initialize your account, you have limited access to the BBS until your account has been processed or *validated*. The validation process takes between 24 and 36 hours, which means that you can access all areas of the BBS the next time you log in.

Please note that until your account has been validated, you cannot post messages or obtain data sheets, specifications, commented code, or ADSP-21xx and ADSP-210xx Family information.

LOGGING ON: FOR VALIDATED USERS

Once you are connected to the BBS, the word CONNECT appears on your screen. To continue, press <**Return**>.

The following message appears on your screen: *Welcome to the DSP and Signal Computing BBS.*

Enter your user-id (log in name) and password, then press <**Return**> to access the Signal Computing Main Menu:

S) Signal Computing Information
D) DSP Processor Information*
P) SoundPort Information*
F) Forums (Discussion Groups)*
M) Messages (Send/Read)
H) Help (with this BBS)
C) Comment to the Sysop
X) Exit System (Log Off)

*Not accessible by non-validated users.

Validated users are allowed three 60 minute sessions per day, for a total of 180 minutes of BBS on-line time per day. After 60 minutes, users are automatically disconnected. If you need more than one hour of on-line time, disconnect and then reconnect to the BBS later.

Note: You can dial up the BBS a maximum of three times per day.

NAVIGATING THE MAIN & SUBMENUS: FOR VALIDATED USERS ONLY

ACCESSING ADSP-21xx & ADSP-210xx FAMILY INFORMATION

To find ADSP-21xx and ADSP-210xx Family information, data sheets, applications notes, and code examples, at the Main Menu

1. Type <**D**> for *DSP Processor Information.*

   The following submenu appears:

   I=> Intro to this Area
   C=> Code Examples
   D=> Data sheets, Specs, etc.
   M=> Message to Applications
   P=> DSPatch Information
   R=> Report a SW or Document Error
   S=> DSP Consultants
   W=> Workshop Schedule
   1=> 21xx Family Information
   2=> 210xx Family Information

For document fax service, choose <**D**>. (See "Document-by-Fax Services" in this guide for more information.)

Depending on the DSP processor family you want to access, choose *1* or *2* to reach this next menu, which gives you the option of selecting applications notes, development tools information and documentation updates:

A=> Applications Notes
D=> Development Tools Information
U=> Documentation Updates & Errata

In this submenu, you can also access the *Applications Handbook, Volumes 1 and 2,* by choosing <**A**>.

ACCESSING SIGNAL COMPUTING INFORMATION

The Main Menu option, *S) Signal Computing Information,* contains information on the following Signal Computing Design Kits: CSDK-100; ADMK-100; ADDG-610/PSS; and, ADMK-510/Soft Modem Menu.

For information about a particular design kit, its respective discussion group, available Library files, or news updates, at the Main Menu.

1. Type <**S**> for *Signal Computing Information.*

   The following submenu appears:
   1=> Introduction to Signal Computing
   2=> The Signal Computing Vision
   K=> Hardware Design Kits
   I=> IAVs, IDVs, ISVs
   T=> Software Development Tools

2. Type <**K**> for *Design Kits* to reach this menu:

   1=> CSDK-100 Menu
   2=> ADMK-100 Menu
   3=> ADMK-610/PSS Menu
   4=> ADMK-510 Soft Modem Menu

Choose a design kit by typing the appropriate number at the prompt. Any selection calls up the following submenu with information about the design kit you selected in the previous menu.

For example, if you choose **1**, the following menu appears:

A=> About **CSDK-100** Design Kit
D=> **CSDK-100** Discussion Group
F=> Files for **CSDK-100**

For information about IAVs (Independent Algorithm Vendor), IDVs (Independent Device Vendor), and ISVs (Independent Software Vendor), at the Signal Computing Menu:

Type <**I**> for IAVs, IDVs, and ISVs at the prompt.

A list of companies appears.

Choose a particular company by entering its corresponding number.

To exit menu(s), type <**X**> and <**Return**> to reach the Main Menu or previous submenus.

ACCESSING SOUNDPORT INFORMATION

Analog Devices' AD1848 Family of CD-quality stereo codecs is the industry standard for voice annotation of documents, voice-controlled commands, voice navigation through Microsoft Windows,* and sound recording and playback.

To obtain product data sheets (and fax service) and descriptions, at the Main Menu,

Type <**P**> for *SoundPort Information,* then press <**Return**> for the following submenu:

I=> SoundPort, SamplePort Intro.
D=> SoundPort Data sheets
F=> SoundPort Files
1=> AD1846 Description
2=> AD1847 Description
3=> AD1848 Description
4=> AD1849 Description
5=> AD1866 Description
6=> AD1868 Description
7=> AD1890, AD1891 Description

For a brief background on SoundPort , select <**I**> and press <**Return**>. For a specific codec description, select the corresponding number and press <**Return**>.

FORUMS & DISCUSSION GROUPS

The BBS Forum lets users post messages or read messages written by other users about topics related to a particular area in signal computing. You can address and send a message to specific users in a Forum, but

*Microsoft is a registered trademark of Microsoft Corp.

note that all users who have access to that particular forum can read your message. (If you want to send a private e-mail message to a BBS user, follow the e-mail procedure in the "E-Mail Services" section of this guide.)

To access Discussion Groups, at the Main Menu,

Type <**F**> for *Forums (Discussion Groups).*

The following menu appears:

A=> ADI Signal Computing Information
S=> Signal Computing News

Choose <**A**> to post or read information about applications.
Choose <**S**> to post or read information about news items.

In addition to posting and answering forum messages, users can "quickscan" through posted messages for particular information by using their own personally-configured searching and scanning facility by entering keywords. Quickscan tracks the last message read in each discussion group so that a search includes only messages that you have not yet read.

To enter Quickscan from the Forum Menu, use the following shortcut:

Type **QK** at the prompt and press <**Return**>.

The following menu appears:

S...scan through file descriptions one at a time
L...list file descriptions (non-stop) to your display
K...keyword-search for specific files.

Use these other shortcuts to Quickscan by entering them at the Main Menu:

- Type **QS** to immediately initiate a Quickscan
- Type **QL** to list file descriptions
- Type **QC** to configure the Quickscan option

After scanning through the Forum menu, the system provides prompts for other options such as replying publicly and downloading files.

FINDING DATA SHEETS & RELEASE NOTES

The BBS contains data sheets for the ADSP-21xx and ADSP-210xx Family software and hardware development tools and for stereo codecs in the AD1848 Family. Also available is a matrix that illustrates the different features of Analog Devices' ADSP-2100 Family processors.

To find ADSP-21xx and ADSP-210xx Family data sheets, at the Main Menu

Type <**D**> for *DSP Processor Information,* then type <**D**> for *Data sheets, Specs, etc.*, at the submenu.

To find data sheets for SoundPort and the AD1848 Family of stereo codecs, at the Main Menu, type <**P**> for SoundPort Information.

At either menu, you can select a list of available data sheets and obtain fax service.

E-MAIL SERVICES

The BBS e-mail messaging service lets you mail privately to other users or publicly in a discussion group. To access the e-mail messaging service, at the Main Menu type <**M**> for *Messages (Send/Read).*

The following submenu appears:

R=> Read message(s)
W=> Write a message
M=> Modify a message
E => Erase a message
S => Special functions
X=> Exit from E-mail

After writing messages, type **Ctrl** <**G**> when finished to receive prompts for the following options : attach files to send with the message or mail a copy of your message to a discussion group.

To specify your preference for handling incoming mail and to personalize your e-mail addresses,

Type <**S**> for *Special functions* to access this menu:

C=> Configure distribution list
A=> Auto-forward incoming email
S=> Set personal preferences

Under the option, <**S**> *Set personal preferences,* the system prompts you with a series of mail handling questions. Answer <**Y**> for yes or <**N**> for no when appropriate.

DOCUMENT-BY-FAX SERVICES

You can receive data sheets or other documents listed in the BBS library files through the Analog Devices' fax service within 24 hours. The library includes data sheets for DSPs (ADSP-2101, ADSP-2105, ADSP-2111, ADSP-2115, ADSP-21020), mixed-signal processors (AD28msp01 and AD28msp02), codecs (AD1848 and AD1849), and the most requested release notes.

To receive DSP data sheets by fax, at the Main Menu

Type <**D**> for *DSP Processor Information* for DSP data sheets
At the submenu, type <**D**> for *Data sheets*
At the next submenu, type <**F**> for *Fax me a data sheet*
then <**S**> for *Send a fax.*

Lengthy data sheets and documents are broken into sections for faxing to let you select a part or the entire document.

The BBS prompts you for the phone number to which it should fax the document. Note that the area code and phone number must be separated by a slash—a diagonal mark (/).

After entering the appropriate phone number, you can include a text message that is written on the fax cover sheet by entering <**Y**> at the prompt and pressing <**Return**>. Users can also send a copy of their message to a discussion group by typing <**Y**> at the prompt, "Do you want to cc anyone else? Y/N."

UPLOAD/DOWNLOAD LIBRARIES

The BBS Library of files, LIBs, contain files of information (data sheets, specifications, and release notes, for example) that can be uploaded and downloaded. They are structured according to a DOS directory of files and they adhere to the same labeling and filing formats:

FILENAME.EXT

(One to eight characters, a dot, and one to three characters)

To access a list of LIBs, type <**S?**> at the Library Menu and then press

<Return>

The BBS prompts you with commands for directory listings, file searching and scaling, downloading, and tagged files—marking files in a the directory to be downloaded. The following list shows some common LIB commands:

F	File directory for this LIB
F <string>	File search through names and descriptions
D <filename>	Display details on a file with download options
D <file> <protocol>	Download a file
D <keyword>	Keyword scan
D -0	Scan today's uploads
D -1	Scan yesterday's uploads
D -LAST	Scan uploads from the day you were last on-line
D <lib> \ <filename>	Download a file that is in a different LIB

If you know something about the subject of the file, refer to it by keyword

D <keyword>

and get a numbered list of files containing that keyword.

EDITING ACCOUNT INFORMATION: CHANGING YOUR PASSWORD

In the BBS Help menu, you can change your account information, including your address and password, by typing <**H**> for *Help* at the Main Menu to access the following submenu:

A=> About this BBS Software
D=> Discussion Groups Help
E=> Edit/Display Account Information
F=> File Download Help
P=> Download PKUNZIP.EXE
I=> For further information

Type <**E**> for *Edit/Display Account Information* then <**A**> for *Edit/Display Account Information* to reach a record that contains your background information. To modify any field, use the arrow keys to move the highlighted bar to the desired area and type over the existing information. To quit this field and save your changes, type **Ctrl** <**S**>. To quit without saving your changes, type **Ctrl** <**Q**>.

TROUBLESHOOTING QUESTIONS AND ANSWERS

This section describes a few common problems encountered by users when calling the BBS.

Q. *My modem connects to the BBS, but nothing happens when I type any character.*

A. Check the connection between the modem and the computer: the modem may not be correctly connected. Also, make sure that you have the proper cabling (correct connection of transmit and receive lines), and that your computer and modem are set to the appropriate baud rate. (For baud rate information, refer back to the "Setting Up" section of this guide.)

Q. *Whenever I type a character, it appears twice on the screen, but everything the BBS prints is shown only once.*

A. Check your settings. They should be set for full duplex mode. It is likely that your terminal package is set for half-duplex or echo operation.

Q. *How do I make my modem call the BBS?*

A. Depending on the type of modem you have, one of the most common types of modem protocols is the Hayes protocol, a direct connect modem that connects directly to your telephone line, which responds to a specific command set.

The **ATD** command (must be capitalized) dials the modem. If you have a touch-tone phone, the command is **ATDT**. If you are calling the BBS outside the (617) area code, use the command **ATDT1,617,461,4258**.

If you do not have a Hayes compatible modem, check your modem for a DATA/TALK switch. If it has this switch, dial the numbers yourself and immediately toggle the DATA/TALK button to DATA. The BBS should answer your call and connect to your modem.

Q. *I've called the BBS, but nothing happens. My modem never connects.*

A. Try dialing the BBS number with a regular telephone. If you hear the modem carrier signal (a high frequency squeal), check your modem to verify that it is properly connected to the phone line and that it is actually dialing.

Q. *I cannot find the information in the BBS that you say is there.*

A. If you do not have access to the full menu (refer to page two of this guide for the Main Menu items), your account may not be validated. Contact the DSP Applications Assistance Line at (617) 461-3672 or send e-mail to the System Operator (Sysop) to validate your account.

FOR NONVALIDATED USERS

Before an account is validated, users have limited access to BBS files and information, which is reflected in the nonvalidated user Main Menu:

S) Signal Computing Information
M) Messages
H) Help (with this BBS)
C) Comment to the Sysop
X) Exit System (Log Off)

From this menu, users can obtain contextual information about Signal Computing, send e-mail to other BBS users and to the System Operator, and obtain limited help options.

AN ONGOING EFFORT TO SATISFY CUSTOMERS' NEEDS

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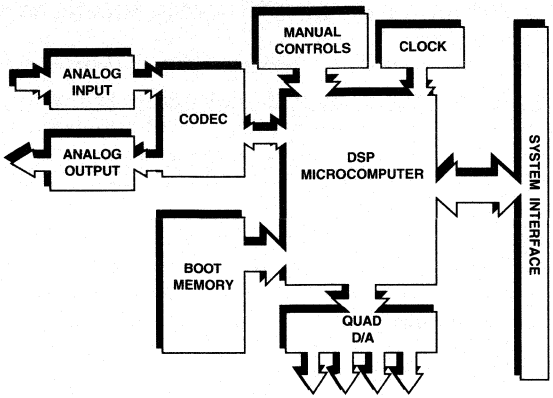
DSP System Development & Programming with the ADSP-2100 & ADSP-21000 Families

2 Three-Day Workshops



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5

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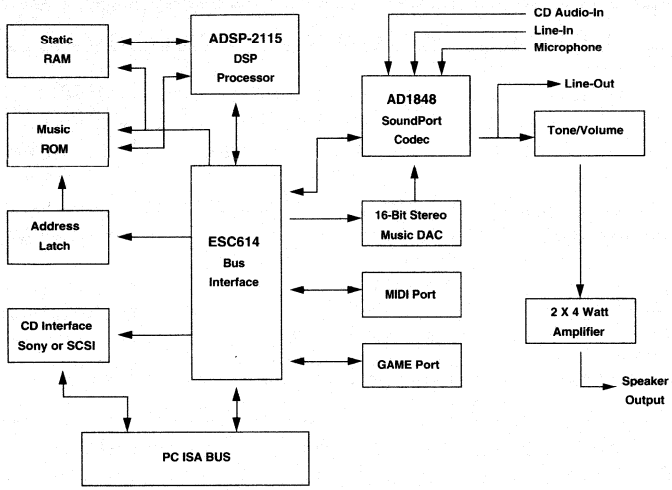
Programming Techniques for the Personal Sound Architecture

A Three-Day Signal Computing Workshop



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Considerations for Selecting a DSP Processor (ADSP-2111 vs. DSP56166)

INTRODUCTION

Digital signal processing applications require high performance computational hardware capable of performing intense mathematical operations in a short amount of time. The performance of a DSP system can be measured as to how well it performs in the following areas:

- Fast and flexible arithmetic
- Dynamic range on multiply/accumulate operations
- Efficient operand fetches (two operands in one instruction cycle)
- Circular buffering capabilities
- Zero overhead program looping and branching

In addition, the DSP processor should be capable of interfacing easily with external devices, be able to access large amounts of memory quickly, be easy to program, and have the support of powerful development tools to ease system debug.

This application note examines the performance of two leading DSP processors, the ADSP-2111 from Analog Devices and Motorola's DSP56000, as to how they meet these requirements.

ARITHMETIC CAPABILITIES

The basis of a good DSP processor is its ability to perform a wide variety of arithmetic and logical operations in a timely manner. The computations should be handled flexibly such that the implementation preserves the order of operations and operands. Too specific an architecture could require rearrangement of an algorithm to fit a given architecture, thereby increasing programming complexity, time, and the possibility of error.

ADSP-2111 Arithmetic Architecture Overview

Figure 1 shows a block diagram of the ADSP-2111 arithmetic section. The ADSP-2111's arithmetic section consists of three independent, parallel-connected computational blocks—an arithmetic logic unit (ALU), multiplier / accumulator (MAC) with 40-bit accumulator, and general purpose barrel shifter. Each computational unit has its own input and output registers. All arithmetic registers can also be used as general purpose data registers. A complete set of background registers is also provided, allowing a single-cycle context switch of all arithmetic registers. The three computational units can also pass information to each other via the Result Bus, which

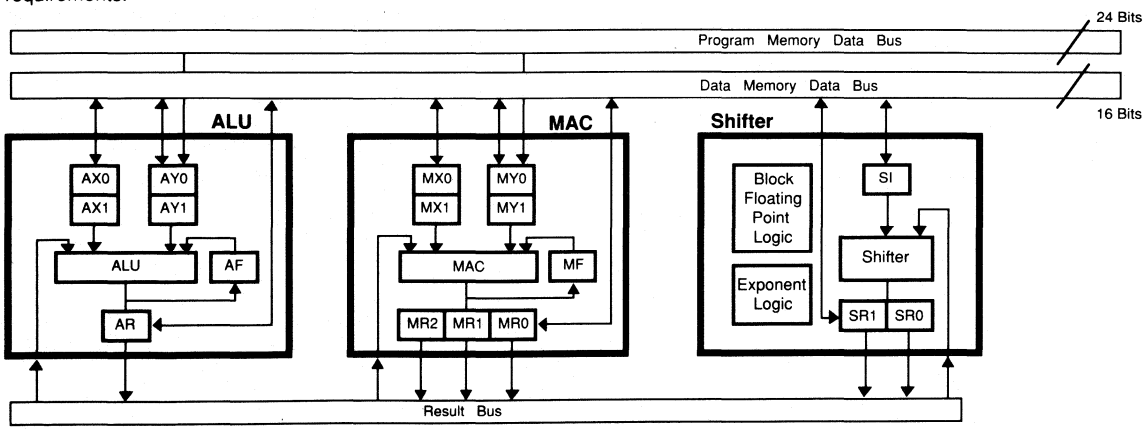

Figure 1. ADSP-2111 Computational Units

eliminates the need for extra data move instructions as any computational unit output can be used directly as an input to any computational unit. ALU and MAC inputs can come from both program and data memory, or any other data register in the processor.

DSP56000 Arithmetic Architecture Overview

Figure 2 shows a block diagram of the DSP56000 Data ALU. The Data ALU handles all of the computational operations within the processor. The Data ALU contains four 24-bit input registers, a multiply-accumulator/logic unit (MAC), two 48-bit accumulator registers, two 8-bit accumulator extension registers, an accumulator shifter (implemented in the data path prior to the MAC), and two data bus shifter/limiter circuits. Inputs for all Data ALU operations come from the four input registers. Computational results are stored in either the A or B accumulators.

Because all DSP56000 computational operations share common input and output registers, extra instructions may be required to handle temporary data storage for intermediate results should an algorithm require multiple interleaved MAC and Arithmetic operations. This would increase both the execution time and program and data memory size requirements of the algorithm. In addition, the lack of a general purpose shifter requires the use of multiple instruction cycles to execute data shifts greater than one bit.

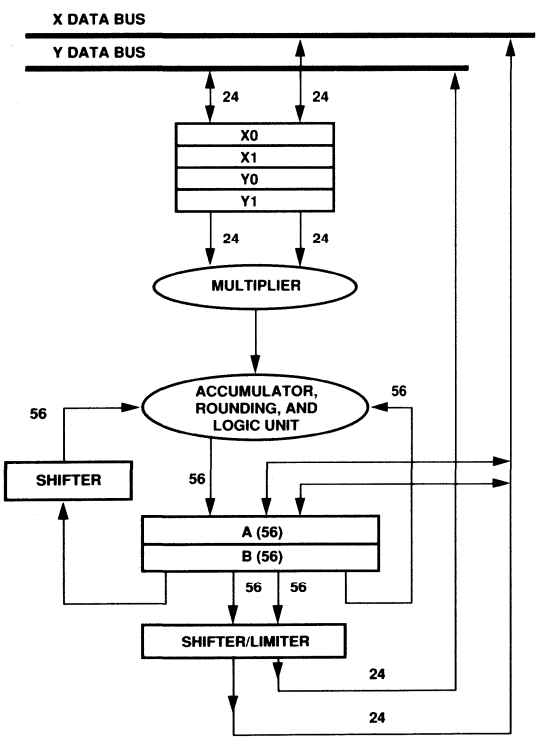

Figure 2. DSP56000 Data ALU

ADSP-2111 ALU

The ADSP-2111 ALU has two X and two Y input registers—AX0, AX1, and AY0, AY1. ALU operations are performed on any X-Y combination of these input registers. The input registers may be loaded from any combination of data and program memory, or from other data registers in the processor. ALU results appear in either the ALU result (AR) or ALU feedback (AF) register. AR and AF can also be used, respectively, as X and Y operands. In addition, MAC and shifter result registers can be used directly as X inputs to the ALU.

The ALU performs mathematical operations on 16-bit data operands. An internal carry bit is always updated during mathematical operations. Addition with carry and subtraction with borrow instructions are provided for implementing multiprecision arithmetic. The ADSP-2111 ALU supports all logic operations as well as a divide primitive and an absolute value function.

Two operands can be fetched or stored in parallel with an ALU operation. This allows for the processor to perform one ALU operation per cycle without speed penalties incurred by operand fetching. All ALU operations execute in a single cycle. ALU operations are coded in a register transfer, algebraic syntax; and all ALU operations can be performed conditionally with no cycle penalty.

Other features of the ADSP-2111 ALU include mode-selectable AR saturation to protect against overflows and six status flags to monitor the condition of the ALU result.

DSP56000 Arithmetic And Logical Operation

Arithmetic and logical operations on the DSP56000 are handled through the accumulator, rounding, and logic unit. For arithmetic instructions, the unit accepts up to three input operands and outputs one 56-bit result in the form *extension:most significant product:least significant product* (EXT:MSP:LSP). When a 56-bit result is to be stored as a 24-bit operand, the LSP can either be truncated or rounded into the MSP. In order to protect against overflows, accumulation registers A and B each have separate limiting circuitry. Arithmetic operations are coded using a mnemonic syntax. No provisions are made for conditional arithmetic, so cycle time is lost on conditional branching.

Logical operations are handled through the logic unit. This unit is 24 bits wide and operates on data in the MSP portion of the accumulator.

ADSP-2111 MAC

The ADSP-2111 multiplier/accumulator (MAC) is separate from the ALU. Like the ALU, it has two X and two Y input registers, MX0, MX1, and MY0, MY1, loadable from either data memory or program memory. Like the ALU, the programmer is free to choose any X-Y input pair. The unit performs both multiplications and multiply-accumulates independently of the ALU, on any X-Y assortment of MAC input registers. Results can be directed to either the MAC result (MR) register or the MAC feedback (MF) register. These registers can also be

used, respectively, as X and Y inputs. ALU and Barrel Shifter result registers can also be used as MAC X-inputs. All MAC operations occur in a single cycle.

The ADSP-2111 performs its mathematical operations on 16-bit data. The data formats of the operands can be any combination of signed or unsigned values, a feature which simplifies the implementation of multiprecision multiplication. The 32-bit multiplier output feeds a 40-bit dedicated add/subtract array, which in turn feeds the Multiplier Result (MR) register set.

The MR register is divided into two 16-bit registers (MR0 and MR1) and an 8-bit extension register (MR2). Because DSP applications frequently deal with values over a wide dynamic range, the extension register is used to allow for 255 full-scale multiply-accumulates before a loss of data can occur. All MAC operations can be performed conditionally with no cycle penalty.

Other MAC features include an overflow status bit, a 16-bit unbiased rounding option, single-cycle conditional MR saturation, as well as the ability to clear all 40 accumulator bits in a single cycle.

DSP56000 MAC Operation

Multiply / accumulate (MAC) operations are performed using the multiplier and accumulator portions of the DSP56000 arithmetic unit. Multiplier inputs can only come from the X or Y registers. The multiplier executes 24-bit x 24-bit parallel two's-complement fractional multiplies. The 48-bit product is right justified and added to the contents of either the A or B accumulator. An 8-bit adder is used as an extension accumulator for the MAC array. Its output is the EXT: portion of the EXP:MSP:LSP format result.

If a 24-bit result is required, the DSP56000 MAC can either truncate the LSP portion of the result or round the result into the MSP.

ADSP-2111 Shifter

Provided as a separate computational unit, the ADSP-2111 barrel shifter can place a 16-bit input value anywhere in a 32-bit output field, from off-scale left to off-scale right, in a single cycle.

The barrel shifter has one input register, SI, but can also accept any computational unit result register as input. The 32-bit Shifter Result (SR) register is divided into two 16-bit sections, SR0 and SR1. The shifter also has an exponent register, SE, which can be loaded either directly from another register or automatically set as a result of exponent detection operation.

In addition to arithmetic (sign extension) and logical (zero fill) shift operations, the barrel shifter also performs exponent detection, normalization, denormalization, block-floating point exponent maintenance, as well as pattern merging. The exponent detection feature provides the user with an efficient means of performing operations using two-word floating-point data formats, utilizing the full dynamic range of a 16-bit mantissa and 8-bit exponent. The block floating point (block exponent detection) allows the normalization of an arbitrary-length frame of data to be normalized to a single exponent, thus simplifying floating point implementations.

All shifter instructions are executed in a single cycle, regardless of the number of bits shifted. All shifter operations can be conditional with no cycle penalty. As with the ALU and MAC, there is a complete set of background registers for the Shifter.

An example ADSP-2111 Shifter instruction is shown below.

```
SR = ASHIFT SI BY -17
```

This instruction performs an arithmetic (sign extended) shift on the contents of the Shifter Input register of 17 bits to the right [multiply by 2^(–17)], and places the result in the Shifter Result register. This instruction executes in a single cycle.

DSP56000 Shifter

The DSP56000 has no general purpose shifter. The accumulator shifter, implemented in the data path prior to the MAC accumulator, is used to shift accumulator input data one bit either to the left or right, pass data through, or force the accumulator to zero. The data shifter/limiters can shift, at most, one bit at a time. This means that shifting a value 32 bits would require 32 instruction cycles.

To implement the 17-bit arithmetic shift shown in the previous section, the following DSP56000 instructions would need to be executed.

```
MOVE    X0, A1    ; load accumulator from input
                  register
ASR     A         ; arithmetically shift
                  accumulator 1 bit to right
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
ASR     A
```

This operation takes the DSP56000 18 cycles to execute and uses 18 instruction words. To save code space, the shift instructions could be placed in a DO loop, requiring only 4 instruction words, but 21 instruction cycles to execute. Compare that to the ADSP-2111's single-cycle, single-instruction execution.

The DSP56000 has no exponent detection circuitry, so two-word floating-point mathematics is difficult to implement.

Computational Summary

Table 1 summarizes the comparison of computational capabilities between the ADSP-2111 and the DSP56000. While the DSP56000 provides for high dynamic range multiply accumulates, the lack of a general purpose shifter and the availability of only four input registers shared by the entire computational unit can make general purpose mathematic operations somewhat cumbersome. Algorithms may have to be altered if additions, MACs, and shifts are interleaved, as all functions share common input and output registers. There is also no provision made for background registers, so that during interrupt processing, time must be spent explicitly saving the contents of the data registers. In addition, arithmetic operations cannot be performed conditionally, thereby requiring additional cycles to handle conditional program branching.

The ADSP-2111 was designed to provide maximum flexibility for arithmetic operations. By having three separate computational units with their own input and output registers, and allowing any computational result to be used directly as a computational input, the processor can be used to implement a wide variety of algorithms without significant rearrangement of the algorithm. A general purpose shifter with built-in exponent detection logic further adds to this flexibility by allowing the programmer to implement arbitrary data scaling and two-word floating-point operations easily. A complete set of data background registers speeds up interrupt processing by allowing a complete single-cycle context switch of all computational data registers. Furthermore, all arithmetic operations can be conditional on any processor condition without cycle penalties.

DATA ADDRESSING

A digital signal processor's ability to perform fast arithmetic is wasted if the processor cannot fetch the required data fast enough to keep pace with the calculations. Many DSP algorithms require that both data operands and coefficients be made available simultaneously. Likewise, circular buffering (modulo addressing) is a natural method for accessing tables efficiently. The architecture of the DSP processor must be able to support these features easily and efficiently.

Figure 3 shows the data address generators of the ADSP-2111. The data address generators of the DSP56000 are shown in Figure 4, which can be found on page 6.

ADSP-2111 Addressing

The ADSP-2111 is based on a modified Harvard architecture. The Harvard architecture means that there are separate data and program memory spaces modified to allow the storage of both opcodes and data in program memory.

There are two independent data address generators (DAGs) in the ADSP-2111. One typically supplies addresses for data memory fetches while the other can supply addresses for data and program memory access. This configuration allows the ADSP-2111's modified Harvard architecture to fetch two data operands simultaneously—one data value from data memory and one data value from program memory. The DAGs are completely separate from the program sequencer, and only address data locations, not opcodes.

Each DAG has four index (I) registers which store memory pointers (addresses), four address modify (M) registers, and four length (L) registers which store circular buffer lengths for modulo addressing. The 14-bit I, M, and L registers can also be used for general purpose data storage.

DAG1 can bit reverse addresses as they are output to the output bus. This zero overhead bit reversing is useful in FFT implementations.

ADSP-2111 Indirect Addressing

With indirect addressing, the address in an I register drives either the data or program memory address bus. While the memory is being accessed, the address is simultaneously updated according to the contents of the specified M register. The specific pairings of I and M registers is up to the programmer. The ability to mix I and M registers is especially useful for two-dimensional addressing or for supporting

DSP Requirement	ADSP-2111	DSP56000
Computational input registers	4 ALU 4 MAC 1 Shifter	4 total
Background register set	✓	No
Single-cycle shifting	0-32 bits left or right	1 bit left or right
Conditional execution of any computation	✓	No

Table 1. Summary of Computational Capabilities

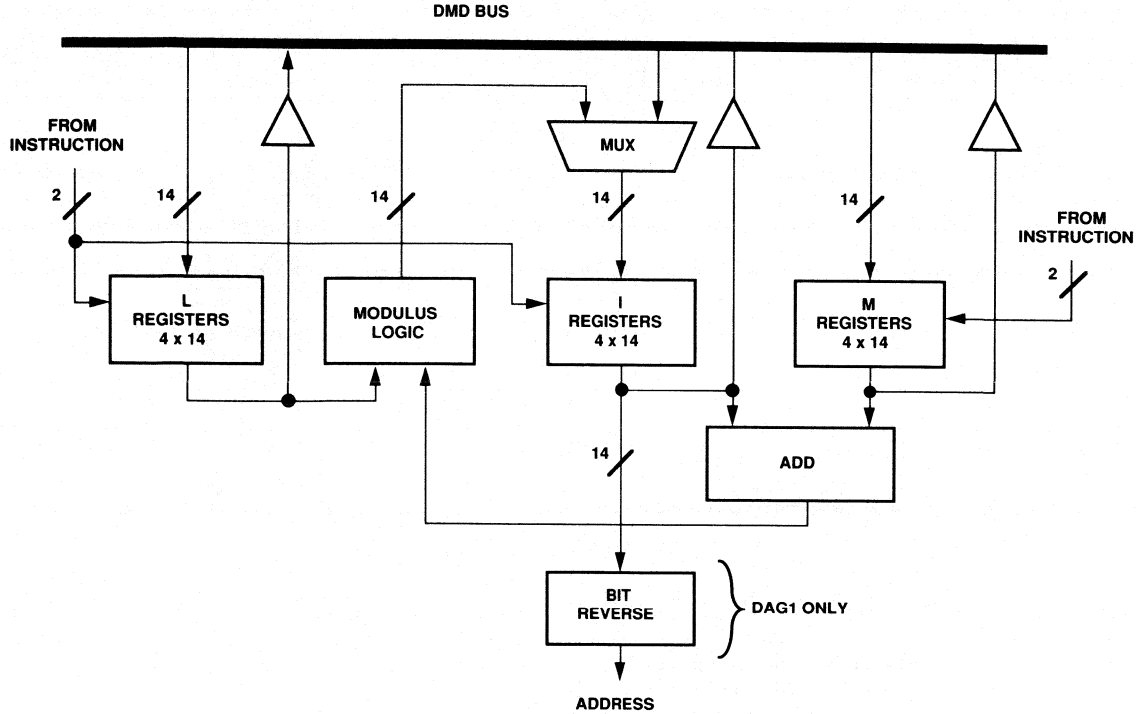

Figure 3. ADSP-2111 Data Address Generator

pointer increment and decrement without continuously loading new modify values. The instruction syntax explicitly shows which register is being used to generate the address and where the data is going; nothing has to be inferred. For example, the assembly language statement

```
DM(I1,M3) = AX0
```

means that the value in register AX0 is loaded into data memory at the address contained in I1. I1 is then updated according to the value contained in register M3. M registers can take values from – 8192 to 8191.

Loading the length of a circular buffer into the L register activates the modulus logic, guaranteeing that the address is kept inside the buffer in a modulo fashion. This structure is maintained automatically by the address generator hardware and does not have to be calculated explicitly by the programmer. Once initialized, circular buffers operate transparently and require no overhead instructions.

ADSP-2111 Direct Addressing

With the 24-bit width of the ADSP-2111 instruction, a full 14-bit address can be specified within a single-word instruction. This feature allows single-cycle access to data located in data memory. The programmer can specify an immediate address or a predefined label variable. Below are some examples of direct addressing memory read instructions.

```
AY1=DM(0x0FE3); {Absolute address specified}

MX0=DM(beta); {The label "beta" is a
               predefined memory buffer label}
```

DSP56000 Addressing

The Address Generation Unit (AGU) of the DSP56000 performs effective address calculations necessary to address data values stored in memory. The AGU is split into identical halves, each containing an address arithmetic logic unit and four sets of three registers—address (R), offset (N), and modifier (M).

The two AGUs can generate two addresses every instruction cycle; one for any two of the XAB, YAB, or PAB memory spaces. Facilities for modulo addressing and address bit reversal are also provided.

DSP56000 Indirect Addressing

Indirect addressing in the DSP56000 is handled through the use of R:N:M register triplets. Register use is restricted in that the registers must be used as triplets, e.g., only N2 and M2 can be used to update R2. No arbitrary R:N pairs can be used. Indirect addressing operations are broken down into a number of modes—no update, postincrement by 1, postdecrement by 1, postincrement by offset N, postdecrement by offset N, indexed by offset N and predecrement by 1.

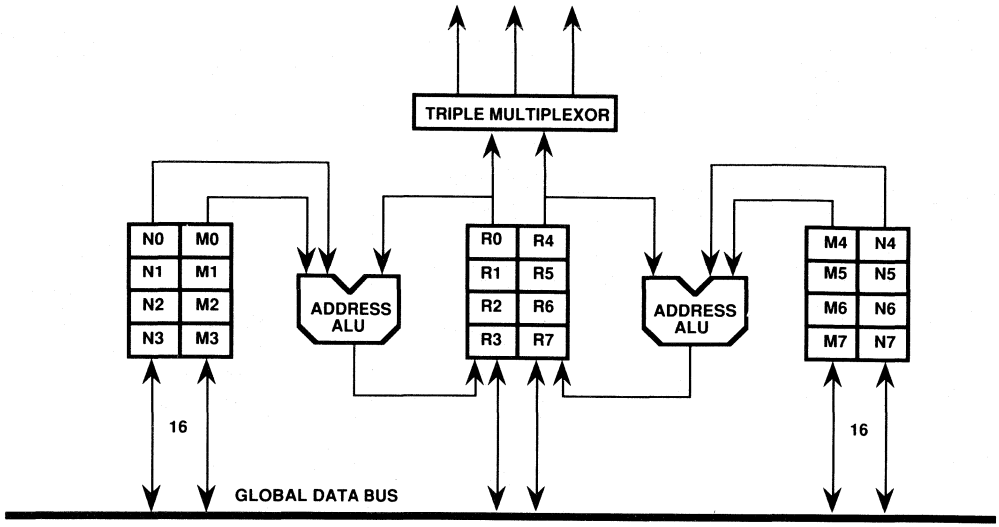

Figure 4. DSP56000 Address Generation Unit

Modulo addressing occurs when a value other than 0xFFFF is loaded into an M register. Address modification is then performed modulo M, with the address pointer remaining in the specified buffer space. Address bit reversing or reverse carry modification can be achieved by setting the appropriate M register to 0x0000.

If any addressing register (R,M,N) is modified, the new value **cannot** be used on the next cycle. A one-cycle delay is introduced due to instruction pipelining. In the ADSP-2111, any value written to any register is available for use on the very next cycle.

DSP56000 Direct Addressing

Direct addressing of memory locations in the DSP56000 can take several forms, some with cycle-time penalties. Moving data from a specific address in memory (for example, MOVE Y:$5432,B0, known as absolute addressing) takes two instruction cycles to execute. If memory between the addresses $0000 to $003F is to be accessed (absolute short addressing), then no penalty is incurred. The speed of memory access is therefore gated by the location of the data. In the ADSP-2111, any location in memory is accessible in a single cycle

Address Generation Summary

Table 2 summarizes the differences between the addressing capabilities of the two processors. Both the ADSP-2111 and DSP56000 have two independent addressing components. Both processors are able to access two operands in a single cycle and both processors support modulo (circular) buffering. The key differences between the two processors is that, depending on addressing mode, the DSP56000 may need multiple cycles to access data, and due to instruction pipelining, any addressing register that is modified cannot be used on the next cycle, thereby reducing the flexibility of the processor for memory access. The ADSP-2111 has single-cycle data access anywhere in its memory space, and any addressing changes are available on the very next cycle.

PROGRAM SEQUENCING

Efficient architectures for signal processing require fast arithmetic capabilities and comparable speed in data addressing and instruction fetching. To fully deliver the speed required for real-world signal processing, a DSP processor must execute its program with little or no overhead spent on maintaining the proper control flow.

Determining the efficiency of program sequencing encompasses many areas of processor control. This comparison focuses on three areas.

- Execution of loops
- Execution of branches and conditional instructions
- Processing of interrupts and subroutine calls

Loops are fundamental to the implementation of DSP algorithms. Many operations, such as sum-of-products, are very repetitive. If a program can be expressed efficiently in looped form, then coding is quite straightforward. Modifying a looped program to change the number of taps in a filter requires very little work.

Quick conditional branching is another natural way to code programs which must respond to its environment. Efficient interrupt servicing is also very important to fast program execution.

Figure 5, located on page 8, shows the architecture of the ADSP-2111 program sequencer. The program control section of the DSP56000 is shown in Figure 6 which can be found on page 9.

DSP Requirement	ADSP-2111	DSP56000
Internal RAM	2K words PM 1K words DM	256 words X 256 words Y
Single-cycle data fetch anywhere in memory	✓	No
Single-cycle fetch of two operands	✓	✓ *
Modify two addresses by two different modify values on every cycle	✓	✓ **

* Location dependent, some memory locations require multiple cycles for access.
** Address and modify registers must be used as a set. Re-indexing an address register requires resetting its corresponding modify register which requires two processor cycles.

Table 2. Summary of Data Addressing Capabilities

ADSP-2111 Program Sequencing

The program sequencer of the ADSP-2111 contains logic that selects a program memory source address and routes the address to the program memory address (PMA) bus. This address selection occurs automatically, in response to the current instruction. The address placed on the address bus can come from either

- the program counter (for sequential addressing),
- a 14-bit address in the instruction word itself, for direct jumps and subroutine calls,
- the PC stack, for returns from subroutines and interrupts, or
- the interrupt logic, for automatic vectoring to the appropriate interrupt service routine.

When an interrupt occurs, the complete status of the processor (stack status, mode status, arithmetic status, and interrupt mask) is automatically pushed onto the status stack as part of the interrupt vector process.

All ADSP-2111 instructions execute in a single cycle. This applies equally to jumps and calls anywhere in the instruction space as well as interrupts. There is no instruction pipelining in the ADSP-2111, so program flow is easy to understand.

ADSP-2111 Looping Capabilities

The ADSP-2111 uses the structure

DO **endlabel** *UNTIL* **condition**

to implement zero overhead software loops. **endlabel** is the label assigned to the last instruction of the loop, and the **condition** can be any arithmetic or counter condition. A "forever" condition is also available to implement infinite loops.

When the *DO ... UNTIL ...* instruction is encountered, the address of the first instruction of the loop is pushed onto the program counter's PC stack, and the address of the last instruction (endlabel) of the loop is pushed onto the program counter's loop stack. Because the upper and lower bounds of the loop are stored internally to the program counter, the loop is able to execute without any additional overhead. DO loops can be nested four deep.

The *DO ... UNTIL ...* instruction operates in a single instruction cycle. For example, a counted loop of three instructions, e.g.,

```
     CNTR = 10;              {initialize counter}
    DO endlabel UNTIL CE; {do until counter expires}
         instruction 1;
         instruction 2;
endlabel: instruction 3;
```

will execute in 32 total instruction cycles; one cycle each for loading the counter and executing the *DO ... UNTIL ...* instruction, and 3 x 10 = 30 instruction cycles for loop execution. Note that program comments are contained between the brackets { }.

DSP56000 Program Sequencing

The Program Controller of the DSP56000 performs address generation (instruction prefetch), instruction decoding, DO loop control, and exception (interrupt) processing. The program controller implements a three-level pipelined architecture in which concurrent instruction, fetch, decode, and execution occur. Although the pipelining operation remains hidden from the user, for the most part it does impose a myriad of restrictions on the programmer. Most DSP56000 operations can execute in a single cycle. There are, however, several critical operations that require multiple instructions to execute, and thus can cause critical delays in program execution. Conditional jumps require up to three instruction cycles to execute. Returns from interrupts and subroutines

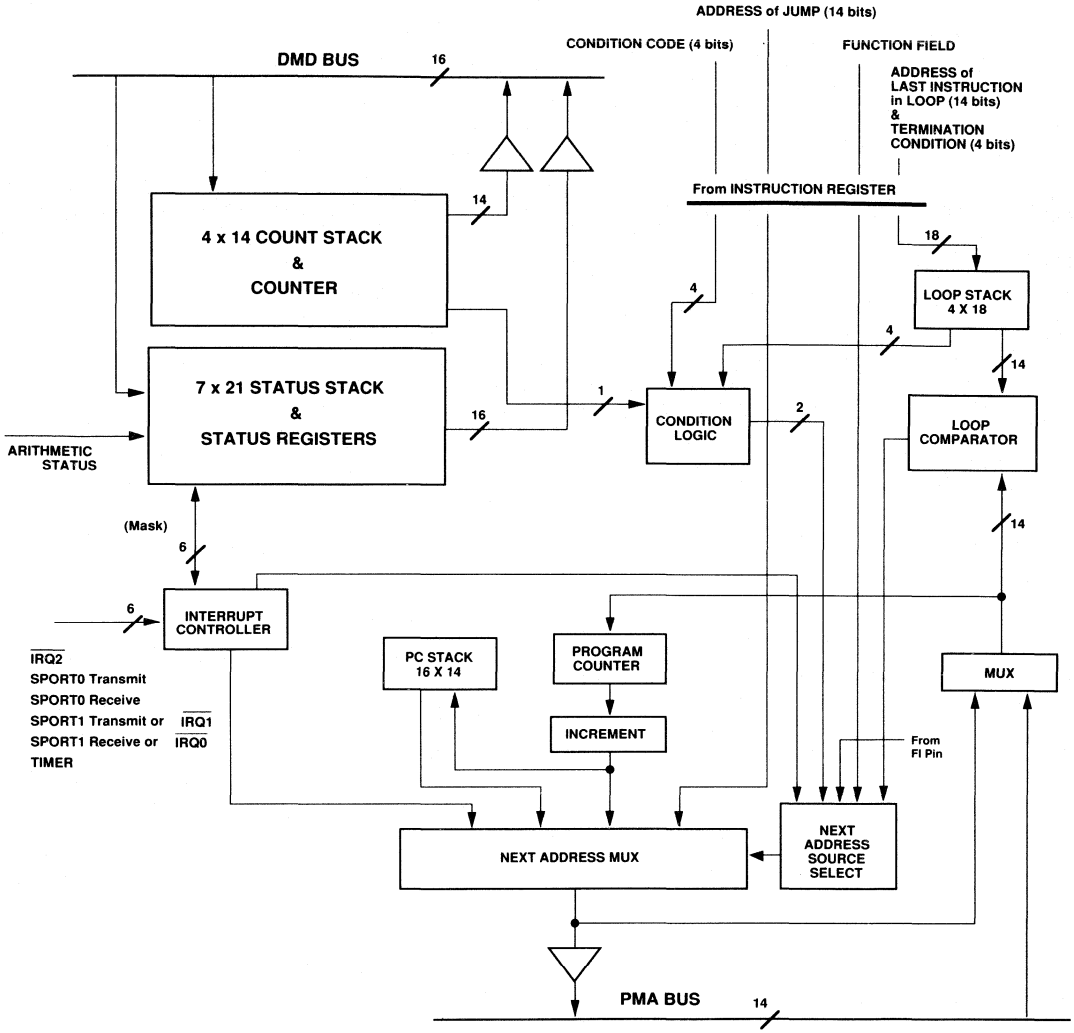

Figure 5. ADSP-2111 Program Sequencer

require two cycles. Because of these instruction latencies, restrictions are placed on which instructions can precede returns, *DO* and *ENDDO* instructions, MOVE, and conditional jump instructions. These multi-cycle instructions also consume extra program memory storage.

DSP56000 Looping Capabilities

The DSP56000 has looping capabilities similar to that of the ADSP-2111. Execution of the *DO* instruction requires three instruction cycles. During the first cycle, the current contents of the loop address and loop counter registers are pushed onto the system stack, and the *DO* instruction's source operand is loaded into the loop counter register. The loop counter register contains the remaining number of times the *DO* loop will be executed. During the second cycle, the current contents of the program counter and status register are pushed on the stack, and the *DO* instruction's address operand is loaded into the loop address register. During the third cycle, the loop flag is set. If the stack is managed to prevent overflow, loops can be stacked indefinitely.

In DSP56000 code, the previous looping example would look like the following.

```
            DO #10, ENDLOOP
              instruction1
              instruction2
              instruction3
ENDLOOP
```

Assuming that the three instructions each take one instruction cycle, this loop would take three instruction cycles to implement the *DO* and 3 x 10 = 30 instruction cycles for the loop—a total of 33. Care must be taken not to violate any

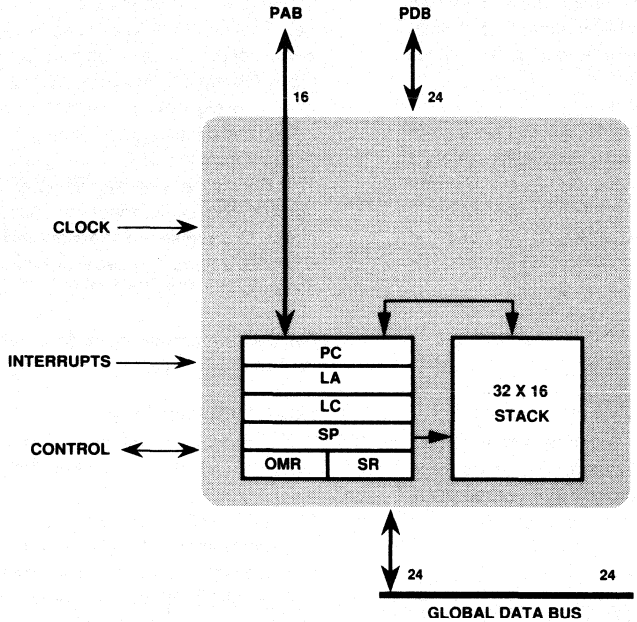

Figure 6. DSP56000 Program Controller

pipelining restrictions prior to the *DO* instruction. An *ENDDO* instruction is provided for early loop termination. Instruction processing would then resume at the first instruction following the loop.

Program Sequencing Summary

Table 3 highlights the key differences in program sequencing capability between the two processors. Due to the instruction pipeline delay, many restrictions are placed on the DSP56000 programmer in terms of the order in which certain instructions may be used. This could invariably lead to rearrangement of algorithms or cycle time wasted waiting for the pipeline to clear.

The ADSP-2111 has **no restrictions** on the order in which instructions can be executed. All ADSP-2111 instructions operate in a single cycle.

DATA COMMUNICATION

The computational efficiency of a processor is negated if the processor is unable to communicate easily and effectively with the outside world. The greatest performance enhancement occurs when the DSP is able to communicate with a variety of external devices, both serially and in parallel. Both the ADSP-2111 and the DSP56000 have provisions for serial and parallel data transfer.

ADSP-2111 Serial Ports

The ADSP-2111 provides two full duplex synchronous serial ports (SPORTs). Each SPORT has an independently programmable serial clock, programmable receive frame sync and transmit frame sync. These control signals can either be internally generated, or received from external devices. Word lengths for each SPORT are independent and user

DSP Requirement	ADSP-2111	DSP56000
All instructions execute in one processor cycle	✓	No
Single-cycle conditional jumps and subroutine calls	✓	No
Single-cycle returns from subroutines and interrupts	✓	No

Table 3. Summary of Program Sequencing Capabilities

programmable from 3 to 16 bits. Built-in hardware is also provided for automatic μ-law and A-law companding of data. The SPORTs support data transfer rates up to the full processor speed of 13 Mbits/second.

For additional functionality, SPORT0 can be set in multichannel mode. Block length can be set to either 24 or 32 words, providing an easy interface with time division multiplexed (TDM) systems. SPORT1 has the option of being configured either as a SPORT or may optionally be configured as two additional external interrupt pins and the Flag Out (FO) and Flag In (FI) pins.

The address generators of the ADSP-2111 can be used in conjunction with the serial ports to provide an automatic data buffering capability. Using the circular buffering capability of the address generator, data can either be received into or transmitted out of a buffer in memory automatically. Interrupts are generated when the buffer pointer wraps around at the end of the buffer, instead of after each word as in normal operation. Autobuffers of any arbitrary length are supported.

DSP56000 Serial Communication

Port C of the DSP56000 contains the processor's Serial Communication Interface (SCI) and Synchronous Serial Interface (SSI). The SCI is a full-duplex 8-bit data port. This interface uses three dedicated pins for transmit data, receive data, and serial clock. The SCI supports asynchronous bit rates and protocols or synchronous data transmission up to 2.5 Mbits/second.

The SSI is a full-duplex serial interface with programmable word length, protocol, clock, and transmit/receive synchronization. There are three modes of operation for the SSI—normal, on-demand or network. Normal mode is used for periodic data transfer, on-demand. No provision for automatic data companding is provided necessitating the use of a memory-based lookup table and additional companding software.

ADSP-2111 Host Interface Port

The ADSP-2111 Host Interface Port (HIP) is a parallel I/O port which allows the ADSP-2111 to act as a memory-mapped peripheral to a host computer. The host addresses the ADSP-2111 HIP as a section of 8-bit **or** 16-bit words of dual-ported memory. To the ADSP-2111, the HIP is a group of six memory-mapped, bi-directional data registers and two status registers. The ADSP-2111 HIP is software configurable for a variety of address, data and read/write strobe formats, allowing easy interface to most industry-standard microprocessors. ADSP-2111 HIP read or write operations can occur within a single 60 ns cycle, allowing several ADSP-2111s to operate at full speed in multiprocessor systems. The HIP is completely asynchronous with the rest of the ADSP-2111 and can be read or written to by the host with the DSP operating at full speed. ADSP-2111 HIP operation can be either interrupt driven or used through software polled operation. The HIP can also be used to load programs from a host processor into internal program memory RAM.

DSP56000 Host Interface

Port B of the DSP56000 can be configured to provide an asynchronous, double-buffered, 8-bit only Host Interface (HI). From the host processor's viewpoint, the DSP56000 HI consists of eight, 8-bit wide, consecutive memory locations for control and data transfer. Three of these locations are for data received from the DSP, three for data transmitted to the DSP. The DSP sees one 24-bit, write-only, host data transmit register; one 24-bit, read-only, host data receive register; a host control register; and a read-only host status register. The DSP56000 HI can be used with either software polled, interrupt driven, or direct memory access protocols.

Table 4 summarizes the data communication capabilities of the ADSP-2111 and the DSP56000.

MEMORY RESOURCES

The availability of on-chip memory simplifies DSP system design by reducing the overall chip count in a system.

The ADSP-2111 provides users with 2K words internal Program Memory RAM and 1K words Data Memory RAM. The modified Harvard architecture allows for data as well as code to be stored in Program Memory. Any portion of the internal program memory is available as mask-programmed ROM.

The DSP56000 has only 256 words X memory RAM and 256 words Y memory RAM internal to the device. 3.75K words of program memory ROM is also provided on chip. The DSP56001 contains the same internal X and Y memory as the DSP56000, with the addition of 512 words Program Memory RAM and optional bootstrap ROM.

SYSTEM CONSIDERATIONS

A clean external architecture, with the ability to connect easily and inexpensively to system resources, eases DSP system design and enhances processor performance.

For the ADSP-2111, the system designer has the choice of using either a clock oscillator or simple microprocessor-grade crystal. The clock or crystal used runs at a 1 x instruction cycle rate, or 16 MHz. The boot memory is typically an inexpensive, single byte-wide EPROM. The boot circuitry of the ADSP-2111 supports up to eight different 2K-word pages of boot memory. If Host Booting is disabled, the ADSP-2111 will automatically load its internal Program Memory from Page 0 of the Boot PROM. The other boot pages are accessible under software control. This feature allows the ADSP-2111 to perform up to eight completely distinct programs without any outside intervention, thereby increasing the flexibility of any ADSP-2111 design. Program modules and variables can also be defined such that data and code can be shared between boot pages.

The DSP56000 system designer also has the choice of using a clock oscillator or crystal, but the DSP56000 requires a 2 x instruction cycle rate clock (27 MHz for a 13.5 MHz instruction rate), necessitating extra care due to the presence of higher frequency signals in the system. For automatic booting into internal RAM, the DSP56001 has available, as an option,

DSP Requirement	ADSP-2111	DSP56000
Host port data registers	6 bi-directional	1 read-only 1 write-only
Host port configurable for 8- or 16-bit operation	✓	No
Serial ports	2 independent synchronous ports	1 synchronous 1 asynchronous
Built-in data companding hardware	✓	No

Table 4. Summary of Data Communication Capabilities

bootstrap code installed in internal ROM which will copy the contents of a byte-wide PROM into internal memory. The DSP56000 has no such provision. Even with the bootstrap circuitry, no boot paging scheme is supported, thereby relegating the part to a single type of functionality. Because the DSP56000 is an internal-ROM based part, quick changes or field upgrades are difficult.

DEVELOPMENT ENVIRONMENT

A complete set of easy-to-use development software and hardware is essential for system development with any DSP processor.

The ADSP-2111 is supported by a complete set of software and hardware development tools. The software development environment consists of the System Builder, Assembler, Linker, PROM Splitter, and full-featured Simulator. A C-compiler is also available. On the hardware side, Analog Devices offers the ADSP-2111 EZ-LAB™, a stand-alone hardware development board, as well as two grades of in-circuit emulators, each capable of full-speed processor emulation.

Software for the DSP56000 consists of the Macro Cross Assembler, Linker/Librarian and Simulator. The hardware development system consists of the Application Development System (ADS). While the ADS can offer emulator-like single stepping, it has no provision for full processor emulation in an arbitrary customer board.

SUMMARY

The DSPs examined in this application note take different approaches to meeting the key DSP processor requirements. The DSP56000 places its emphasis on high dynamic range MAC operations at the expense of general purpose processing flexibility. The ADSP-2111's parallel-connected arithmetic architecture, single-cycle instruction execution and flexible host port allow it to conform easily to meet algorithm requirements instead of algorithms being required to meet processor limitations.

While we're on the subject of comparison....

If the level of on-chip integration in the ADSP-2111 is not a system requirement, but high performance and low cost are priorities, then the ADSP-2105 should merit consideration.

The ADSP-2105 is a 10 MIPS processor with 1K words internal Program Memory RAM, 512 words internal Data Memory RAM and one serial port. The device is code-compatible with the ADSP-2111, as well as with all other ADSP-2100 family members (ADSP-2100A, ADSP-2101). The ADSP-2105, along with all ADSP-2100 family members, shares the same internal core architecture (arithmetic, addressing and program sequencing units) and features such as zero overhead looping and branching, circular buffering, and single-cycle instruction execution.

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Considerations for Selecting a DSP Processor (ADSP-21000 Family vs. TMS320C30)

INTRODUCTION

Digital signal processing algorithms consist of multiplications and additions. In signal processing algorithms, additions are necessary to accumulate multiplier products. Most general purpose digital signal processors sustain single instruction cycle *multiply/accumulate* throughput. A digital signal processor must also meet the following requirements to efficiently process sampled signals in real time.

- Efficient access of dual data operands to sustain single-cycle multiply/accumulate throughput
- Circular/modulo data addressing to restrict index registers to a range of data addresses
- Hardware zero overhead program looping to eliminate the overhead of branching and of decrementing loop counters from time critical loops
- Extended arithmetic dynamic range to avoid overflows when accumulating fixed-point multiplier products

Many of today's digital signal processors satisfy these requirements, some more efficiently than others. This application note compares the core architecture of the Analog Devices ADSP-21020 (Figure 1) and the ADSP-21010 to that of the TMS320C30 (Figure 2) from Texas Instruments. The **ADSP-21010** is a pin-compatible, **32-bit only, low-cost** version of the ADSP-21020. To avoid confusion, most references in this application note are made to the ADSP-21020.

The three sections that follow discuss the four requirements mentioned emphasizing the differences between the Analog Devices ADSP-21020 and Texas Instruments TMS320C30 digital signal processors. The arithmetic section discusses fixed- and floating-point data formats, parallel operation of the multiplier and ALU, and the general purpose arithmetic capabilities of each processor. The data addressing section discusses the various addressing modes of each processor

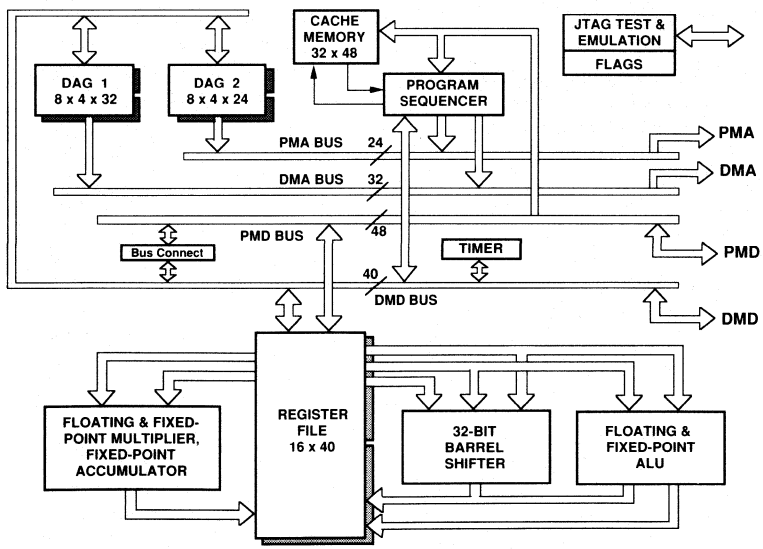

Figure 1. Analog Devices ADSP-21020

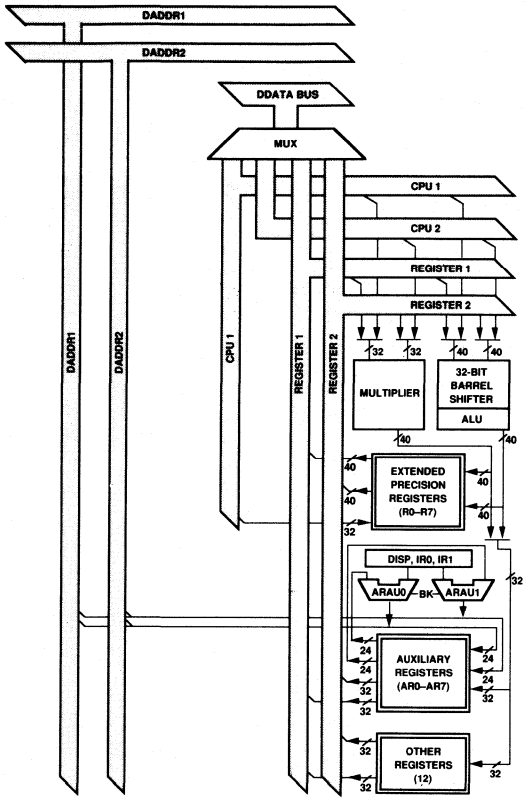

Figure 2. Texas Instruments TMS320C30 CPU

and the parallel operation of the arithmetic units with data moves. The third section discusses program sequencing including zero overhead program loops, conditional branching, and other conditional operations.

A comparison of assembly language syntax and a programming example (using the Fast Fourier Transform or FFT) are presented at the end of this application note.

ARITHMETIC CAPABILITIES

Digital signal processors must be able to multiply data operands and accumulate the products with single-cycle throughput. Some calculations require fixed-point arithmetic, others require the dynamic range of floating-point. A processor must also efficiently perform general purpose arithmetic and logical operations. Independent operation of the ALU and multiplier allowsefficient software to be written.

Data Formats

Both the ADSP-21020 and the TMS320C30 support fixed- and floating-point data formats. The ADSP-21020 supports a 32-bit and a 40-bit floating-point data format. The 32-bit floating point conforms to the IEEE 754/854 standard. This format specifies a 24-bit mantissa and an 8-bit exponent. The 40-bit format includes a 32-bit mantissa and an 8-bit exponent.

The TMS320C30 supports a 32-bit floating-point data format that specifies a 24-bit mantissa and 8-bit exponent. This format does not conform with the IEEE standard.

The TMS320C30 converts its generic floating-point format to IEEE format in 12 instruction cycles and from IEEE to TMS320C30 format in 23 instruction cycles worst case. The TMS320C30 ALU operates on 40-bit floating-point data, while the multiplier is limited to 32-bit floating-point inputs.

The ADSP-21020 multiplier and ALU operate on 32-bit fixed-point inputs as well as floating-point. The TMS320C30 multiplier only supports 24-bit fixed-point inputs while the TMS320C30 ALU operates on 32-bit fixed-point data.

The ADSP-21020 interfaces to either 32-bit or 40-bit data memory. The TMS320C30 interfaces to 32-bit data memory.

The ADSP-21020 supports two IEEE rounding modes; round-to-nearest and round-toward-zero. One of the two modes is always enabled so that both ALU and multiplier results are automatically rounded to 32-bit or 40-bit floating-point numbers. TMS320C30 results can be rounded using an instruction, RND. This instruction requires one instruction cycle to execute.

The ADSP-21020 can generate interrupts upon ALU/multiplier fixed-point overflow, floating-point overflow, floating-point underflow, or floating-point invalid operation. The TMS320C30 requires conditional branch instructions to trap on these arithmetic conditions.

Arithmetic Architecture

Figure 3 shows a block diagram of the ADSP-21020 register file and computational units. The register file is local storage for arithmetic input data and results. It consists of sixteen 40-bit registers and of eight data ports. In one instruction cycle, it can perform two memory transfers, source two inputs to the ALU, source two inputs to the multiplier, and store ALU and multiplier results. The two memory transfers can either both be reads, both writes, or one read and one write.

The register file consists of two groups of eight registers. Each register group can be swapped with a set of secondary registers in one instruction cycle. The secondary registers are typically used during interrupts or subroutines to eliminate time consuming memory transfers of register file data. Use of the 16 secondary registers provides a total of 32 register file registers.

Figure 4 shows the TMS320C30 register file and computational units. The register file consists of eight 40-bit registers.

The register file can source two inputs to the multiplier while the two ALU inputs are fetched directly from memory. Conversely, the inputs to the ALU can be sourced from the register file while the multiplier inputs are fetched directly from memory. The ALU and multiplier results are stored into the register file. The TMS320C30 register file does not have secondary registers.

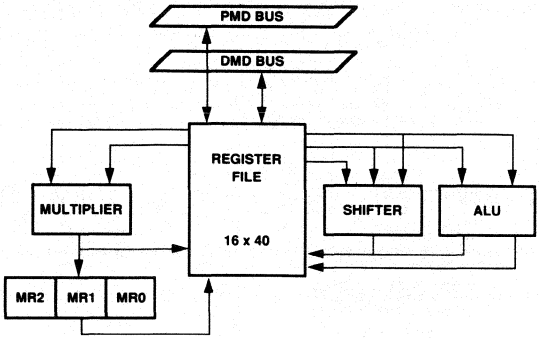

Figure 3. ADSP-21020 Register File/Computational Units

General Purpose Math

Signal processing and data compression algorithms require subtractions, division, square root, minimum/maximum comparisons, shifting, and logical operations, as well as multiply/accumulate operations. A powerful instruction set implements these functions directly. Direct implementation of such functions reduces programming errors. Single-cycle execution of such functions will result in faster execution of algorithms.

ALU

The ADSP-21020 ALU provides a complete set of logical and general arithmetic functions. The ALU operates on 32-bit fixed-point, 32-bit IEEE floating-point, or 40-bit floating-point data. In addition to performing fixed- and floating-point adds and subtracts, the ADSP-21020 ALU supports many non-traditional processor functions. All functions execute in one instruction cycle. The table below lists those functions.

INSTRUCTION	*21020*	*C30*
ABS X	x	x
–X	x	x
(X+Y)/2	x	
MIN(X,Y)	x	
MAX(X,Y)	x	
COMP(X,Y)	x	x
CLIP X BY Y	x	
X+Y,X–Y	x	
FLOAT Y	x	x
SCALE X BY Y **	x	
MANT X *	x	
LOGB X *	x	
FIX X *	x	x
FIX X BY Y **	x	
COPY X SIGN TO Y *	x	
ABS (X+Y) *	x	
ABS (X–Y) *	x	
SEED 1/X	x	
SEED 1/SQRT(X)	x	

* x and y are floating point

** x is fixed point, y is floating point

The ADSP-21020 ALU supports multiprecision fixed-point additions and subtractions preserving carry and borrow respectively. The ADSP-21020 has the ability to generate a seed for fast floating-point calculation of reciprocal and reciprocal square root. The TMS320C30 requires more instruction cycles to evaluate those expressions.

OPERATION	*21020*	*C30*
1/X	6 cycles	35 cycles
Y/X	6 cycles	36 cycles
1/SQRT(X)	9 cycles	74 cycles
SQRT(X)	10 cycles	39 cycles

The TMS320C30 ALU satisfies the basic requirements of addition, subtraction, absolute value, negate, and logic functions. The TMS320C30 however does not directly support many of the instructions available on the ADSP-21020. The ADSP-21020 maximum instruction R7=MAX(R5,R6) is coded on a TMS320C30 as:

```
LDF   R6,R7
CMPF  R5,R7
LDFLT R5,R7
```

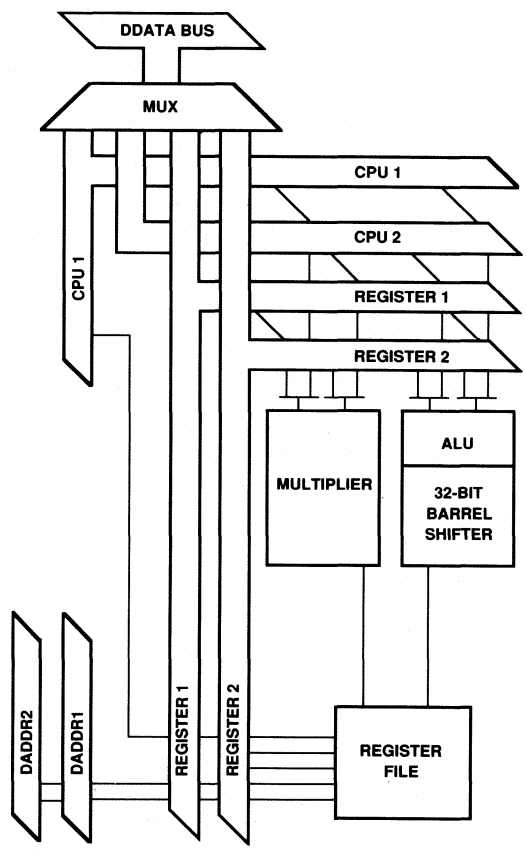

Figure 4. TMS320C30 Register File/Computational Units

ALU Summary		
FEATURE	21020	C30
40-bit floating point	x	x
32-bit fixed point	x	x
Multiprecision add/subtract	x	x
Min/max/avg/clip/scale	x	
Abs(x+y),abs(x–y)	x	
Simultaneous x+y,x–y	x	
8-bits accumulated cmp status	x	
Seed 1/x, seed 1/sqrt(x)	x	

Multiplier

The ADSP-21020 multiplier operates on 32-bit fixed-point, 32-bit floating-point, or 40-bit floating-point inputs. For 32-bit fixed-point multiplies, the upper 32 bits of the 64-bit product can be sent to a data register, or the 64-bit product can be added to or subtracted from one of two 80-bit fixed-point accumulators. Fixed-point inputs can be individually chosen as signed or unsigned, fractional or integer. Products of 32-bit or 40-bit floating-point multiplies must be sent to one of the sixteen 40-bit data registers.

The TMS320C30 multiplier operates on 24-bit fixed-point or 32-bit floating-point inputs. In the case of 24-bit fixed-point multiplication, a 48-bit product is generated. Inputs are assumed to be signed integers. Fractional fixed-point multiplication is not supported. The 32-bit ALU is used for accumulation of fixed-point products. A fixed-point product's magnitude is limited to 32 bits because only the lower 32 bits of the product are written to the destination register. Products of 32-bit floating-point multiplies are 40 bit.

Multiplier Summary		
FEATURE	21020	C30
32-bit fixed-point input	x	
Unsigned fixed-point input	x	
Fractional fixed-point input	x	
80-bit accumulators	x	
32-bit floating-point inputs	x	x
40-bit floating-point results	x	x
40-bit floating-point inputs	x	

Parallel Operation Of ALU And Multiplier

Since many DSP algorithms are modeled around a sum-of-products calculation (Figure 5), a DSP microprocessor must be able to perform multiply/addition operations efficiently. The ADSP-21020 and the TMS320C30 have the ability to multiply two operands and add (accumulate) the product from the previous multiply to a running sum simultaneously. There are other cases where code can be optimized by simultaneous operation of the ALU and multiplier. The ALU and multiplier may be performing completely independent tasks. The ADSP-21020 instruction set allows for such flexibility. The table below summarizes possible combinations of ALU and multiply operations on both the ADSP-21020 and TMS320C30.

$$y(n) = \sum_{K=0}^{M-1} a(k)\, x(n-k)$$

Figure 5. Example of Sum-of-Products Equation

OPERATION	21020	C30
Multiply/add	x	x
Multiply/subtract	x	x
Multiply/add/subtract	x	
Multiply/fixed-->float*	x	
Multiply/float-->fixed*	x	
Multiply/avg*	x	
Multiply/abs*	x	
Multiply/max*	x	
Multiply/min*	x	

* floating point only

Barrel Shifter

DSP microprocessors allow multiple bit shifting within a single instruction cycle. Bit and bit field manipulation is important for general purpose I/O functions and in graphics processing.

The ADSP-21020 instruction set includes many bit, bit field, and shift operations. The ADSP-21020 supports either left or right arithmetic, logical, and rotational shifts. The shift amount can originate from a register or can be specified in the instruction word. Shift results can be logically OR'd with other data registers. The ADSP-21020 supports bit test, bit set, bit toggle, and bit clear. The ADSP-21020 can extract arbitrary bit fields from one word and deposit the result anywhere inside another word. The ADSP-21020 can extract the exponent from a fixed-point input. It can count either leading ones or leading zeros in a fixed-point input.

The TMS320C30 supports only a subset of the ADSP-21020 shifter operations. The table below compares the instruction sets.

OPERATION	21020	C30
logical/arithmetic shift	x	x
rotate	x	x
shift/or with register	x	
bit test/clr/toggle/set	x	x*
field extract/deposit	x	
exponent extract	x	
count leading ones/zeros	x	

* requires masks stored in memory to accomplish

DATA ADDRESSING

Data addressing pertains to how data is read from memory or how data is written to memory. In order to perform multiplies each instruction cycle, new input data must also be made available at the same rate. Most DSP microprocessors satisfy this requirement of two data accesses in a single cycle. The basic addressing modes for most microprocessors are direct and register indirect addressing.

Direct Addressing

Direct addressing implies that the data address is specified directly in the instruction. The ADSP-21020 instruction, R2=DM(0x100000), loads data register R2 with the contents of address 1024K in data memory.

A 48-bit instruction word allows the ADSP-21020 to directly address the full 24-bit program memory or 32-bit data memory in one instruction cycle with one instruction opcode. Any general purpose or data register can be loaded from memory or stored into memory. The ADSP-21020 can also perform a single-cycle ALU/multiplier operation and direct memory read or write within a 64 location offset conditionally. Any of the 16 index registers can be used as base addresses for this offset.

The TMS320C30 only has a 32-bit instruction word. The TMS320C30 can only directly address data within 64K pages. The page base address is preloaded into the data page pointer (DP) register. There is only one data page pointer. The TMS320C30 can perform either an ALU or multiply instruction (but not both) with a direct memory read within a 64K page unconditionally. A direct memory write combined with a compute is not possible.

Indirect Addressing

Indirect addressing uses address generator registers as address sources. The ADSP-21020 instruction, PM(I9,M13)=R1, writes data from data register R1 into program memory. The program memory address is provided by index register I9. I9 is modified at the end of the cycle by the contents of modify register M13.

The ADSP-21020 has two data address generators (DAGs). One DAG is used to access data from data memory, the other allows data access of program memory. Each DAG (Figure 6) contains eight index registers and eight modify registers. Each index register can be used to address a different area in memory. When using indirect addressing, the programmer can pre-update or post-update the designated index register with any of the eight modify registers in the same DAG. The index register can also be modified by a 6-bit immediate offset.

The ADSP-21020 can perform a compute (multiplier + ALU), and two memory transfers (two reads, two writes, or one read and one write) in a single instruction cycle. The ADSP-21020 can perform a conditional compute (multiplier + ALU) and one memory transfer (read or write) in a single instruction cycle.

Each index register has a corresponding base address and length register. The base address and length registers allow one to confine the index register value within a range of data addresses. Each time the index register is modified, the resultant address is transparently tested by the DAG. If the resultant address is out of range, the index register is corrected with the modulo address. This feature is referred to as modulo or circular data addressing. The base and length registers allow placement of circular buffers within any range of addresses. Since the ADSP-21020 contains 16 index, base, and length registers, 16 circular buffers can be maintained simultaneously.

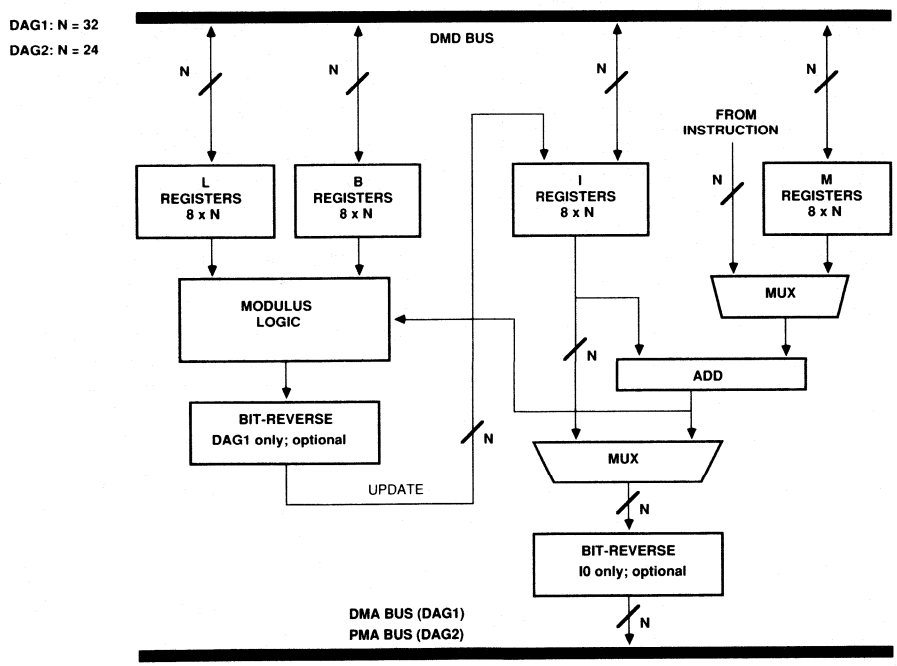

Figure 6. ADSP-21020 Data Address Generator

Each DAG's eight index, base, length, and modify registers has associated alternate registers configured in two groups of four. In the case of an interrupt or subroutine, one or both of the DAG's register groups can be swapped with secondary registers saving the overhead of register to memory transfers for a context save. The secondary DAG registers make available an additional 16 circular buffers.

The TMS320C30 also supports indexed addressing. It has eight 24-bit address registers AR7-AR0. These eight registers can be used to address different areas of memory. There are no alternate address registers. The TMS320C30 can fetch two operands from memory in a single cycle using two of the eight address registers. The address registers can be pre or post-modified by 0, 1, or one of two pre-programmed modify registers (IR1,IR0). Address registers can be modified by an 8-bit offset.

The TMS320C30 can perform a compute (multiplier + ALU) and two memory reads. It can perform a single compute (multiplier or ALU) with both one memory read and write.

The TMS320C30 supports circular buffers, but there is only one length register (BK). Therefore, if multiple circular buffers are used in one routine, they must all be the same length or the BK register must be modified for each circular data access. Circular buffers must be placed on the next power of two boundary greater than the buffer length.

Bit-Reversed Addressing

Bit- reversed addressing is necessary for proper addressing of data for the FFT. Both the ADSP-21020 and the TMS320C30 support bit-reversed addressing. Only the ADSP-21020 supports read back of bit-reversed addresses. Therefore, efficient, in-place bit-reversal is available.

Data Addressing Summary

FEATURE	*21020*	*C30*
Direct addressing (read or write)	32-bit	16-bit
Direct read, one compute	6-bit *	16-bit **
Direct read, two computes	6-bit *	n/s
Direct write, one compute	6-bit *	n/s
Direct write, two computes	6-bit *	n/s
Number of index registers	16	8
Number of modify registers	16	2
Number of length registers	16	1
Number of base address registers	16	0
Secondary index, modify, length, base registers	x	
Two indirect reads, two computes	x	x
Indirect read & write, one compute	x	x
Indirect read & write, two computes	x	
Two indirect writes, no compute	x	x
Two indirect writes, one compute	x	
Two indirect writes, two computes	x	
Compute, modify by immediate offset	6-bit	8-bit **
Bit-reversed addressing	x	x

* conditional or unconditional execution

** two operand compute only (reg1=reg1+src)

n/s not supported

PROGRAM SEQUENCING

An essential part of any microprocessor is the program sequencer. It is responsible for determining the program flow. In most cases, programs flow linearly from one address to the next sequential memory location. Branching is a form of program sequencing where the program jumps conditionally or unconditionally to another address. Subroutine calls are similar to branches, but store the pre-call address in order to return later. Interrupts also take advantage of the program sequencer. A DSP unconditionally branches to a dedicated program memory address upon interrupt. Each interrupt has a reserved memory location. Zero overhead program looping is another feature common to both the ADSP-21020 and TMS320C30.

Both the ADSP-21020 and TMS320C30 have these basic program sequencing capabilities. There are subtle differences that make programming easier and more efficient with the ADSP-21020.

Branching

Branching is necessary to change direction of program flow. Branch conditions are typically based on the arithmetic results of a bit operation, a subtraction of two inputs, or perhaps an overflow. Both the ADSP-21020 and the TMS320C30 can branch upon floating-point overflows or underflows.

The ADSP-21020 has the ability to branch on either downcounter status or on the level of any of four programmable input pins. It also has separate status bits for the ALU and multiplier. The ADSP-21020 also has complex conditional instructions where an arithmetic operation and a data move can all be executed on one condition.

Branch addresses can either be specified directly in the instruction word or can be indirectly specified through an index register. The ADSP-21020 allows a full 24-bit program address to be specified on any branch instruction. The TMS320C30 only allows full 24-bit addresses to be specified on unconditional branches. The TMS320C30 is limited to a +/– 32K (16-bit) offset from the conditional branch address.

Both the ADSP-21020 and TMS320C30 support indirect branch instructions where an index register is the address source. Using an index register allows a programmer to change a branch address during program execution. On the ADSP-21020, indirect jumps are pre-modified and execute in one instruction cycle. This is useful for implementing jump tables. The TMS320C30 does not have a pre-modified jump feature.

Pipeline Delays

When the ADSP-21020 fetches an instruction from memory, that instruction is not executed until two cycles later. The ADSP-21020 has a three-level (fetch, decode, execute) instruction pipeline. When a branch is taken, the two instructions fetched after the branch are in the pipeline waiting to be executed. When branching, the ADSP-21020 executes two NOPs instead of the two pipelined instructions. If the programmer specifies a delayed branch, the ADSP-21020 executes the two pipelined instructions. Eliminating the NOP

overhead allows the programmer to write more efficient code. The TMS320C30 has a delayed branch feature, but it has a four-level instruction pipeline. Non-delayed branches require four cycles to execute on the TMS320C30.

Subroutine Calls And Interrupts

When a subroutine call is made, the return address is stored on the program counter (PC) stack. The ADSP-21020 subroutine call is a single-cycle, single-operand instruction and is made using a direct or indirect address. Subroutine calls on the ADSP-21020 can be delayed allowing the two subsequent instructions to be executed. The TMS320C30 only supports non-delayed subroutine calls.

Interrupts

Interrupts are generated by internal or external events. Both the ADSP-21020 and the TMS320C30 have external interrupt input pins which generate interrupts upon high-low signal edges or in the presence of a low-level input. Both processors have internal timers to generate periodic software interrupts.

The ADSP-21020 responds (vectors) to an interrupt with no more than four cycles of latency. An interrupt mask register allows interrupts to be individually enabled by setting bits. There is one bit, IRPTEN, which allows masking of all interrupts. Each interrupt has eight reserved memory locations. Therefore, a delayed branch can be placed at the first interrupt vector address. There is also a five-level status stack. Anytime an interrupt occurs, arithmetic, mode, and interrupt mask status are automatically pushed onto the status stack. Status can be manually pushed onto this stack for subroutines. It is sometimes necessary that higher priority interrupts remain unmasked during lower priority interrupt routines. ADSP-21020 has a mode which allows such interrupt nesting. The ADSP-21020 has a special instruction, IDLE, which allows the processor to wait for interrupts in a low power mode. If an interrupt occurs while in IDLE, the processor stores the address of the instruction after IDLE as the interrupt return address and jumps to the interrupt vector.

The ADSP-21020 has four external interrupt input pins (IRQ3-0). It has several internally generated interrupts. An interrupt is generated any time the PC, status, or loop stacks overflow. The 32-bit internal timer can be made either a high priority or low priority interrupt. Interrupts can be generated anytime index registers I7 or I15 have modulo/circular buffer overflows. Interrupts can be generated upon fixed-point result overflow, floating-point result overflow, floating-point result underflow, or upon invalid floating-point input. The ADSP-21020 has eight user software interrupts which can be activated by setting their respective bits in the interrupt latch register (IRPTL). These are useful for creating multitasking software.

The TMS320C30 can vector to interrupts with no more than five-cycle latency. All interrupts can be masked individually or can all be masked by one master bit (GIE). Each interrupt only has one memory location. Therefore, a four-cycle, non-delayed branch to an interrupt subroutine must be placed at the interrupt vector address. Total interrupt latency is nine instruction cycles. The TMS320C30 does not have a status stack. Arithmetic and mode status must be manually saved when an interrupt occurs. An IDLE instruction is available while waiting for interrupts.

The TMS320C30 has four external interrupt input pins (INT3-0). Internal interrupts can be generated by both internal timers. The TMS320C30 can not generate interrupts upon arithmetic conditions or address register modulo overflows. The TMS320C30 has user software interrupt capability.

Subroutine And Interrupt Returns

At the end of a subroutine or an interrupt routine, program control has to be restored to the calling routine. Return instructions restore the pre-subroutine or pre-interrupt program address. The ADSP-21020 supports conditional subroutine or interrupt returns with an optional compute. Delayed branch returns allow the two instructions after the return to be executed. The TMS320C30 supports conditional subroutine or interrupt returns. It does not support delayed branch returns which incur three cycles of overhead after each return.

Zero Overhead Looping

Most digital signal processing algorithms are vector operations. Due to their repetitive nature, these vector operations are usually coded into short program loops. On most microprocessors, program loops require a branch instruction at the end of the loop for testing the loop condition. Both the ADSP-21020 and the TMS320C30 support zero overhead looping. This feature allows the end loop address and loop condition to be set up before entering the loop.

The ADSP-21020 can support six levels of nesting on zero overhead program loops. This is accomplished with a six-level loop stack. There is a six-level counter stack so that each loop can have its own 32-bit loop counter. The ADSP-21020 can ternimate a loop on loop counter status, arithmetic conditions, flag input pin states, bit test results, or unconditionally. The loop abort (LA) branch feature allows conditional branch out of a loop and automatically have the stacks, which maintain the loop, popped.

The TMS320C30 only supports one zero overhead loop. Zero overhead loop nesting is not supported. Loops can only be terminated on loop counter expired status. If the required loop condition is arithmetic, the loop requires a branch instruction and is not zero overhead. Loops are maintained by the RS (repeat start address register), RE (repeat end address register), and RC (repeat count register). If the main program is executing a zero overhead loop and an interrupt occurs, the interrupt routine must save the loop control registers (RS, RE, RC) before initializing its zero overhead loop if the interrupt routine uses zero overhead looping. The loop control registers must be restored before returning to the main program.

The two loop setup instructions, RPTS (repeat single) or RPTB (repeat block), flush the instruction pipeline and incur four instruction cycles of overhead on the first pass through the loop. RPTS is not interruptable. RPTB is interruptable. The TMS320C30 does not have a loop abort branch feature. If a loop must be aborted, the RC register must be loaded with zero after the branch is taken.

Cache Memory

Both the ADSP-21020 and TMS320C30 have on-chip instruction cache memories to minimize bottlenecks caused when both instructions and data must be accessed from the same external memory space.

The ADSP-21020 has a 32-word instruction cache. The cache is two-way, set associative. It only stores instructions which cause a bus conflict. Put another way, the ADSP-21020 cache memory only stores the last 32 instructions which require program memory data access. In the case of loops which contain more than 32 program memory data accesses, the cache can be frozen. The cache can be disabled allowing use of a logic analyzer to trace all instructions executed.

The TMS320C30 has a 64-word instruction cache. This cache stores all of the past 64 instructions fetched externally no matter if they cause a bus conflict or not. For loops of length greater than 64 instructions, the TMS320C30 cache can be frozen. In the case of the ADSP-21020, loops greater than 64 instructions can exist without bus conflict as long as no more than 32 of the instructions cause a bus conflict. The TMS320C30 can freeze, disable, or clear its cache memory.

Program Sequencing Summary

FEATURE	*21020*	*C30*
Single-cycle/operand branching with 24-bit address	x	x
Pre-modified indirect branching	x	
Conditional branch/subroutine cal with compute	x	
Instruction pipeline levels	3	4
Delayed branch	x	x
Delayed branch subroutine calls	x	
Memory locations at interrupt vector	8	1
Interrupts on index/address register modulo overflow	x	
Interrupts on arithmetic status	x	
Delayed branch returns	x	
Zero overhead loop nesting levels	6	1
Conditional branch with loop abort	x	
Status stack	x	
Instruction cache	x	x

EXTERNAL MEMORY

The ADSP-21020 efficiently interfaces to a large amount of external program and data memory. Any access, whether it be a read or a write, completes in a single cycle unless the programmer explicitly declares wait state values.

The access time requirements of external memory for the ADSP-21020 are not as stringent as those for the TMS320C30. An ADSP-21020 with a cycle time of 50 ns requires a memory access time of 35 ns.

The TMS320C30 is not as efficient with external memory accesses. A write to external memory always takes two cycles and in certain cases a read from external memory takes two cycles.

ASSEMBLY LANGUAGE

For more efficient operation, digital signal processors can be programmed in assembly language. Assembly language syntax usually takes the form of two, three, or four letter mnemonics followed by a register or immediate data field. The following is an example of a TMS320C30 assembly language instruction:

```
SUBI3 R7,R2,R0
```

Translated, this instruction performs an integer subtraction of R0 = R2 – R7 where R0, R2, and R7 are internal data registers. The ADSP-21020 has a much simpler, algebraic assembly language syntax. The same instruction programmed on the ADSP-21020 is:

```
R0 = R2 - R7;
```

If one programmer is trying to decipher another's code, the ADSP-21020 assembly language syntax is easier to understand.

The following comparison illustrates how easy it is to use the ADSP-21020 assembly language.

FUNCTION	*ADSP-21020*	*TMS320C30*
store reg direct	`DM(0x98A1)=R2;`	`STF R2,@98A1h`
load reg indirect	`R3=DM(I4,M1);`	`LDF *AR4++(IR1),R3`
parallel mult/add + data move	`R12=R2*R4, R8=R8+R12, R2=DM(I3,M1), R4=PM(I12,M8);`	`MPYF3 R7,R4,R0 || ADDF3 *-AR3,*AR5-(1),R3`

An example of zero overhead program loop initialization is another case of the ADSP-21020 assembly language's legibility.

```
LCNTR=99, DO fir_lup UNTIL LCE;
```

Here is an example of zero overhead loop initialization on the TMS320C30.

```
LDI  99, RC
RPTS fir_lup
```

BENCHMARKS

All digital signal processors have the ability to execute FIR filters at one instruction cycle per filter tap. Algorithms which require general purpose features and instructions intended for DSP algorithms can be used to demonstrate the differences between one processor and another. One example is the Fast Fourier Transform (FFT). The table below compares a 1024-point complex, radix-2 FFT on the ADSP-21020, ADSP-21010 and TMS320C30.

ADSP-21020 (40 ns)	*ADSP-21010 (80 ns)*	*TMS320C30 (50 ns)*
21314 cycles 0.852 ms	21314 cycles 1.705 ms	50660 cycles 2.533 ms

The ADSP-21020's FFT core loop (FFT butterfly) executes in four instruction cycles, while the TMS320C30's executes in nine. The ADSP-21020's assembly syntax is also more legible.

ADSP-21020 Radix-2 Complex FFT Butterfly (4 instructions)

```
R8=R1*R6,  R14=R11-R14,
             DM(I2,M0)=R10, R9=PM(I11,M8);
R11=R1*R7, R3=R9+R14, R9=R9-R14,
             DM(I2,M0)=R13, R7=PM(I8,M8);
R14=R0*R6, R12=R8+R12,
             R8=DM(I0,M0), PM(I10,M10)=R9;
R12=R0*R7, R13=R8+R12, R10=R8-R12,
             R6=DM(I0,M0), PM(I10,M10)=R3;
```

TMS320C30 Radix-2 Complex FFT Butterfly (9 instructions)

```
   subf  *ar2,*ar0,r2
   subf  *+ar2,*+ar0,r1
   mpy   r2,r6,r5
|| addf  *+ar2,*+ar0,r3
   mpyf  r1,*+ar4(IR1),R3
|| stf   r3,*+ar0
   subf  r0,r3,r4
   mpyf  r1,r6,r0
|| subf  *ar2,*ar0,r3
   mpyf  r2,*+ar4(IR1),r3
|| stf   r3,*ar0++(IR0)
   addf  r0,r3,r5
   stf   r5,*ar2++(IR0)
|| stf   r4,*+ar2
```

The key to the ADSP-21020's efficiency lies in its ability to simultaneously generate the sum and difference of the same two inputs, perform a multiply, store one number in memory, and fetch another from memory all in a single cycle. The TMS320C30 can not store data to memory while performing both a multiply and an add. The TMS320C30 can not simultaneously add and subtract the same two inputs.

SUMMARY

Digital signal processors must meet three basic requirements:

1. Perform multiply/accumulate operations at a single-cycle throughput rate
2. Maintain circular data buffers
3. Maintain loops with zero overhead

Floating-point digital signal processors such as the ADSP-21020 and TMS320C30 meet those requirements differently. As these products evolve, the core architectures will remain the same in order to retain upward compatibility. Therefore, the advantages and disadvantages mentioned above should be carefully analyzed.

This application note can not cover all topics in detail. Consult the *ADSP-21020 User's Manual*, *ADSP-21020 Development Software Manual*, ADSP-21020 data sheet, and ADSP-21010 data sheet for more detailed information.

Analog Devices' DSP bulletin board system (BBS) is available to the public for benchmarks, application notes and general product information.

Analog Devices Bulletin Board System
8 Data Bits, 1 Stop Bit, No Parity
300/1200/2400 Baud
(617)461-4258—On-Line 24 Hours

REFERENCES

Analog Devices, Inc., *ADSP-21020 User's Manual*, 1991.

Texas Instruments, Inc., *Third-Generation TMS320 User's Guide*, 1988.

Papamichalis, P., Simar, R., "The TMS320C30 Floating-Point Digital Signal Processor" in: *Digital Signal Processing Applications with the TMS320 Family, Volume 3*, Texas Instruments, Inc., 1990. Reprinted from IEEE Micro Magazine: Vol. 8, No. 6, December 1988.

ANALOG DEVICES

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Considerations for Selecting a DSP Processor (ADSP-2105 vs. TMS320C25)

INTRODUCTION

Digital signal processing systems demand high performance. But high performance cannot be measured by a processor's clock speed or multiplication/accumulation speed alone. What distinguishes DSPs from other types of microprocessor and microcontroller architectures is how well they perform in each of the following areas.

1. Fast and flexible arithmetic
   A DSP processor must provide single-cycle computation for multiplication, multiplication with accumulation, arbitrary amounts of shifting, and standard arithmetic and logical operations. In addition, the arithmetic units should allow for any sequence of computation so that a given DSP algorithm can be executed without being reformulated.
2. Extended dynamic range on multiplication/accumulation
   Extended sums-of-products are common in DSP algorithms. Protection against overflow in successive accumulations ensures that no loss of data or range occurs.
3. Single-cycle fetch of two operands
   Again, in extended sums-of-products calculations, two operands are always needed to feed the calculation. A processor must be able to sustain two operand data throughput.
4. Hardware circular buffering (both on- and off-chip)
   A large class of DSP algorithms, including most filters, require circular buffers. Hardware to handle address pointer wraparound reduces overhead increasing performance) and simplifies implementation.
5. Zero overhead looping and branching
   DSP algorithms are naturally repetitive and can easily be expressed as loops. Program sequencing that supports looped code with zero overhead provides the best performance and the easiest programming implementation. Likewise, overhead penalties for conditional program flow are unacceptable in signal processing applications.

Not all processors currently used for DSP and DSP-like functions meet these architectural and performance requirements equally well. This article examines these considerations for selecting a DSP processor, comparing two leading 16-bit fixed-point processors, the ADSP-2105 from Analog Devices and the TMS320C25 from Texas Instruments.

The three sections that follow discuss the five points above. The arithmetic section discusses items one and two, the addressing capabilities sections discusses items three and four and the program sequencing section discusses item five.

Program examples and benchmarks can be found at the end of this article.

ARITHMETIC CAPABILITIES

The basis of a successful DSP implementation is the ability to perform fast math. Arithmetic capabilities are the foundation of DSP performance.

General Purpose Math

One indicator of a good arithmetic architecture is the ability to perform a wide range of arithmetic computations. These computations should be handled in a flexible manner so that the algorithm can be implemented without rearranging the order of the arithmetic operations or operands. If the arithmetic architecture is fixed, too special-purpose or limited and the algorithm must be rearranged, this poses extra work for the DSP designer or programmer and delays getting a system running. Algorithm development frequently turns out to be much of the work of implementing a DSP system. If an algorithm can be used "as is" with no extra work, the design can be finished sooner and with less chance of error.

Arithmetic Architecture

Figure 1 shows a block diagram of the arithmetic section of the ADSP-2105, while Figure 2 shows that of the TMS320C25. Both of these devices utilize a modified

Harvard architecture which can feed data operands from both program memory and data memory to the arithmetic section. Both of these devices work with 16-bit numbers.

The ADSP-2105 has three independent computational units: an ALU, multiplier/accumulator (MAC), and a barrel shifter. They are connected (via the R bus) so that the output of any unit may be used as the input for itself or any other unit on the next cycle. The ALU and MAC are directly connected to both the program and data memory buses. Operands for ALU and MAC operations can come from both memories or any combination of off-chip memory and other data registers in the processor.

The TMS320C25 contains a multiplier, an ALU, a 16-bit scaling shifter and additional shifters at the outputs of both the accumulator and multiplier. The multiplier has an input register and an output register. The multiplier has direct connection to both the program and data bus while the ALU connects only to the data bus (through the shifter) and to the output of the multiplier. Results are always sent to either the data bus or the accumulator registers. In some cases, the result must first be stored back in data memory before it can be used as an input to another calculation.

ADSP-2105 ALU

The ALU has two X and two Y input registers: AX0, AX1, and AY0, AY1. ALU operations are performed on any X-Y assortment of these input registers. They may be loaded from any combination of program and data memory or other data registers in the processor. The result of the operation appears in the ALU result (AR) or ALU feedback (AF) register. AR and AF can also be used as the X and Y operands (respectively) in any calculation. In addition, the result registers of the MAC and barrel shifter can also be used directly as X inputs to the ALU (and vice versa).

ALU instructions are coded in a register transfer, algebraic syntax. An example of addition is shown below. This example is a multifunction instruction. The first "clause" of the instruction (up to the first comma) is the addition operation. The second clause loads the X input register from data memory (DM) and the third clause loads the Y input from program memory. An addition (or any other ALU operation) can be executed on a sustained, single-cycle basis. (These operand fetching clauses of the instruction may be omitted, if they are not needed.)

```
AR = AX0 + AY1, AX0=DM (I0,M0), AY1=P(I4, M4)
```

All ALU operations complete in single 72.3 ns cycle. (All references to cycles for the ADSP-2105 assume a 13.824 MHz device.) The ADSP-2105 runs at full speed even with off-chip memory access.

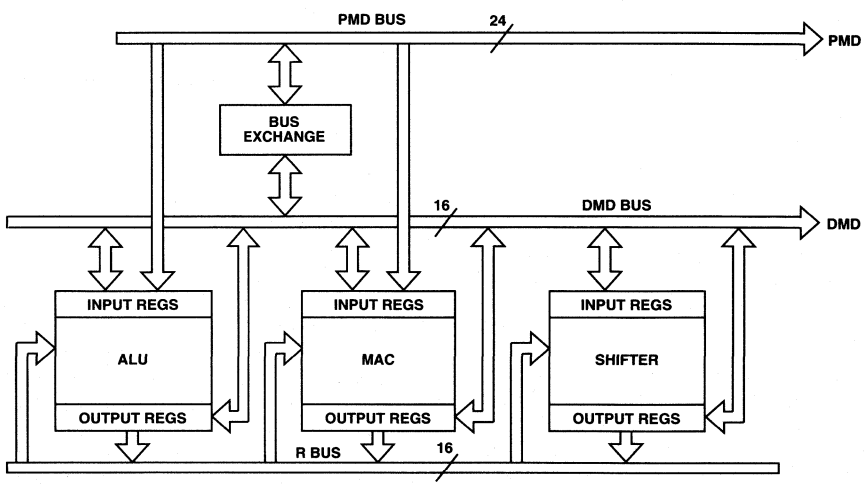

Figure 1. ADSP-2105 Arithmetic Section

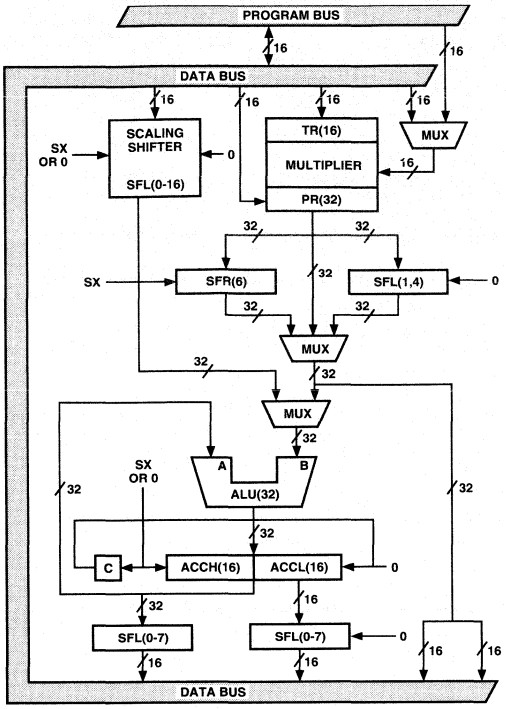

Figure 2. TMS320C25 Arithmetic Section

TMS320C25 ALU

ALU operations require that one operand must come from the accumulator while the other comes from either the multiplier output or from the data bus through a shifter. To add two numbers, the accumulator must be loaded with the first data value. After the accumulator is loaded, a second number can be added to the accumulator. The instructions for the ALU are specified with a mnemonic. The two instructions required to add two numbers are shown below.

```
ZALH   <Data memory address>
ADDH   <Data memory address>
```

For the result to be used as an input value for anything other than another ALU operation, the data must first be stored back into data memory from the accumulator. Not all ALU operations can be performed in a single 80 ns cycle; an add as shown above can be accomplished every two cycles. (All references to TMS320C25 cycles assume a 50 MHz device with an 80 ns cycle time.) Not all ALU instructions can be used with the repeat feature. There is a speed penalty for use off chip data memory; depending upon the memory configuration, some ALU operations can take as many as four cycles.

ADSP-2105 MAC

As shown in Figure 1, the ADSP-2105 multiplier/accumulator (MAC) sits next to the ALU. Like the ALU it has two X and two Y input registers, MX0, MX1 and MY0, MY1. The unit performs both multiplications and MACs independent of the ALU. This is a key difference from the architecture of the TMS320C25.

MAC operations are performed on any X-Y assortment of input registers. They may be loaded from any combination of program and data memory or other data registers in the processor. The result of the operation appears in the MAC result register (MR) or the MAC feedback register (MF). Like the ALU, the feedback and result registers can also serve as the X and Y operands for any multiplication or MAC operation. The result registers of the barrel shifter and ALU can also be, used directly as X inputs to the MAC (and vice versa).

The instructions for the MAC are specified in a register transfer, algebraic syntax. An example is shown below. The first line shows multiplication of two signed operands and the second example shows multiplication with accumulation of one signed and one unsigned operand. (Signed and unsigned operands can be mixed in any combination.)

The second example is a multifunction instruction. The first "clause" of the instruction (up to the first comma) is the MAC operation. The second clause loads the X input register from data memory (DM) and the third clause loads the Y input from program memory. Any MAC operation can be executed on a sustained, single-cycle basis. (These operand fetching clauses of the instruction may be omitted, if they are not needed, as in the first example.)

```
MR=MX0*MY0(SS)
MR=MR+MX1*MY1 (SU), MX1=DM(I0,M0),MY1=PM(I4,M4)
```

The MR (MAC result) register is actually a 40-bit accumulator. For 16-bit calculations it is divided into two 16-bit pieces (MR0 and MR1) and an 8-bit overflow register (MR2). DSP applications frequently deal with numbers over a large dynamic range. The eight "overflow" bits of MR2 allow for 256 MAC overflows before a loss of data can occur.

All multiplication and MAC operations execute in a single 72.3 ns cycle. Two new operands can be loaded into the input registers in parallel with the computation so that a new MAC operation with new operands can be started every cycle. The ADSP-2105 runs at full speed even with off-chip memory access.

TMS320C25 MAC Operation

There is no dedicated multiplier/accumulator hardware in the TMS320C25. The TMS320C25 requires the use of both the multiplier and the ALU to perform a complete multiplication/accumulation operation. A multiplication is performed by loading the T register with the first operand. Once this data is loaded, a value from the data bus

can be multiplied with the value in the T register. The instructions for the multiplier are specified with a mnemonic. The instructions for a multiplication are shown below.

```
LT <data memory address>
MPY <data memory address>
```

A product is obtained every two cycles.

A full multiplication accumulation requires the use of the ALU as well as the multiplier. The instruction required to perform a MAC operation is shown below. This instruction requires two words of program memory storage.

```
MAC <prog. mem. address> <data mem. address>
```

With both operands in on-chip memory, the MAC instruction takes three 80 ns cycles in nonrepeat mode. In repeat mode, it will require $2 + n$ cycles, where n is the number of repeats.

The TMS320C25 provides one bit of extension in the accumulator (a 33-bit accumulator compared to the 40-bit accumulator of the ADSP-2105). After more than one overflow, the calculation is corrupted.

ADSP-2105 Shifter

The barrel shifter in the ADSP-2105 has an input register, SI, and accepts as inputs any result registers in the processor (e.g., MR1, AR) including its own result register, SR. Like the MAC result register set, the 32-bit SR is divided into two 16-bit registers, SR0 and SR1. The shifter also has an exponent register, SE, which is set automatically by the exponent adjust instructions and used for normalization instructions.

The shifter can place a 16-bit input value anywhere within a 32-bit field in a single cycle. The input can be shifted any number of bits from off-scale left to off-scale right. Other functions such as exponent detection, normalization, denormalization, block floating point exponent maintenance, and pattern merging can also be performed with this shifter. All shifter operations are performed in a single cycle. Numbers can be normalized, regardless of the number of bits to be shifted, in a single cycle.

TMS320C25 Shifter

The TMS320C25 scaling shifter shifts to the left from 0 to 16 bits. Two other shifters can shift data coming from the multiplier left 1 bit or 4 bits, or right 6 bits, or can shift data coming from the accumulator left from 0 to 7 bits. These two shifters add the advantage of being able to scale data during the data move instead of requiring an additional shifter operation.

Table I. Arithmetic Capabilities

DSP Requirement	ADSP-2105	TMS320C25
Single-Cycle ALU Operations	✓	No
Single-Cycle Multiplication	✓	No
Single-Cycle MAC Operations	✓	✓*
Single-Cycle Shifting	0–32 Bits	0–16 Bits Left or Left or Right 0–7 Bits Left or 1 or 4 Bits Left or 6 Bits Right
Accumulator Overflow Protection	8 Bits	1 Bit
Signed, Unsigned or Mixed-Mode Multiplications	✓	No Mixed Mode

*Approaches single-cycle efficiency when using repeat mode.

Arithmetic Summary

Table I summarizes the comparison of arithmetic capabilities of these processors.

The side-by-side architecture of the ADSP-2105 results in easier implementation of many DSP algorithms as compared to the fixed sequence, end-to-end architecture of the TMS320C25. Due to the dependency of the ALU on the multiplier for multiplication/accumulations in the TMS320C25, MAC operations can not be easily intermingled with ALU operations. This may require changing the order of calculations in an algorithm so that the interdependency of ALU and multiplier does not cause a problem. The local storage registers found in the ADSP-2105 make data movement for calculations easy. If data is to be used many times, it can reside in a register to eliminate the need of fetching it from memory each time. With local registers and the open architecture, it is easy to perform arithmetic operations in any order and to guarantee that input operands and results remain intact until explicitly overwritten or moved.

DATA ADDRESSING

A digital signal processor's ability to perform fast arithmetic is wasted if the required data cannot be fetched at an equal and sustained speed. Addressing hardware must support the dual operand fetches required to fully utilize the Harvard architecture found in most DSPs. Circular buffers are frequently found in DSP algorithms; hardware support of address pointer wraparound is another feature distinguishing a signal processor from other types of high-performance processors.

Figure 3 shows the address generation circuitry of the ADSP-2105 while Figure 4 shows that of the TMS320C25.

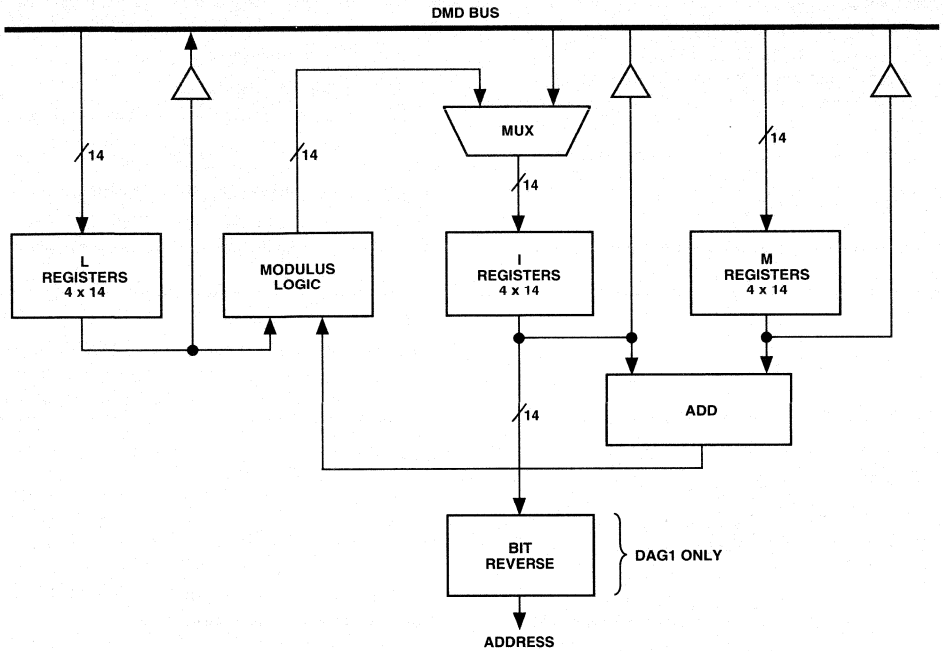

Figure 3. ADSP-2105 Address Generation Logic

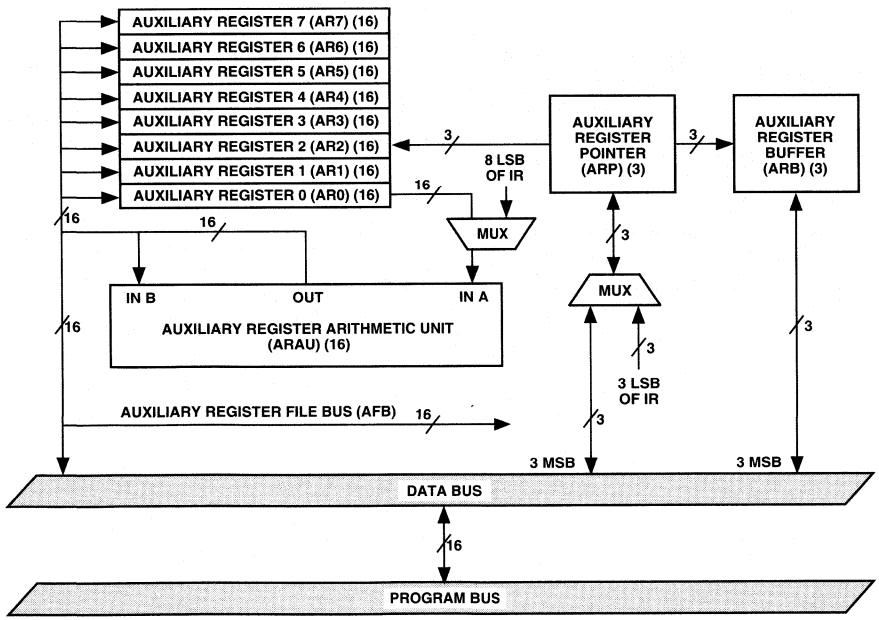

Figure 4. TMS320C25 Address Generation Logic

ADSP-2105 Addressing
There are two independent address generators in the ADSP-2105. One typically supplies addresses for program memory data fetches while the other handles data memory, making efficient use of the modified Harvard architecture. Each address generator has four I registers which store pointers (addresses), four M registers for address modifiers, and four L registers storing buffer lengths for modulo addressing of circular buffers.

The address generator can bit-reverse an address as it is sent out to the address bus for zero-overhead bit-reversing for the FFT. The I, M, and L registers can be also used for general purpose data storage.

ADSP-2105 Indirect Addressing
With indirect addressing, the address in an I register drives either the data or program memory address bus. While the memory is being accessed, the address is simultaneously updated with the contents of any of the modify (M) registers, as shown in Figure 5. The specific pairing of I and M registers is up to the programmer. For example, I0 and M3 could be specified in the instruction as in

```
AX0 = DM(I0,M3)     {load AX0 from Data Memory}
```

The ability to mix I registers and M registers is especially useful for two-dimensional addressing or for supporting pointer increment and decrement without constantly reloading a new modify value. This instruction syntax shows explicitly what registers are used to generate the address and where the data is going; nothing has to be inferred.

Loading the length of a circular buffer into the L register activates the modulus logic, guaranteeing that the address is kept inside the buffer in a modulo fashion. This is maintained automatically by the address generator hardware and does not have to be calculated explicitly by the programmer. Circular buffers, such as for the delay lines of digital filters, are both transparent and require zero-overhead.

ADSP-2105 Direct Addressing
Due to the 24-bit width of the ADSP-2105 instruction, a full 14-bit address can be specified within a (single-word) instruction for single-cycle access to any data. Figure 6 illustrates this. Below is an example of an instruction using direct addressing to read from data memory.

```
MX0 = DM (some_label)
```

TMS302C25 Addressing
The auxiliary register file of the TMS320C25 is used for storage of addresses and a single modifier. Only one address can be supplied at a time with the auxiliary register file so that two data fetches cannot be achieved.

TMS320C25 Indirect Addressing
The auxiliary register file is connected to an arithmetic unit which will auto-index the contents of the auxiliary register or modify a register by the contents of auxiliary register number 0. The TMS320C25 has a single modify register. This limits the addressing capabilities for indirect addressing. No support is provided for circular modulo addressing; it must be calculated by the programmer as part of the computational load of the program. This diminishes the performance of DSP algorithms using circular buffers.

Also, the only way to read coefficients from program memory using indirect addressing is to use table reads.

TMS320C25 Direct Addressing
The TMS320C25 can directly access data within a 128-word block (compared to a 16K word block with the ADSP-2105). A data page register is used in conjunction with the direct address to access a larger data space. To

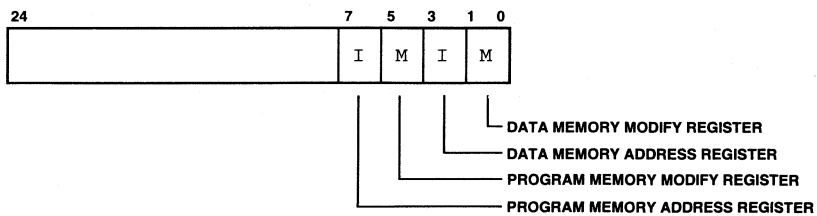

Figure 5. Indirect Addressing In ADSP-2105

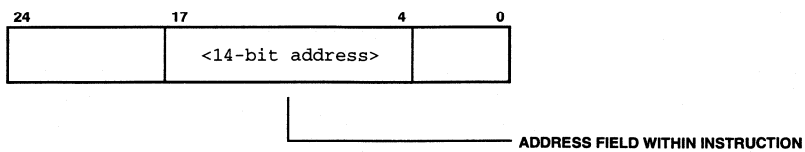

Figure 6. ADSP-2105 Direct Addressing

access data within a different block requires software overhead to update the 9-bit data page register. The update of the page register poses the requirement on the programmer to detect when the page boundary has been exceeded and when it is necessary update the page register.

TMS320C25 Addressing Instructions

The instruction mnemonics of the TMS320C25 involve several addressing modes. Since the number of registers are limited there is not a set of specific instructions to load registers from memory as with the ADSP-2105. Indirect and direct addressing is specified within arithmetic instructions and, depending upon the memory configuration, can impose several overhead cycles (overhead can be as high as eight cycles with external memory). Some general syntax example are shown below.

```
ADDH   {*|*+|*-|*0+|*0-|*BRO+|*BRO-}  [,>next ARP>]
MPY    {*|*+|*-|*0+|*0-|*BRO+|*BRO-}  [,<next ARP>]
```

Specific examples of these are shown below:

```
ADDH   *
MPY    *0+
```

The first example uses the contents of an auxiliary register as the address and the second uses the contents of an auxiliary register as the address and adds the contents of auxiliary register 0 as a modifier. This instruction syntax can be hard to decipher because it does not directly name which auxiliary register is being used. That information is stored in the auxiliary register pointer (ARP).

The address generator can bit-reverse an address as it is sent out to the address bus for zero-overhead bit-reversing for the FFT. Auxiliary registers can also be used for general purpose data storage and the Auxiliary ALU can be used for limited math.

ADDRESS GENERATION SUMMARY

Sustaining high rates of arithmetic operations demands maximum performance from the data addressing part of a processor's architecture. Table II summarizes the differences between the two processors in terms of their data addressing capabilities.

PROGRAM SEQUENCING

Efficient architectures for signal processing require fast arithmetic capabilities and matching speed in data addressing and fetching capabilities. To fully deliver the performance required for real-world signal processing, a DSP machine must execute its program with little or no overhead spent on maintaining the proper flow of control.

Efficiency in program sequencing has many different aspects; they cannot all be covered in this article. The comparison focuses primarily on two features:

- the execution of loops and
- how branching and branching on conditions are handled

Loops are fundamental to the way DSP algorithms are expressed in their natural mathematical form. Operations such as sums-of-products are repetitive. If the program can be efficiently expressed in a looped form then coding is quite straightforward and changing the program (for example, to increase the number of taps in a filter) requires very little work.

Branching is fundamental to program structure. Branching on conditions (and executing arithmetic on conditions) is a natural way to construct any program which must respond to its environment.

Program Sequencer Architecture

Figure 7 shows the architecture of the program sequencer of the ADSP-2105, and Figure 8 shows that of the TMS320C25.

ADSP-2105 Program Sequencer

The program sequencer of the ADSP-2105 contains logic that selects a program memory address source and routes the address to the program memory address bus (PMA). This address selection occurs automatically in

Table II. Data Addressing Capabilities

DSP Requirement	ADSP-2105	TMS320C25
Single-Cycle Fetch of Two Operands from On-Chip	✓	✓*
Generate New Program Memory and Data Memory Addresses Each Cycle	✓	✓**
Modify Two Addresses by Two Different Modify Values on Every Cycle	✓	No
Bit-Reverse Data Memory Addresses for FFT	✓	✓
Automatic Pointer Wraparound for Circular Buffers	✓	No

*MAC & MACD instructions only
**Direct addressing mode only and only with MAC and MACD instructions

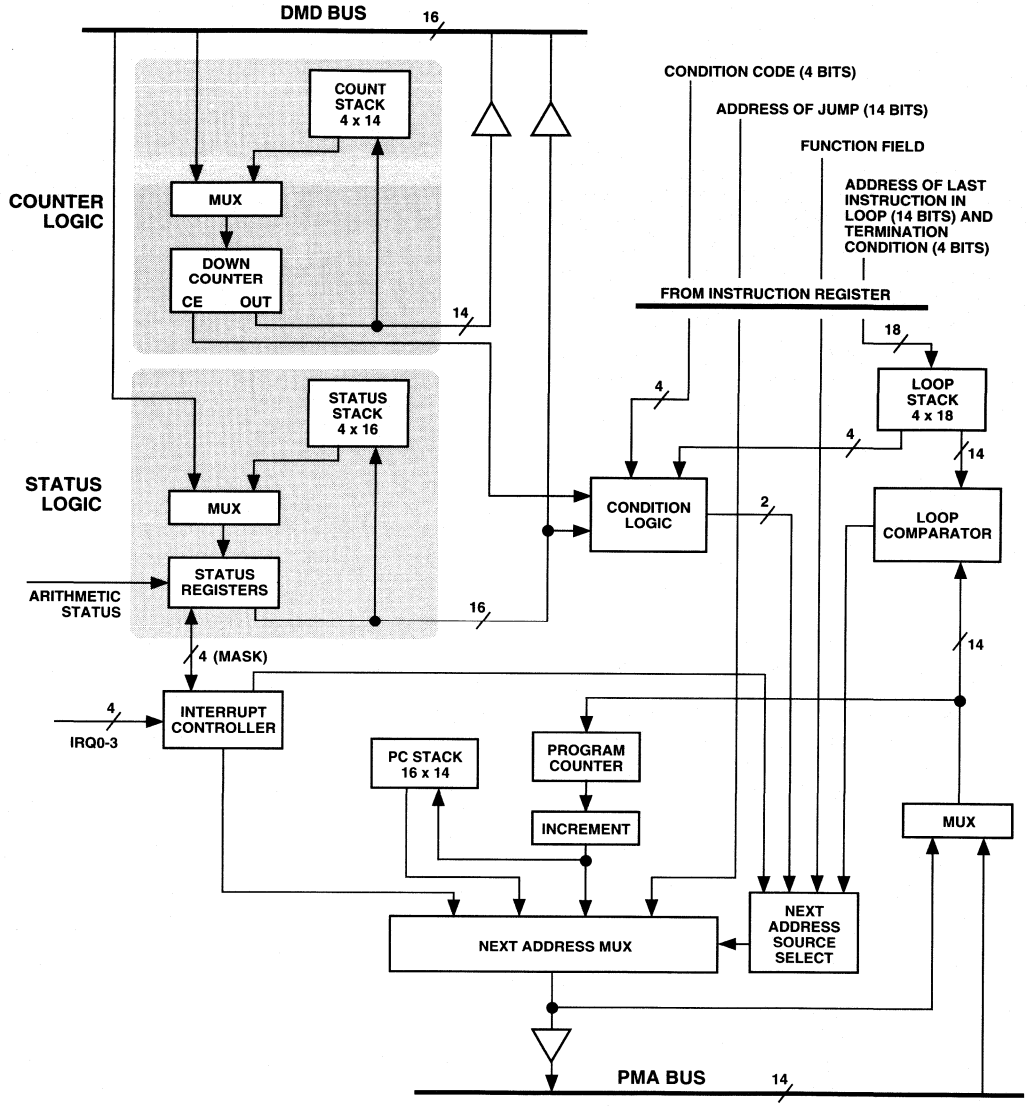

Figure 7. ADSP-2105 Program Sequencer Architecture

response to the current instruction. The address placed on the address bus can come from

- the program counter (for sequential addressing)
- a 14-bit address in the instruction word itself, for direct jumps and subroutine calls
- the PC stack, for returns from subroutines and interrupts
- the interrupt logic, to automatically vector to the interrupt routine upon assertion of any external interrupt

All instructions execute in a single cycle; this applies equally to jumps, calls and interrupts. No instruction pipelining is required in the ADSP-2105 so that program flow is simple to understand.

When an interrupt occurs, the complete status of the processor (stack status, mode status, arithmetic status and interrupt mask) is automatically pushed onto the status stack as part of the interrupt vector process.

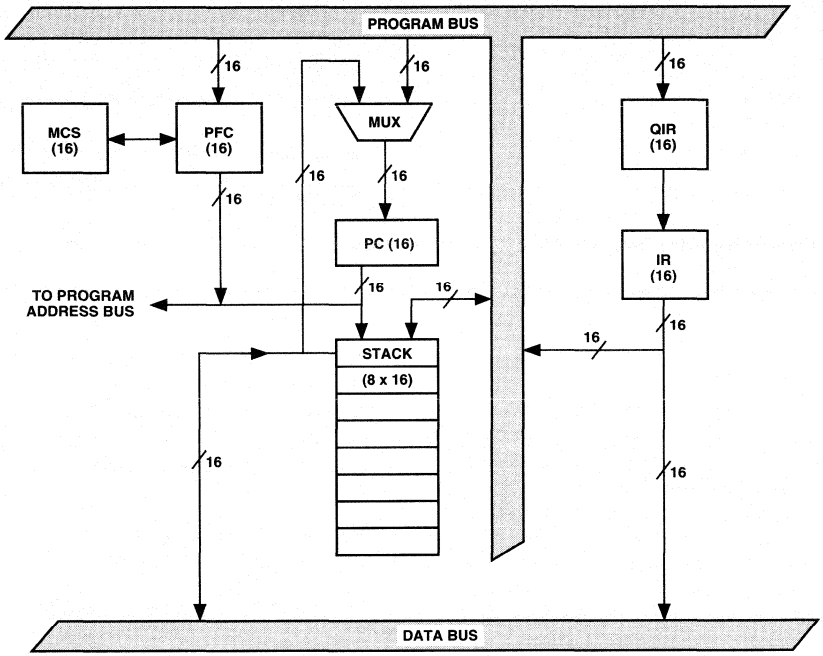

Figure 8. TMS320C25 Program Sequencer Architecture

ADSP-2105 Looping Capabilities

The ADSP-2105 program sequencer supports zero overhead "DO UNTIL" loops. Using the count stack, loop stack and loop comparator, the processor can determine whether a loop should terminate and can supply the address of the next instruction (either the top of the loop or the instruction after the loop) with no overhead cycles.

A DO UNTIL loop may be as large as program memory size permits. A loop may terminate when a 16-bit counter expires or when any arithmetic condition occurs. The example below shows a three instruction loop that is to be repeated 100 times.

```
        CNTR = 100
        DO Label UNTIL CE

              First instruction of loop
              Second instruction of loop
Label:        Last instruction of loop
        First instruction outside loop
```

The first instruction loads the counter with 100. The DO UNTIL instruction contains the address of the last instruction in the loop (in this case the address represented by the identifier, *Label*) and also contains the termination condition (in this case the count expiring, CE). The execution of the DO UNTIL instruction causes the address of the first instruction of the loop to be pushed on the PC stack and the address of the last instruction of the loop to be pushed on the loop stack (see Figure 7).

As instruction addresses are output to the program memory address bus and the instruction is fetched, the loop comparator checks to see if the instruction is the last instruction of the loop. If it is, the program sequencer checks the status and condition logic to see if the termination condition is satisfied. The program sequencer then either takes the address from the PC stack (to go back to the top of the loop) or simply increments the PC (to go to the first instruction outside the loop).

The looping mechanism of the ADSP-2105 is automatic and transparent to the user. As long as the DO UNTIL instruction is specified, all stack and counter maintenance and program flow is handled by the sequencer logic with no overhead. This means that in one cycle the last instruction of the loop is being executed, and in the very next cycle, the first instruction of the loop is executed or the first instruction outside the loop is executed, depending upon whether the loop terminated or not.

ADSP-2105 Program Sequencer Instructions

There are many conditional instructions for the ADSP-2105. Most arithmetic instructions as well as jumps, subroutine calls, returns from interrupts and returns from subroutines may all be conditional. The program sequencer decides whether the condition is true and what action to take, requiring zero overhead cycles. The

coding of conditional jumps, subroutine calls and returns is straightforward. Some examples of the syntax are shown below.

```
IF condition JUMP label
IF condition JUMP I4
IF condition CALL label
IF condition CALL I4
IF condition RTS
```

In the above examples, I4 references an address generator register for indirect branching. *Condition* refers to any of a set of sixteen arithmetic conditions in the processor and *label* refers to any address or label in the program memory space.

TMS320C25 Program Sequencer

The program sequencer logic of the TMS320C25 controls instruction execution and consists of a program counter and related hardware. Instruction execution for the TMS320C25 utilizes a three-level pipeline consisting of a prefetch, decode, and execution stage. A prefetch counter (PFC) contains the address of the next instruction to be prefetched. The prefetched instruction is loaded into the instruction register (IR), unless the instruction register still contains an instruction currently executing. In this case the prefetched instruction is temporarily stored in the queue instruction register (QIR). The instruction pipeline (which can be either two levels or three levels depending upon the memory configuration) in conjunction with multicycle instruction execution can make program flow complex and difficult to understand. Calculating a benchmark for a particular algorithm can also become difficult for the same reason.

The program counter can supply an address for sequential addressing. The single 8-deep PC stack is used for storage of return addresses as well as for providing the ability to push and pop data for the accumulator. An interrupt flag register (IFR) is used for the vectoring to an interrupt routine. Unlike the ADSP-2105, status is not automatically saved on the TMS320C25 for interrupts so that the programmer must perform any save and restore functions explicitly. Logic is included to repeat an instruction as many as 256 times.

Branch instructions which contain a direct address require multiple program memory locations because both the instruction bits and the address can not fit in the 16-bit instruction width.

Instruction Pipelining in the TMS320C25

Anytime the flow of the program deviates from sequential instruction fetches, the instruction pipeline must be emptied and then refilled based on the destination address of the branch, call or interrupt vector. These types of operations require at least three cycles to execute when fetching the instruction from external memory or from internal program ROM. This type of instruction pipelining is not found in the ADSP-2105 (the fast instruction execution speed is achieved by other design techniques), and no extra overhead is encountered in the ADSP-2105 for jumps, subroutines or interrupts regardless of whether they are conditional or not.

TMS320C25 Program Sequencer Instructions

Arithmetic instructions cannot be conditional. Only branch instructions are conditional. Branch instructions with direct addresses require two program memory words.

```
BACC
BANZ address
BGEZ address
BIOZ address
```

The TMS320C25 must use an explicit instruction to check a loop count and perform conditional branches. This requires one cycle of overhead for each iteration. A repeat instruction is also provided. It allows a single instruction to be repeated up to 256 times. The syntax is shown below.

```
RPT data memory address
RPT{*|*+|*-|*0+|*0-|*BRO+|*BRO-} [,<next ARP>]
```

PROGRAM SEQUENCER SUMMARY

Efficient looping capabilities are very important for DSP algorithms due to their repetitive nature. If zero-overhead looping capabilities are not found in a DSP processor, as with the TMS320C25, straight line coding may be required to avoid the overhead incurred with looping. This type of coding avoids overhead cycles but makes inefficient use of program memory space. In fact, the TMS320C25 can require hundreds of times more program memory than the ADSP-2105 for algorithms such as the FFT because of this characteristic of its architecture.

Table III. Program Sequencing Capabilities

DSP Requirement	ADSP-2105	TMS320C25
Zero-Overhead Looping (1 Instruction Inside Loop)	✓	✓
Zero-Overhead Looping (2 or More Instructions Inside Loop)	✓	No
Conditional Arithmetic Instructions	✓	No
Zero-Overhead Branching	✓	No*
Speed Achieved with Pipelining	Not Required	✓
Automatic Status Saving During Interrupt Vector	✓	No

*Affects the pipeline; the exact number of cycles of overhead is a function of memory configuration and branch destination

A FOOTNOTE

THE ADSP-2105 COMPARED TO THE TMS320C50

The TMS320C50 architecture has some of the same characteristics as the TMS320C25. Limited support for circular buffering was added. However, only two circular buffers can be maintained with only increment and decrement for address modifications. Circular buffers can only be used in data memory.

The TMS320C50 also has an instruction pipeline similar to the TMS320C25. Pipeline conflicts as well as overhead cycles in the program flow will result because of the instruction pipeline. The ADSP-2105 instructions execute in a single cycle with no extra overhead regardless of whether that instruction is a jump, subroutine call, or conditional instruction.

The looping capability of the TMS320C50 is improved over that of the TMS320C25. It still cannot execute some constructs supported by the ADSP-2105 such as terminating a loop upon an arithmetic condition as well as the expiration of a count.

SUMMARY

The DSP processors available on the market today vary drastically in their ability to meet these requirements. In fact, some DSP-oriented processors, like the TMS320C25, are better high speed microcontrollers than they are DSP processors. Analyzing the requirements of your DSP system and matching them to the capabilities of a DSP architecture will assure efficient operation.

Digital signal processing is a specialized branching of processor design and application. The fundamental requirements of DSP are summarized in Table IV.

Due to space limits, this article, does not cover many topics in detail. Consult the *ADSP-2100 Family User's Manual* and the *ADSP-2100 Family Assembly Tools Manual* for a greater depth of information on this processor.

Table IV. Overall DSP Requirements

DSP Requirements	ADSP-2105	TMS320C25
Fast Arithmetic	✓	Some Multicycle
Extended Dynamic Range on Multiplication/Accumulation	✓	No
Single-Cycle Fetch of Two Operands	✓	✓*
Hardware Circular Buffering (Both On- and Off-Chip)	✓	No
Zero Overhead Looping & Branching	✓	No

*MAC and MACD instructions only

APPENDIX A: PERFORMANCE BENCHMARKS

Since evaluating every detailed feature of many DSP processors can be time consuming and tedious, performance benchmarks can be frequently used to tell the whole story. If the arithmetic, address generation, and program sequencing architecture is superior it will be reflected in the benchmarks. A list of benchmarks are shown below for the ADSP-2105 and the TMS320C25.

Table V. Benchmark Comparison

Function	ADSP-2105KP-55	TMS320C25-50
Cycle Time	72.3 ns	80 ns
MIPS	13.824	12
FIR Filter Tap	72.3 ns	80 ns
Biquad IIR Filter	506 ns	800 ns
LMS Adaptive Filter Tap Update	145 ns	320 ns
1024-Point Complex Radix-4 FFT	2.69 ms	5.6 ms
GSM Speech Coding Processor Loading	3.25 MIPS	5 MIPS

APPENDIX B: PROGRAM EXAMPLE

To illustrate some of the issues discussed above, a code example is shown below for the ADSP-2105 and the TMS320C25. To avoid long listings and confusion, a short program which performs a matrix multiply of a 3×3 matrix with a 3×1 matrix is shown. Both processors perform identical tasks so that no interpretation of the type of algorithm is required. Neither code example shows any initialization of pointers nor the set up of any modes. The examples only focus on the core operation for simplicity.

Because these example are short, the performance advantage of the ADSP-2105 is not as apparent as in a more realistic example. Nevertheless, the ease of coding and benefits of the looped structure can be seen. Consult the benchmark tables for more definitive performance comparisons.

ADSP-2105 Code Example Description

The code above uses the looping capabilities of the ADSP-2105 and can be expanded for larger matrices by simply changing the number of loops (the value loaded into the counter). The I registers of the address generator are initialized to point to the first element of the input arrays and the output array. Circular buffering is used so that the address will circulate through the array. This allows automatic circulation through the 3×1 matrix for each row calculation. Data can reside anywhere in data memory without restrictions and can take up the full 16K data space if necessary.

The routine starts by fetching the first element of the two matrices from the data memories. One value is fetched from program memory data space while the

other is fetched from data memory. The counter is then loaded with the number of rows of the matrix. The DO UNTIL loop is set up and the computations can begin.

Matrix elements are multiplied while the next elements are fetched. Both values are treated as signed numbers with the specification (SS). The products are accumulated with the MAC instructions and the final sum of products is rounded so that it can be sent as a 16-bit result to data memory.

The program memory requirements are not large because of the looping capabilities. The program size does not change for larger arrays, only the loop counter value changes. Also, for multidimensional arrays, the loops can be nested with column loops inside of row loops for very compact code. Total execution time for this example program is 1.446 μs.

ADSP-2105 MATRIX MULTIPLY CODE EXAMPLE

```
start:      MX0=DM (I0,M0), MY0=PM (I4, M4);
            CNTR=3;
            DO row_loop UNTIL CE;
            MR=MX0*MY0(SS), MX0=DM(I0,M0),
              MY0=PM(I4,M4);
            MR=MR+MX0*MY0(SS), MX0=DM(I0,M0),
              MY0=PM(I4,M4);
            MR=MR+MX0*MY0(RND), MX0=DM(I0,M0),
              MY0=PM(I4, M4);
row_loop:   DM(I1,M0)=MR1;
```

TMS320C25 Code Example Description

The code for the TMS320C25 is straight line since no looping capability is available. Direct addressing is used so that the data must be restricted to a 128 word block. If the matrix is to be expanded, the program must be rewritten because it is not general purpose. Indirect addressing is not used because there is no support for circular buffering and there is no looping capability that allows for more iterations to be specified.

The routine starts by loading the T register with the first matrix element. Next, data of the second matrix is fetched and the two values are multiplied. A new value is loaded into the T register and the first product is saved in the accumulator. Another multiply is performed. The T register is loaded with another value as the previous products are accumulated. Notice that the fetching of operands and accumulate, and the multiply are specified and performed in different cycles as opposed to the ADSP-2105 which allows for everything to be specified and performed in a single cycle. The data result is then written to data memory.

As the matrix gets larger, the code space requirement also gets larger. The lack of looping capability results in the inefficient use of program memory space. If looping is desired, it would need to be done explicitly with extra instructions. These extra instructions would introduce overhead and would hurt the benchmark performance. Almost all benchmarks for the TMS320C25 need to be done with straight line code for good performance. This program executes in 1.8 μs. This approach, of course, can use quite a bit of program memory space.

TMS320C25 MATRIX MULTIPLY CODE EXAMPLE

```
LT a1
MPY b1
LTP a2
MPY b2
LTA a3
MPY b3
LTA a4
SACH R1, S
MPY b1
LTP a5
MPY b2
LTA a6
MPY b3
LTA a7
SACH R2, S
MPY b1
LTP a8
MPY b2
LTA a9
MPY b3
APAC
SACH R3, S
```

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AD1847 Serial-Port Codec Interface Example for a Parallel Bus

INTRODUCTION

This document describes in detail an example of how the AD1847 Codec can be interfaced to a parallel data bus utilizing interrupt driven data transfers. While simple, this design can serve as a starting point for more sophisticated bus interfaces.

OVERALL DESCRIPTION OF THE SYSTEM

The goal of the system described below is as follows:

1. The AD1847 is to be interfaced to a 16-bit parallel bus.
2. The AD1847 should operate in a 2-wire mode, with 16 slots per frame.
3. The bus interface logic will issue a bus interrupt when data and control information can be read/written.
4. Control data needs only be sent to the interface logic (by the CPU) when new AD1847 controls are to be implemented.

Even though the system presented in this document describes an ISA bus interface, most of the design is not bus specific and is therefore applicable to other parallel busses.

HARDWARE DESCRIPTION

Figure 1 shows a block diagram of the system whereas Figures 2–9 show the individual blocks. As one might expect from reading the specs on the AD1847 interface, the bulk of the system is composed of six 16-bit shift registers. Three of these are dedicated to sending data to the AD1847 (PISO, Parallel-In-Serial-Out registers) and the other three to receiving data from the AD1847 (SIPO,

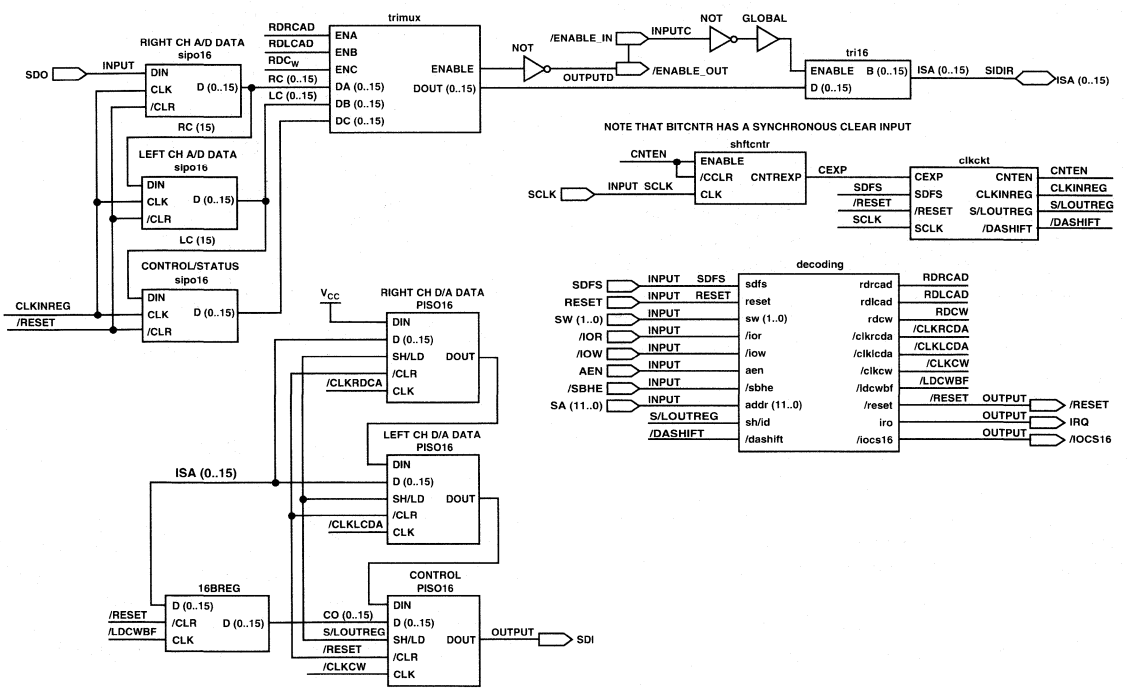

Figure 1. System Block Diagram

Serial-In-Parallel-Out registers). An additional 16-bit register contains outgoing control information (to be sent to the AD1847). It is assumed that the bus can always respond to data requests (interrupts) well within $1/F_S$, (where F_S is the sample rate). This eliminates the need for data buffers (FIFOs). To be more precise, the system has about $1/F_S - 3 \times 16/F_{SCLK}$ seconds to respond to an interrupt, where F_{SCLK} is the frequency of the AD1847 serial clock (either 12.288 MHz or 16.9344 MHz depending on the sample rate selected).

The AD1847 serial clock (SCLK) is used to clock data in and out of the shift registers. Note that the AD1847 input/output data is valid on the falling edge of SCLK and therefore an inverted version of SCLK (/SCLK) is used to clock the SIPOs.

As the AD1847 data sheet explains, the SDFS output indicates the start of a new frame. Since the AD1847 will be configured for a two-wire, 16-frames-per-slot mode in this design, the shift registers only need to receive (SIPOs) or transmit (PISOs) the first three 16-bit words of a frame. The first word contains control information, the second left channel data, and the third the right channel data. This applies to both AD1847 data input (SDI) and output (SDO).

Both the PISO and the SIPO registers are connected in series so that after 3×16 clocks all the bits are in proper positions. At that time the shift register clocks are disabled and an interrupt is generated as explained later.

Shift Register Clock Control

The SDFS signal indicates the beginning of a new frame and can therefore be used to synchronize a state machine or activate signals that control the AD1847 data stream. As Figure 8 shows, a flip-flop (CNTEN) is set when SDFS goes high, which in turn enables a 6-bit counter. This counter keeps track of how many data bits have been shifted in/out of the AD1847. CNTEN also controls the clear function of the counter. Whenever CNTEN is low, counting is disabled and the counter is cleared upon receiving a clock signal. When CNTEN is set high the counter starts counting. Upon a count of 3×16, when all input bits have been shifted into their correct positions, a counter expiration signal (CEXP) is generated that results in CNTEN being brought low. Half a SCLK period later both the PISO and SIPO clocks are disabled. The cycle repeats when SDFS goes high again.

Figures 8 and 9 show how the clocks for the shift registers, PISOs and SIPOs are generated. These clocks are gated versions of SCLK and /SCLK. Also shown is a signal called S/LOUTREG which controls whether the PISO registers perform shift or parallel load operations upon receiving a clock.

Figure 10 shows one cycle of the SDFS, CNTEN, interrupt, PISO/SIPO clocks and other signals.

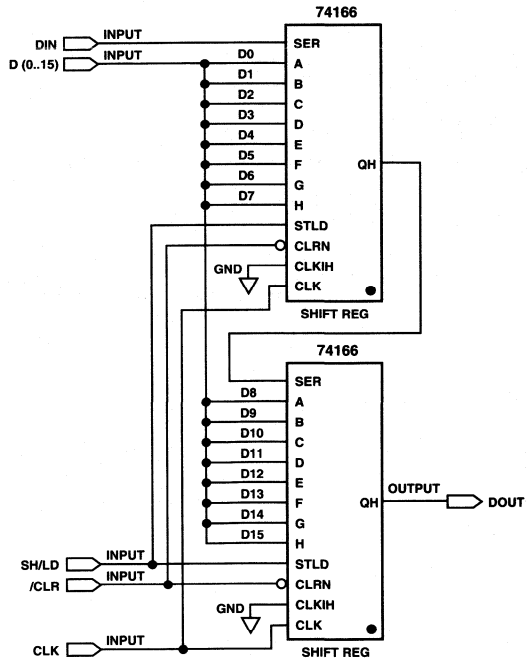

Figure 2. PISO16

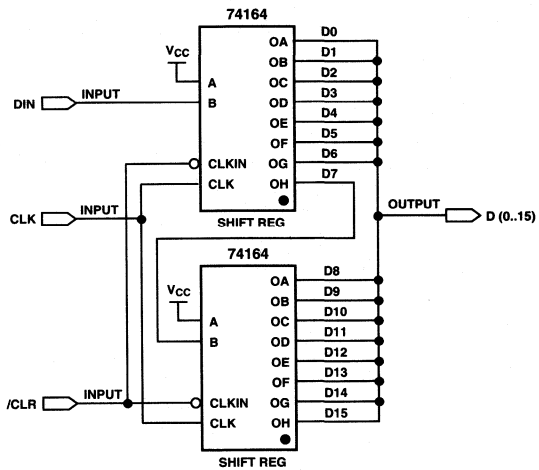

Figure 3. SIPO16

Interrupts

The interrupt generation is handled by a flip-flop called "interrupt." The falling edge of S/LOUTREG is used to set the flip-flop. The output of the interrupt flip-flop can be connected directly to the bus interrupt line since the SIPO data is valid when the interrupt signal is generated and the PISO registers are ready to accept data. The bus

has until half a SCLK period after the next SDPS signal, or about ($1/F_S - 3 \times 16/F_{SCLK}$) seconds, to respond to the interrupt, i.e., read the SIPO registers and write to the PISO registers. The SDFS signal, RESET, or a bus access to any of the six registers clears the interrupt.

Register Addressing

The mapping of the data registers to the bus I/O memory space is obviously design specific. The system described in this document uses a couple of jumpers to determine the addresses of the PISO and SIPO registers. Depending on the state of these jumpers a base address of 200H, 220H or 240H is selected. The control registers (SIPO and PISO) sit at the base address. The state of the bus read (IORD) and write (IOW) signals determine whether the PISO or SIPO registers are selected. The PISO registers are write only registers, where as the SIPO registers are read only. The left channel data is mapped into base address +2, and the right channel data into base address +4. Note that in addition to a clock signal, the PISO registers need a signal, shift load control (SH/LD), indicating whether the register should be loaded from the bus or its contents shifted upon receiving a clock signal. The SH/LD is generated by the "clkckt" module (S/LOUTREG) as shown in Figure 8. The signal ensures that the PISO data will get shifted properly during an AD1847 frame. Subsequent clock signals (generated by a decoded IOW signal) will clock data on the bus into the PISO register being addressed. The PISO clocks are therefore a combination of a gated SCLK and a decoded IOW signal as shown in the text design file in Figure 9.

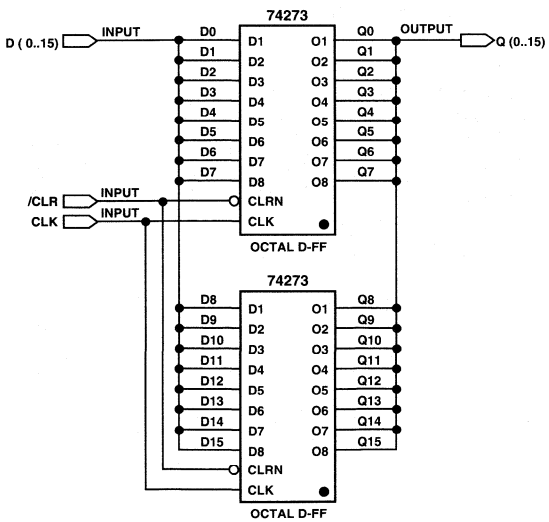

Figure 4. 16BREG

Control Word Buffer

Slot one of the AD1847 interface always contains control information to be received by the AD1847. These bits can therefore not be set arbitrarily. To relieve the bus from having to update the control PISO for every sample when they are not changing, a separate 16-bit buffer contains the most recent control word written by the bus master. The falling edge of SDFS loads this buffer into the control PISO. This ensures that the AD1847 always receives valid control data.

Right Channel D/A SIPO Input

As explained later, the AD1847 initialization procedure calls for shifting a one into the right channel D/A PISO. Its input is therefore tied to V_{CC}. During digital loopback, the AD1847 A/D data is mixed with the D/A data sent from the CPU to form the final data sent to the D/A converters. If one only wants to loop data from the A/D to the D/A, shifting a logic one into the right channel D/A PISO does not cause a problem because the external D/A data input can be disabled while the internal loopback is still enabled. Consult the AD1847 data sheet for details.

Configuring the AD1847 for Two Wire, 16 Slots per Frame

Upon reset, the AD1847 is by default configured in a single line mode with 32 slots per frame. The first task the system software needs to do is to change the AD1847 from the default mode to the two-wire, 16-slots-per-frame mode by writing a hexadecimal word of 4CC0H to the Control Word Input Register (MCE=FRS=TSSEL=1). This will instruct the AD1847 to change to 2-wire, 16-slot-per-frame mode upon the generation of next frame sync signal (SDFS). This will be the

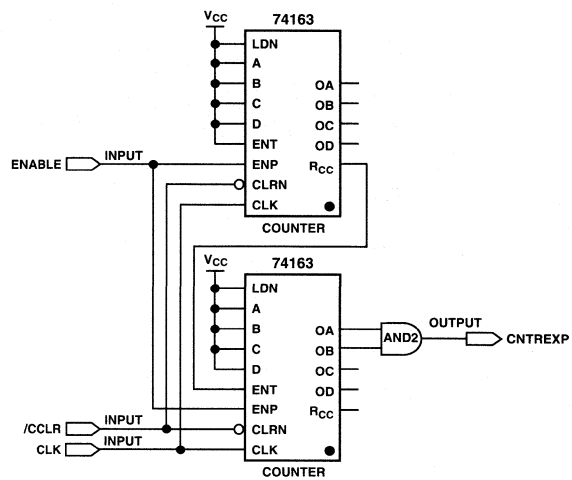

Figure 5 SHFT CNTR

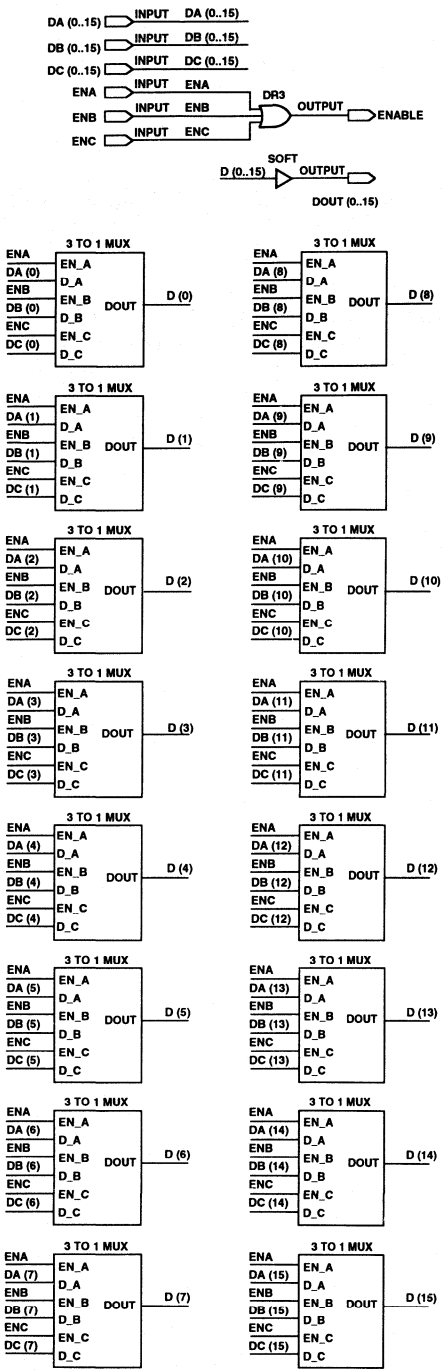

Figure 6. TRIMUX

first 16-bit word shifted out to the AD1847 after the falling edge of SDFS and the only control word sent to the AD1847 during this frame. Note, however, that since the AD1847 is configured for default mode it is expecting another control word (slot number 16). Since the PISO clocks are disabled after 3 × 16 clocks, all the bits of the remainder of the frame, including the control word in slot 16, will get the value shifted into the right channel D/A PISO (see Figure 1) at the first rising SCLK after SDFS. If this bit is 0, all the bits of the second control word, including MCE, will be 0. Bringing MCE low will place the part in autocalibration which is not desirable at this point. It is therefore important that the MCE bit of the second control word of this frame be 1. Since writing all ones to the second control register will not have any effect at this point, it is acceptable to permanently tie the input to the right channel D/A PISO high. At the next frame sync (SDFS) the AD1847 serial interface is temporarily disabled. The INIT bit will be set to 1 to indicate this fact. The software should wait for the INIT bit to be set to 1 followed by 0 (an interrupt indicates the presence of new control information). This indicates that the serial interface is alive again. At this point the interface will be configured properly. The software would typically proceed to configure the AD1847 controls to their desired value with the MCE bit still high to hold off autocalibration and only when fully configured (except for output muting) the MCE bit would be brought low. At that point the AD1847 will enter autocalibration mode. The ACI bit of the status register should be polled and the software should wait for ACI to be set to 1 and then to 0. When ACI is 0, autocalibration is finished and after muting the D/A outputs the part is ready for normal operations.

APPENDIX

Hardware Summary

The design described above was implemented on an EPM7160LC84 using MaxPlus2 software. The Figures 1–9 show the modules that make up the design. The following summarizes the functions of the main modules.

Decoding
This text design file contains the description of the interrupt flipflop, along with decoding logic for the interface registers. The following lists the regctrl input and output signals:

Name	Origin
sdfs	AD1847 frame sync
reset	ISA bus
sw 1–2	External jumpers that determine register base address
/iord	ISA bus
/iowr	ISA bus
aen	ISA bus
/sbhe	ISA bus
addr0–11	ISA bus
s/loutreg	clkckt module
/dashift	clkckt module

Output	Destination and Purpose
rdrcad	trimux. Rdrcad controls the three-state buffer at the output of right channel A/D SIPO. The buffer is enabled when the bus reads the right channel A/D data.
rdlcad	trimux. Same signal as rdrcad except for left channel.
rdcw	trimux. Same signal as rdrcad except for control data.
/clkrcda	Right Channel D/A Data PISO. This clock signal causes the PISO data to be shifted or data to be loaded from the bus into the PISO, depending on the status of the PISO SH/LD input.
/clklcda	Left Channel D/A Data PISO. Similar function as /clkrcda.
clkcw	Control PISO. Similar function as clkrcda except data is loaded from the control buffer (16BREG).
/ldcwbf	16BREG. This signal loads the bus contents into the control buffer.
/reset	Resets the AD1847. Inverted version of the ISA reset.
irq	ISA bus interrupt.
/iocs16	ISA bus.

/clkckt
This module generates control and clock signals for the PISO and SIPO registers along with a shftcntr control signal.

Output	Destination and Purpose
cnten	shftcntr. Controls when the shift counter is enabled, disabled and when it is cleared.
clkinreg	SIPO clock input. Enabled only when AD1847 data is being received.
s/loutreg	PISOs. This signal determines whether the PISO input clocks will result in shifting or loading.
/dashift	decoding. Used by the decoding module to generate the clock signals for the PISOs.

shftcntr
This synchronous counter (synchronous clear) keeps track of the number of bits being received or sent to the AD1847. Upon a count of 3 × 16 a counter expiration signal (cexp) is generated.

trimux and tri16
These blocks implement three-statable buffers at the output of the SIPO registers. Whenever the bus reads one of the SIPO registers the proper buffer is enabled.

SIPO
Serial-In-Parallel-Out registers. These registers shift data in (control, left and right channels) from the AD1847. This data is then read by the bus.

PISO
Parallel-In-Serial-Out registers. These registers, after being loaded from the bus, shift data (control, left and right channels) to the AD1847.

16BREG
This buffer is loaded by the bus with control information for the AD1847. The SDFS signal loads this information into the PISO control shift register.

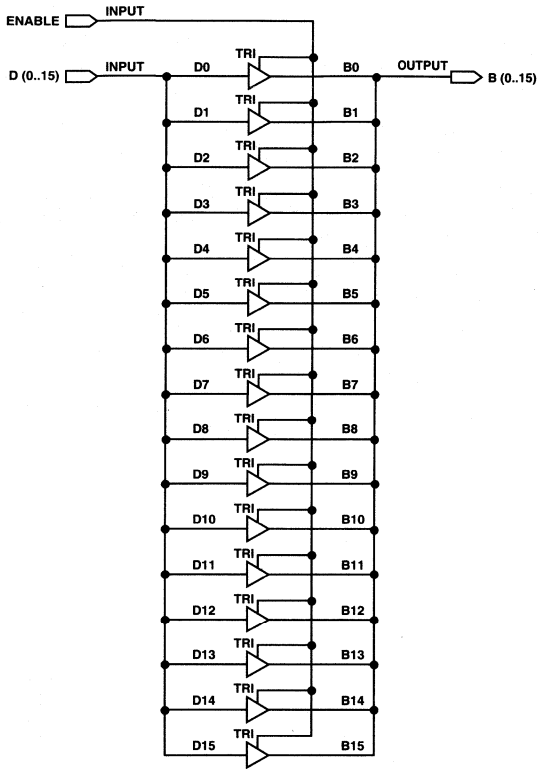

Figure 7. TRI16

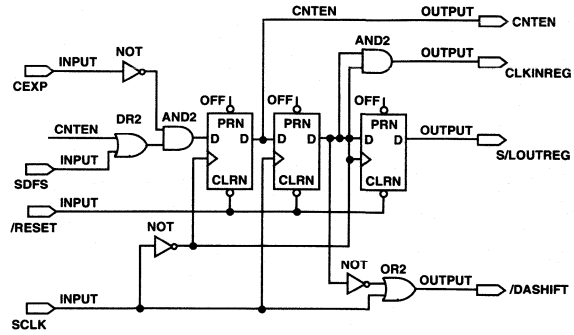

Figure 8. CLK CKT

SUBDESIGN Decoding

```
(
        sdfs, reset, sw[1. .0], /ior, /iow                  :INPUT;
        aen /sbhe,addr[11. .0],sh/ld,/dashift               :INPUT;
         rdrcad,rdlcad,rdcw,/clkrcda,/clklcda,/clkcw        :OUTPUT;
         /ldcwbf, /reset,irq,/iocs16                        :OUTPUT;
)
VARIABLE
        adv, /cw, /lcd, /rcd                                :LCELL;
        interrupt                                           :DFF;

        BEGIN

%The following case statement decodes the bus address lines.%
%The valid addresses depend on the status of two external
%signals (jumpers)%
```

Figure 9. (Continued on next page)

```
CASE (SW[1. .0]) IS
        WHEN B"00" =>
        adv     =(((addr[]==H"200") # (addr[]==H"202") #
                  (addr[]==H"204")) & !aen & !/sbhe);
        /cw     =!(addr[]==H"200") # aen # /sbhe;
        /lcd    =!(addr[]==H"202") # aen # /sbhe;
        /rcd    = !(addr[]==H"204") # aen # /sbhe;

        WHEN  B"01" =>

        adv     =(((addr[]==H"220") #     (addr[]==H"222") #
                  (addr[]==H"224")) & !aen & !/sbhe);
        / cw    =!(addr[]==H"220") # aen # /sbhe;
        /lcd    =!(addr[]==H"222") # aen # /sbhe;
        /rcd    =!(addr[]==H"224") # aen # /sbhe;

        WHEN B"10" =>
        adv     =(((addr[]==H"240") # (addr[]==H"242") #
                  (addr[]==H"244")) & !aen & !/sbhe);
        /cw     =!(addr[]==H"240") # aen # /sbhe;
        /lcd    =!(addr[]==H"242") # aen # /sbhe;
        /rcd    =!(addr[]==H"244") # aen # /sbhe;
END CASE;

        rdcw    =!(/cw # /ior) ;%read (enable) signal for the control
                                word three-state buffer%
        rdlcad  =!(/lcd # /ior) ;%. . . left channel a/d . . . .%
        rdrcad  =!(/rcd # /ior) ;%. . . right channel a/d . . .%

        /ldcwbf =(/cw # /iow) ;%load signal for the control word buffer%


%the following signals are the clock signals for the piso16 registers%
%the clock signals are active during data being shifted to the AD1847%
%and when the ISA bus loads these registers%

        /clkcw  =   !sdfs & (/dashift) ;        %control data piso clock%
        /clklcda =(/lcd # /iow) & (/dashift) ;  %left ch d/a piso clock%
        /clkrcda =(/rcd # /iow) & (/dashift) ;  %right ch d/a piso clock%

%The following defines an interrupt flip flop that is set when%
%three 16 bit words have been received/sent from/to the AD1847.%
%The interrupt is cleared by accessing any register on the chip.%
%by the sdfs signals or reset%

        interrupt.clrn  = !(reset # sdfs # adv);
        interrupt.clk   = !sh/ld;
        irq             = interrupt.q;
        interrupt.d     = vcc;

        /reset          = !(reset);
        /iocs16         = TRI (GND,adv) ;%indicates to ISA bus that data
                                         transfers are 16 bit%
END ;
```

Figure 9.

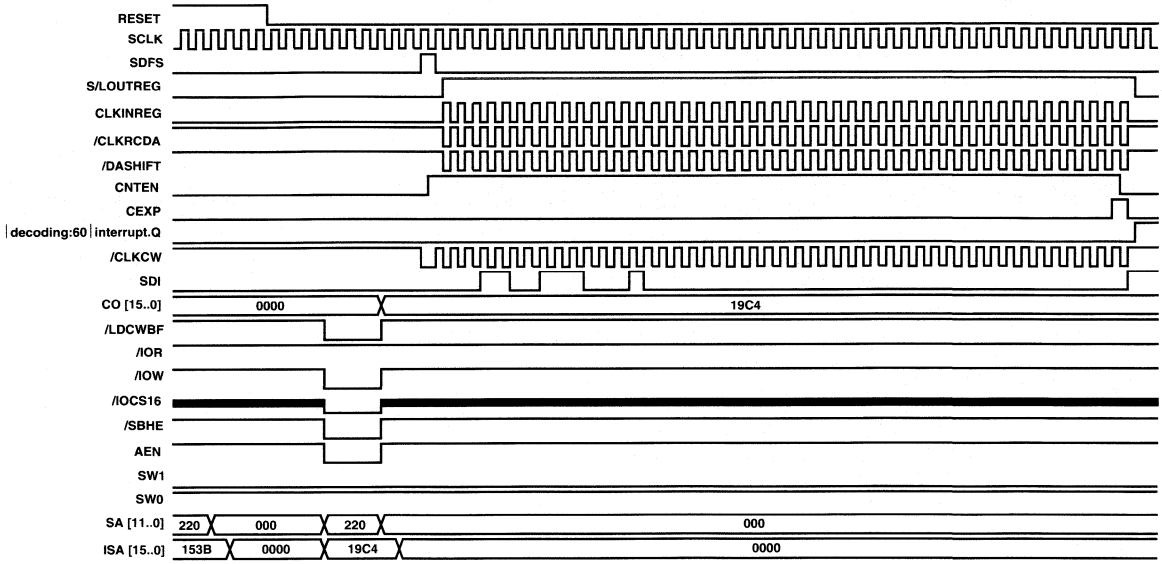
RESET
SCLK
SDFS
S/LOUTREG
CLKINREG
/CLKRCDA
/DASHIFT
CNTEN
CEXP
decoding:60 interrupt.Q
/CLKCW
SDI
CO [15..0]
0000
19C4
/LDCWBF
/IOR
/IOW
/IOCS16
/SBHE
AEN
SW1
SW0
SA [11..0]
220
000
220
000
ISA [15..0]
153B
0000
19C4
0000

Figure 10.

CODEC PCB & CIRCUIT APPLICATION GUIDELINES

Extending the comments in the data sheets (e.g., AD1848) regarding grounding (and bypassing), include the following brief notes and comments as a general "good-practice" guide for mixed signal designs.

1. The power supply decoupling and bypassing shown in the attached drawing (ref AD1848K) is okay. It needs to be emphasized that low ESL 10 nF to 100 nF surface mount ceramic capacitors *must* be mounted right at the leads of the chip (or at least within a couple of mm). Remember the "rules-of-thumb" for trace length—L $\approx$ 1 nH/mm, R $\approx$ 2 mΩ/mm (for common 250 μm wide traces, 38 μm thick (1 oz) foil).

2. Avoid switch mode power supplies near ADCs, DACs and analog circuits. Sometimes it is easier to use a separate 5 V three terminal regulator (e.g., TO-39 metal can), at the chip, for the analog supply. A 10 μF Tantalum or aluminum capacitor at the board edge helps to reduce power supply noise and the ESR damps ringing from decoupling chokes.

3. ADI recommends extending the ground plane philosophy to include separate digital and analog power planes directly over their respective ground planes—no overlapping of planes. The two plane pairs should be separated by a 2 mm–3 mm gap. This means using a three or four layer board with the ground and power planes forming a high capacitive sandwich. This gives an extremely effective, low ESR, low ESL bypass capacitor consisting of the separate ground and power planes themselves, with an effective capacitance of $\approx$5 pF/cm^2. The IC leads will have vias that go directly to the appropriate plane for power and ground. All digital components are mounted over the digital power/ground plane sandwich and all analog components over the analog power/ground sandwich. This doesn't minimize the need for additional ceramic bypass capacitors at the pins as mentioned above. The importance and effectiveness of ground planes cannot be overemphasized.

4. A single link between the two planes should be established, preferably close to the chip itself. This is necessary to prevent any potential difference due to ESD or fault currents that could otherwise flow through the chip substrate with damaging affect. It may be useful to provide for removable links in several PCB locations, to permit debugging and testing for ground isolation.

5. All digital signals and components should be located away from analog circuitry (and, naturally, vice versa). All high-speed traces should take the most direct route *over the correct ground or power plane.* If this is not possible, a ground trace should be routed under the high speed trace wherever possible, to minimize self-inductance.

6. Avoid the use of sockets.

7. Don't overlook adjacent PLDs and VLSI logic chips on the same PC board. These chips frequently include lots of synchronous logic and generate large switching currents that can infiltrate the rest of the board. Make sure they are well bypassed—at the chip pins! This will not only ensure their reliable operation but minimize impact on the supply lines.

8. Be aware of problems that might occur due to multiple crystal oscillators, e.g., beats between harmonics that can enter the CODEC through either the analog or digital supplies or signal/reference pins. If possible, only enable a single oscillator on a PC board at a time or derive all the required frequencies from a single oscillator.

9. Watch out for the "traditional" design problems. Ground loop area (inductive coupling), minimize. Common impedance (current) coupling, minimize or use star points. Capacitive (voltage) coupling, separate, shield or lower circuit impedance. Surface and/or bulk leakage—separate, guard, conformal coat. Parallel trace coupling (combinations of above)—separate, terminate in characteristic impedance, use ground plane and/or intermediate grounded traces.

10. Watch out for capacitive coupling from the body of large components. Use the "outside foil ring," marked on capacitors, to identify which end to ground.

11. Watch out for the external magnetic field of inductors and transformers. Use electrostatic and magnetically shielded components if necessary. RF decoupling chokes can be mounted at right angles to minimize mutual inductance. Power transformers should be mounted off the board and oriented, with the most intense area of their external field away from critical analog circuits. Use of toroidal power transformers will minimize external fields.

12. Minimize capacitive loading on output pins. For digital signals, driving 'long' traces, it may be necessary to terminate the trace in its characteristic impedance, $\approx$100 Ω for most applications.

13. Ensure that offset biased, analog CODEC/ADC input signals, can*NOT* go above V_{CC} or below ground even momentarily. Use 'clamps' or five-volt single rail op amps buffers to limit signal excursions.

14. Consider EMI/RFI requirements for analog input and output lines. Input lines can radiate (and receive) RF and the CODEC line output contains many harmonic products of the sampling process.

15. Finally—remember when debugging, that *every assumption is suspect*!!

REFERENCES

Additional, general high-speed and mixed signal design, information is available in our seminar handbooks and application manuals as noted below. They are recommended as a source of good techniques and inspiration.

1. *Mixed Signal Processing Design Seminar,* Analog Devices, Inc., 1991, ISBN-0-916550-08-7.

2. *High Speed Design Seminar,* Analog Devices, Inc., 1990, ISBN 0-916550-07-9.

3. *Applications Reference Manual,* Analog Devices, Inc., 1993. Especially refer to collected Application Notes–Section 24, AN-214, AN-280, AN-282, AN-345, AN-346, AN-347, AN-353, AN-362.

4. *Noise Reduction Techniques in Electronic Systems,* 2nd Ed, Henry W. Ott, Wiley Interscience, 1988.

5. *Interfacing Techniques in Digital Design With Emphasis on Microprocessors,* Ronald L. Krutz, John Wiley, 1938.

6. *Audio/Video Reference Manual,* Analog Devices, Inc., 1992.

7. *Systems Application Guide,* Analog Devices, Inc., 1993, ISBN 0-916550-13-3.

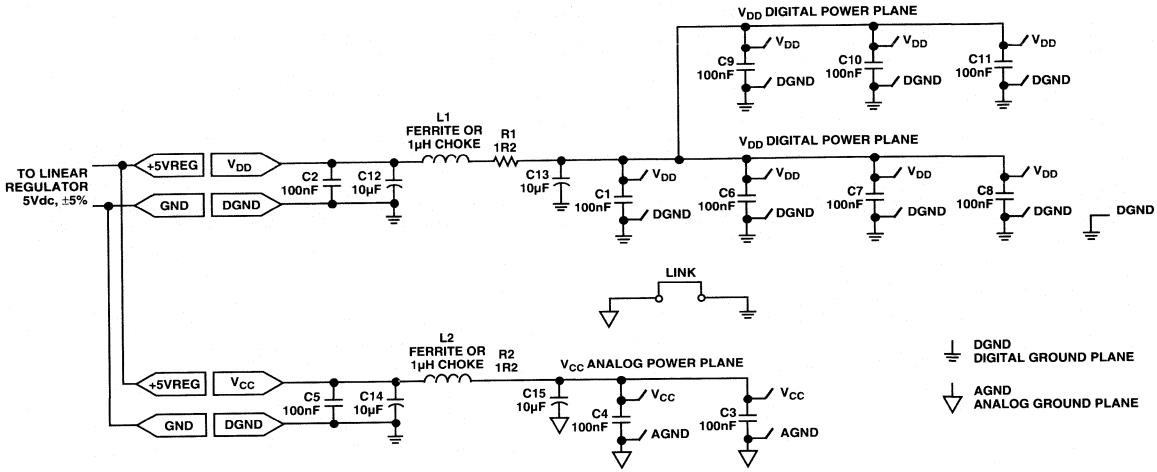
VDD DIGITAL POWER PLANE
VDD
C9
100nF
DGND
C10
100nF
C11
100nF
L1
FERRITE OR
1µH CHOKE
R1
1R2
TO LINEAR
REGULATOR
5Vdc, ±5%
+5VREG
GND
DGND
C2
100nF
C12
10µF
C13
10µF
C1
100nF
C6
100nF
C7
100nF
C8
100nF
LINK
L2
FERRITE OR
1µH CHOKE
R2
1R2
VCC ANALOG POWER PLANE
VCC
C5
100nF
C14
10µF
C15
10µF
C4
100nF
C3
100nF
AGND
DGND
DIGITAL GROUND PLANE
AGND
ANALOG GROUND PLANE

Figure 11.

ANALOG DEVICES

AN-388
APPLICATION NOTE

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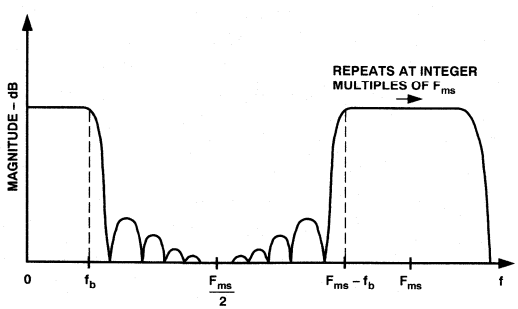
Using Sigma-Delta Converters–Part 1

Q: I'd like to use sigma-delta A/Ds but have some questions because they seem markedly different from what I've been using. To start with, what issues do I need to consider when designing my antialiasing filter?

A: A major benefit of oversampling converters is that the filtering required to prevent aliases can be quite simple. To understand why this is the case and what the filter constraints are, let's look at the basic digital signal processing that takes place in such a converter. For the purpose of anti-alias filter design we can think of a sigma-delta converter as a conventional high-resolution converter, sampling at a rate much faster than the Nyquist sampling rate, followed by a digital decimator/filter. That the input into the digital decimator is 1-bit serial with a noise-shaping transfer function doesn't matter.

The input signal is sampled at F_{ms}, the modulator input sampling rate, which is much faster than twice the maximum input signal frequency (the Nyquist rate). The figure shows what the frequency response of a decimation filter may look like; frequency components between f_b and $F_{ms}-f_b$ are greatly attenuated. Thus, the digital filter can be used to filter out all energy from the converter within $[0, F_{ms}-f_b]$ that does not fall within the bandwidth of interest $[0, f_b]$. However, the converter can not distinguish between signals appearing at the input that are in the range $[0, \pm f_b]$ and those in the ranges, $[kF_{ms} \pm f_b]$, where k is an integer. Any signals (or noise) in those ranges get aliased down to the bandwidth of interest $[0, f_b]$ via the sampling process; the decimation filter, which works only on the digitized samples, cannot be of any help attenuating these signals.



Thus it is the input noise energy in these bands $[kF_{ms} \pm f_b]$ that must be removed by the antialiasing filter before the input signal is sampled by the converter.

Q: So if I were to use the AD1877 (available in Spring, 1994), which has a dynamic range of 90 dB, the anti aliasing filter will need attenuation well above 90 dB at $F_{ms}-f_b$ (≈ 3 MHz)?

A: Not quite. You are assuming that the A/D has full-scale input at frequencies close to the modulator sampling rate; this is simply not the case in most systems. The only signal input of concern for aliasing is normally just noise from sensors and circuitry preceding the converter. The noise is usually low enough for a simple RC filter to suffice as an anti-alias filter.

Q: How do I make sure that a one-pole RC filter will suffice for my application—and establish the time constant of the filter?

A: Your application will typically specify a maximum allowable attenuation of an input signal that falls within the bandwidth of interest. This in turn puts a minimum on the 3-dB point of the RC filter. Let's take a look at an example using the AD1877 to illustrate this point further and to show how one might verify that a single-pole filter will provide enough filtering.

Let's assume that we have an application where the bandwidth of interest is 0 to 20 kHz, and signals in this range must not be attenuated more than 0.1 dB, or a ratio of 0.9886 [dB = 20 $\log_{10}$ (*ratio*) for voltage and 10 $\log_{10}$ (*ratio*) for power]. From the formula for attenuation of a single-pole filter,

$$ratio = \frac{1}{\sqrt{1 + (2\pi fRC)^2}} > 0.99 \text{ at } f = 20 \text{ kHz}$$

$$RC \leq \sqrt{\frac{1 - (ratio)^2}{(2\pi f)^2 (ratio)^2}} \approx 1.21 \times 10^{-6} \text{ s}$$

Choosing RC = 1.0 μs, to allow for component tolerances, the −3-dB frequency will be 159 kHz. We can now calculate the attenuation the filter will provide in the frequency bands, $kF_{ms} \pm f_b$, that alias down to the baseband. Assuming that the AD1877 has a modulator sampling rate of 3.072 MHz (and output sampling rate of 48 kHz), the first frequency band occurs at 3.052 MHz to 3.092 MHz. The attenuation of the RC filter at these frequencies is approximately 25.7 dB (about 0.052) over the whole band. Over the second band (6.124 MHz to 6.164 MHz), the attenuation is 31.8 dB (0.026). We know

that the noise in these two bands (and all higher bands up the scale) that escapes through the filter to the A/D input will be aliased down to the baseband and get added as root sum-of-the-squares (rss) of their rms values, i.e., $\sqrt{n_1^2 + n_2^2 + \ldots + n_1^2}$. For values given in dB, the formulas shown the Appendix can provide results directly in dB, avoiding the intermediate step of computing the ratios.

For white noise, the noise spectral density is constant as a function of frequency, and each frequency range has the same bandwidth, so each band contributes an equal amount of noise to the input of the filter. We can therefore find the effective attenuation of the RC filter by adding the attenuation of the different frequency bands in rss fashion. The noise contribution from the first two bands, for example, is the same as the contribution from a single frequency band with attenuation of $\sqrt{0.052^2 + 0.026^2} = 0.058$, or 24.7 dB, compared with 25.7 dB for the first band. How many bands do we need to consider when calculating the total aliased noise? For this case, the rss sums of the first 3, 4, 5, and 6 bands are, respectively, −24.2, −24.0, −23.9, −23.8 dB. The first band is therefore quite dominant; its attenuation is within 2 dB of the attenuation for all bands. It is usually sufficient to take only the first band into account unless the noise is exceptionally large or has a non-white spectrum; in addition, the A/D itself, though fast, has limited bandwidth; it tends to reject high-order bands.

Now that the attenuation is in hand, we can consider the noise magnitude itself: Let's be conservative (by about 50%) and take the effective filter attenuation to be 20 dB (i.e., 0.1 V/V). To be able to calculate the maximum allowed noise spectral density when using a single pole filter, an estimate should be made of the maximum performance degradation that aliased noise can contribute. From the dynamic specs of the AD1877 we find that the total noise power internal to the converter is 90 dB below (32 ppm of) full-scale input. If the whole system is to be within, say, 0.5 dB of this spec, the total aliased noise power can't exceed the rss difference between −90 dB and −89.5 dB or −99.1 dB (11.1×10^{-6}). Using this information, and the fact that the input scale of the AD1877 is 3 V p-p, we find that aliased noise must not exceed $3/(2\sqrt{2})$ V × 11.1×10^{-6} = 11.8 μV. If all this noise were assumed lumped in a single aliased band, and noting that rms noise = noise spectral density $\times\sqrt{\text{BW}}$,

$$N.S.D. < \frac{11.8\ \mu\text{V}}{\sqrt{3.092\ \text{MHz} \times 3.052\ \text{MHz}}} = 59\ \text{nV}/\sqrt{\text{Hz}}$$

This is the maximum post-filter spectral density allowed. To find the maximum prefilter spectral density (MPSD), with the effective filter attenuation of 20 dB (i.e., × =10) established previously, M.P.S.D. = 10 × 59 nV/$\sqrt{\text{Hz}}$ = 0.59 μV/$\sqrt{\text{Hz}}$.

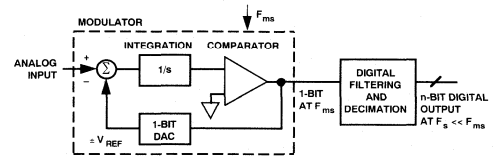
Clearly your system has to be pretty noisy in the 3-6-9-12-MHz regions in order for a simple RC filter not to suffice; however, as always, one must be careful of ambient rf pickup.

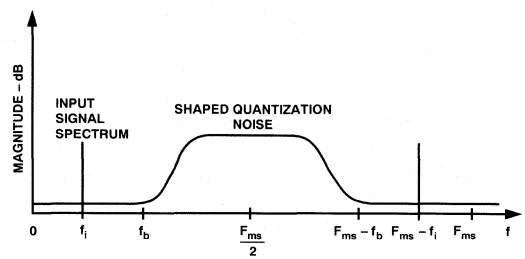
Q: As I understand it, the noise floor of sigma-delta converters may exhibit some irregularities. Any thoughts on that?

A: Most sigma-delta converters exhibit some spikes in the noise floor, called *idle tones*. In general, these spikes have low energy, not enough to substantially affect the S/N of the converter. Despite that, however, many applications cannot tolerate spikes in the frequency spectrum that extend much beyond the white noise floor. In audio applications, the human ear, for example, does an excellent job of detecting tones in the absence of large input signals even though the tones are well below the integrated (0-20-kHz) noise of the system.

There are two sources of idle tones. Their most common cause is voltage-reference modulation. To understand this mechanism a basic understanding of sigma-delta converters is needed. Here is a one minute crash course on sigma-delta converters (to probe further please consult).[1]

As the block diagram shows, a basic sigma-delta A/D converter consists of an oversampling modulator, followed by a digital filter and a decimator. The modulator output swings between two states (high and low, or 0 and 1, or +1 and −1), and the average output is proportional to the magnitude of the input signal. Since the modulator output always swings full-scale (1 bit), it will have large quantization errors. The modulator, however, is constructed so as to confine most of the quantization noise to the portion of the spectrum beyond f_b, the bandwidth of interest.





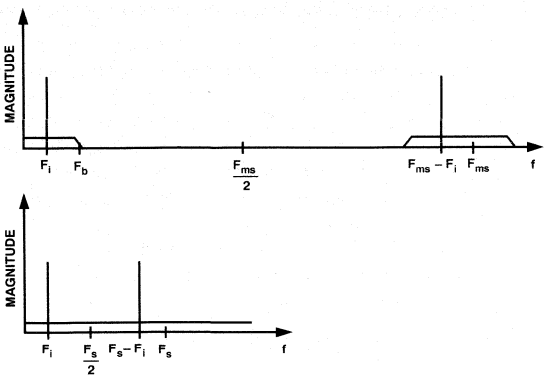
As shown, the spectral "sticks" (single frequencies) at f_i *and* $F_{ms}-f_i$ correspond to an input signal, while the shaded area shows how the quantization noise has been pushed (shaped) beyond the bandwidth of interest, f_b.

The digital filter, which is often an n-tap FIR filter, takes the high-speed low-resolution (1-bit) modulator output and performs a weighted average of n modulator outputs in a manner dictated by the desired filter characteristics. The output of the filter is a high-resolution word, which becomes the A/D output. The digital filter is designed to filter out "everything" between f_b and $F_{ms}-f_b$, *where* F_{ms} is the sampling rate of the modulator. Cleaning out all the noise in between f_b and $F_{ms}-f_b$ makes it possible to reduce the sampling rate to values between F_{ms} and $2f_b$ without causing any spectra to overlap (i.e., aliasing).

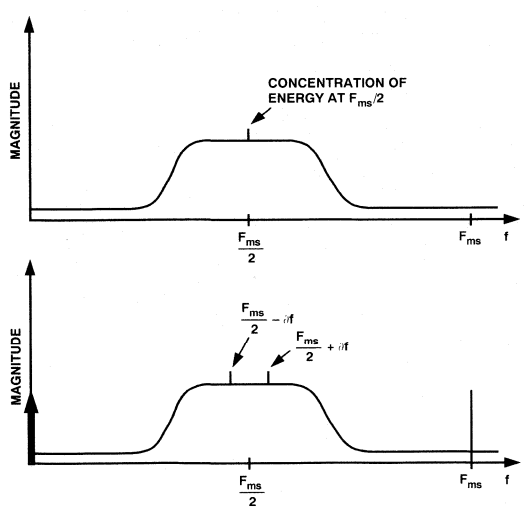
Conceptually, reducing the sample rate, i.e., *decimation*, can be thought of as only sending every dth digital filter output to the A/D output, where d is the decimation factor. This will bring the spectral images close together, as shown in the figure, which

makes the output look like an output from a non oversampled converter. The upper figure shows the output of the modulator after digital filtering but prior to decimation. The lower figure shows the spectral output after decimation—the final A/D output.

In real converters, digital filtering and decimation are intimately combined for economy in design and manufacture. Thus, the terms "digital filter" and "decimator" are used interchangeably to describe the digital circuitry processing the modulator output to produce the output of the converter.



O.K., now back to "idle tones". Let's start by looking at the output of the modulator when a dc signal is applied to the input. For an exact mid-scale dc input level, the output of the modulator is equally likely to be high (1) or low (0), in other words, the pulse density is 0.5, very likely to result in bitstream patterns like 010101. These regular patterns mean that the output spectrum will have a spike at $F_{ms}/2$ (upper figure). If the dc input now moves somewhat off midscale, the modulator output bit pattern will change accordingly. The spectrum of the modulator output will now show spikes at $F_{ms}/2-\partial F$ and $F_{ms}/2+\partial F$, with ∂F proportional to the dc change from midscale (lower figure).



With effective digital filtering, how can such tones possibly find their way down to baseband? The answer is via the *voltage reference*. The digital output is a measure of the ratio of the analog input to the voltage reference. An x% change in the magnitude of the voltage reference will result in a $-x$% change in the magnitude of the digital output word. Voltage-reference change will, in effect, amplitude modulate the A/D output. Now, we have clocks internal to the converter, and possibly also externally, running at $F_{ms}/2$. If small amounts of these clock pulses get coupled onto the voltage reference line, they will change it slightly and, in effect, modulate the tones at $F_{ms}/2-\partial F$ and $F_{ms}/2+\partial F$. One of the difference frequencies created by this modulation is at ∂F, and it is clearly in the bandwidth of interest. Nonlinearities may also create tones at multiples of ∂F.

Q: *From your explanation it seems that if I apply an ac signal to the converter I do not have to worry about idle tones?*

A: Well, any ac signal generally has a dc component associated with it, which will have to be represented by the modulator output, so the explanation above still applies. But if the total dc input offset (i.e., internal converter offset plus external offsets) in your system is exactly 0, the tones will be at dc (0 Hz).

There is another source of idle tones in lower-order (<3rd-order) modulators. The order of the modulator (number of integrations) is a measure of how much quantization-noise shaping takes place. Second-order modulators can actually exhibit bit patterns that show up directly in the baseband, even if voltage-reference modulation is not occurring. This is one of the reasons why sigma-delta converters from Analog Devices that are designed for ac applications use higher-order (≥3) sigma-delta modulators.

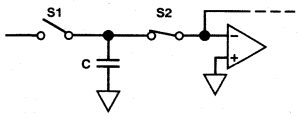
Q: *So what can I do to minimize the chances of idle tones interfering with my A/D conversion?*

A: Follow the layout recommendations and bypassing schemes recommended by the manufacturer of the converter. This applies not only to the voltage reference, but to power supplies and grounding as well. It is the manufacturer's responsibility to minimize the voltage-reference corruption that takes place *inside* the converter, but it is up to the system designer to minimize the *external* coupling. By following those guidelines, the user should be able to reduce the coupling to a negligible level. If, despite the proper design precautions, idle tones are still an issue, there is yet another option that can be pursued. As I explained previously, frequency of the idle tones is a function of the dc input. This opens up the possibility of introducing enough dc offset on the A/D input to move the idle tones out of the bandwidth of interest to where they will be filtered out by the decimation filter. If the user does not want the dc offset to propagate through the system it can be subtracted out by the processor that handles the data from the A/D.

Q: *What kind of a load does the input of sigma-delta converters present to my signal conditioning circuitry?*

A: It depends on the converter. Some sigma-delta converters have a buffer at the input, in which case the input impedance is very high and loading is negligible. But in many cases the input is

connected directly to the modulator of the converter. A switched-capacitor sigma-delta modulator will have a simplified equivalent circuit like that shown in the figure.



Switches S1 and S2 are controlled by the two phases of a clock to produce alternating closures. While S1 is closed, the input capacitor samples the input voltage. When S1 is opened, S2 is closed and the charge on C is dumped into the integrator, thus discharging the capacitor. The input impedance can be computed by calculating the average charge that gets drawn by C from the external circuitry. It can be shown that if C is allowed to fully charge up to the input voltage before S1 is opened that the average current into the input is the same as if there were a resistor of $1/(F_{sw}C)$ ohms connected between the input and ground, where F_{sw} is the rate at which the input capacitor is sampling the input voltage. F_{sw} is directly proportional to the frequency of the clock applied to the converter. This means that the input impedance is inversely proportional to the converter output sample rate.

Sometimes other factors, such as gain, can influence the input impedance. This is the case for the 16/24-bit AD771x family of signal conditioning A/Ds. The inputs of these converters can be programmed for gains of 1 to 128 V/V. The gain is adjusted using a patented technique that effectively increases F_{sw} (but keeps the converter output sample rate constant) and combines the charges from multiple samples. The input impedance of these converters is, for example, 2.3 MΩ when the device's external clock is 10 MHz and the input gain is 1. With input gain of 8, the input impedance is reduced to 288 kΩ.

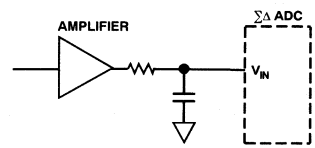
These impedances, as noted earlier, represent the average current flow into or out of the converters. However, they are not the impedances to consider when determining the maximum allowable output impedance of the A/D driver circuitry. Instead, one needs to consider the charging time of the capacitor, C, when S1 is closed. For dc applications the driver circuit impedance has only to be low enough so that the capacitor, C, will be charged to a value within the required accuracy before S1 is opened. The impedance will be a function of how long S1 is closed (proportional to the sampling rate), the capacitance, *C* and C_{EXT} in parallel with the input (unless $C_{EXT} >> C$). The table shows allowable values of external series resistance with f_{CLKIN} = 10 MHz which will avoid gain error of 1 LSB of 20 bits—for various values of gain and external capacitance on the AD7710.

Typical External Series Resistance Which Will Not Introduce 20-Bit Gain Error

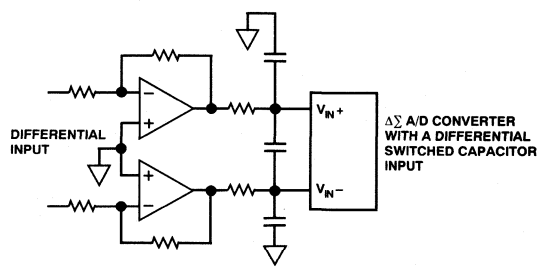
	External Capacitance (pF)					
Gain	**0**	**50**	**100**	**100**	**500**	**5000**
1	145 kΩ	34.5 kΩ	20.4 kΩ	5.2 kΩ	2.8 kΩ	700 Ω
2	70.5 kΩ	16.9 kΩ	10 kΩ	2.5 kΩ	1.4 kΩ	350 Ω
4	31.8 kΩ	8.0 kΩ	4.8 kΩ	1.2 kΩ	670 Ω	170 Ω
8–128	13.4 kΩ	3.6 kΩ	2.2 kΩ	550 Ω	300 Ω	80 Ω

For ac applications, such as audio, where the modulator sample rate is around 3 MHz for 64× oversampling, the input capacitor voltage may not have enough time to settle within the accuracy indicated by the resolution of the converter before the capacitor is switched to discharging. It actually turns out that as long as the input capacitor charging follows the exponential curve of RC circuits, only the gain accuracy suffers if the input capacitor is switched away too early.

The requirement of exponential charging means that an op amp can not drive the switched capacitor input directly. When a capacitive load is switched onto the output of an op amp, the amplitude will momentarily drop. The op amp will try to correct the situation and in the process hits its slew rate limit (non linear response), which can cause the output to ring excessively. To remedy the situation, an RC filter with a short time constant can be interposed between the amplifier and the A/D input as shown in the figure. The (low) resistance isolates the amplifier from the switched capacitor, and the capacitance between the input and ground supplies or sinks most of the charge needed to charge up the switched capacitor. This ensures that the op amp will never see the transient nature of the load. This additional filter can also provide antialiasing.



For converters that have a differential input, a differential version of this circuit may be used, as shown in the figure below. Since one input is positive with respect to ground while the other is negative, one input (the negative one) needs to be supplied negative charge while the other needs to get rid of negative charge when the input capacitors are switched on line. Connecting a capacitor between the two inputs enables most of the charge that is needed by one input to be effectively supplied by the other input. This minimizes undesirable charge transfers to and from the analog ground.



APPENDIX

RSS addition of logarithmic quantities: The root-square sum of two rms signals, S_1 and S_2, has an rms value of $\sqrt{S_1^2 + S_2^2}$. One often needs to calculate the rss sum of two numbers that are expressed in dB relative a given reference. To do this one has to take the antilogs, perform the rss addition, then convert the result back to dB. These three operations can be combined into one convenient formula: If D_1 and D_2 are ratios expressed in dB [negative or positive] their sum, expressed in dB, is

$$10 \log_{10} (10^{D_1/10} + 10^{D_2/10})$$

Similarly, to find the difference between two rms quantities,

$$x = \sqrt{S_2^2 - S_1^2}$$

the result, x, expressed in dB, is

$$10 \log_{10} (10^{D_2/10} - 10^{D_1/10})$$

References (not available from Analog Devices):

[1]*Oversampling Delta-Sigma Data Converters—Theory, Design, and Simulation*, edited by J.C. Candy and G.C. Temes, IEEE Press, Piscataway, NJ, 1991.

[2]J. Vanderkooy and S.P. Lipshitz, "Resolution Below the Least Significant Bit in Digital Systems with Dither," *J. Audio Eng. Soc.*, vol. 32, pp. 106-113 (1984 Mar.); correction ibid., p.889 (1984 Nov.).

[3]A.H. Bowker and G.J. Lieberman, *Engineering Statistics*, Prentice Hall, Englewood Cliffs, NJ, 1972.

ANALOG DEVICES

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APPLICATION NOTE

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Using Sigma-Delta Converters–Part 2

This is a continuation of a discussion of sigma-delta converters begun in the last issue. We covered antialiasing requirements, idle tones, and loading on the signal source.

Q: What happens if my input signal is beyond the input range of the sigma-delta converter? I remember hearing something about the converter becoming unstable?

A: The modulator can become temporarily unstable if it is driven with inputs outside the recommended range. However, this instability is invisible to the user, since decimators are designed to simply clip the digital output and show either negative or positive full scale, just as one would expect with a conventional converter.

Q: The specifications for sigma-delta converters assume a certain input clock rate and therefore a specific sampling rate. Can I safely use the converter with a higher or lower clock frequency?

A: While the specs are measured at a particular sampling frequency, we often specify a range of input clock frequencies that the device can be operated with. This translates into a range of possible sampling rates. If you plan to go much beyond that range you can expect some performance degradation. If you sample at higher rates than specified, the internal switched-capacitor circuits may not be able to settle to the required accuracy before a new clock edge comes along. With too slow a sampling rate, capacitor leakage will degrade performance.

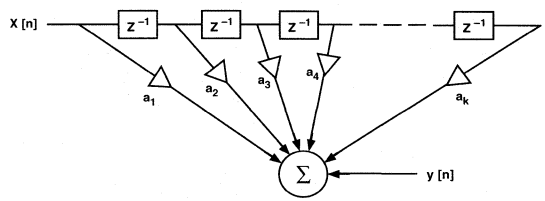
The digital filter characteristics of the converter (group delay, cutoff frequency, etc.) scale with sampling rate; so too do the input impedance (unless the input is buffered) and power consumption.

Q: I am planning to use a sigma-delta converter to digitize several signals by using a multiplexer at the input of the converter. Is that a problem?

A: While sigma-delta converters have a certain appeal due to their ease of antialiasing, they do not lend themselves well to applications for multiplexed ac signals. The reason for this is that the output of a sigma-delta converter is a function not only of the latest analog input but also of previous inputs. This is mostly due to the memory that the digital filter has of previous inputs, but the modulator has some memory as well. In a multiplexing application, after switching from one input to another, all information the filter has about the old input needs to be flushed out before the converter output word represents the new input.

Most decimation filters in sigma-delta converters intended for ac applications are FIR filters, principally because of their linear phase-response. For FIR filters, it is easy to calculate the time it takes to rid the filter of any information about the old input. The figure shows the structure of a FIR filter; the number of clock cycles required to clock all old data points out (i.e., the filter settling time) is equal to k, the number of taps in the filter. While data corresponding to a new input is propagating through the filter and replacing the earlier data, the output of the filter is calculated from a combination of the old data and the new data. The AD1879, for example, an 18-bit audio A/D converter, has a 4096-tap FIR filter which, when running at 3.072 MHz, has a 1.33-ms settling time.

The effective sampling rate for sigma-delta converters in multiplexed applications is quite low because of this need to wait for the old signal to be flushed out before capturing a valid data point for the new input. Traditional converters, which convert directly, or in a small number of stages, are therefore a much better choice in applications requiring the capture of multiple ac channels.



For a multichannel dc application where time is available to wait after switching between channels, or if the application does not require frequent changes between channels, the use of a sigma-delta converter can be very feasible. In fact, Analog Devices offers 16-24-bit converters with multiplexers on the input (AD771x family) specifically for such applications.

Q: Does this also explain why sigma-delta converters are not suitable for some control applications?

A: Yes. Since delays in control loops must be minimized for stability, sigma-delta converters are not suitable for control applications where they add a relatively long time delay. However, the actual delay is predictable; in applications that involve relatively slow signals, the converter phase delay, and therefore the effect on pole and zero locations of the control loop, may be negligible. However, even if this is the case, a traditional non-oversampling converter may still be a much better choice for the application, because a sigma-delta converter would need to run at a much faster sampling rate than a traditional converter in order to have the same phase delay. This will unnecessarily burden the circuitry that processes the A/D data.

Q: Are there any other issues I should be aware of when using sigma-delta converters?

A: In addition to the general guidelines on grounding, power supply bypassing, etc., that apply to all converters, there are a couple of points worth remembering when designing with sigma-delta converters. The first issue involves their input. As mentioned earlier, some sigma-delta converters (such as the AD1877) have buffers on the input; others (such as the AD1879), without a buffer, present a switched-capacitor load, which needs periodic current transients to charge the input capacitor. It is important that the circuitry driving the converter be as close to the converter as possible to minimize the inductance in the leads between the external circuitry and the switched-capacitor node. This reduces the settling time of the input and minimizes radiation from the input to other parts of the circuit board.

Another issue has to do with interference from clock signals affecting the A/D conversion. As I noted earlier, the digital decimation filter can't provide any filtering of signals whose frequencies are close to multiples of the modulator sampling rate. To be precise, the passbands are $[kF_{ms} \pm f_b]$s *where* k is an integer, F_{ms} is the modulator sampling rate, and f_b is the decimator cutoff frequency.

Besides the consequences for anti-aliasing discussed earlier, the decimator cutoff frequencies have a bearing on the selection of clock frequencies for devices that operate in the same system as the converter. These frequency bands (i.e., the passbands) embody the converter's greatest vulnerability to interference (inductive or capacitive coupling, power supply noise, etc.), because any signals in these frequency bands that manage to get into the modulator will not be subjected to attenuation in the filter. Therefore one is wise to avoid using clock frequencies that fall in these bands to minimize the possibility of interfering with the conversion—unless they are synchronous with the converter clock.

QUESTIONS ON NOISE IN CONVERTERS

Q: I recently evaluated a dual-supply A/D converter; one of the tests I did was to ground the input and look at the output codes on a LED register. To my big surprise I got a range of output codes instead of a single code output as I expected?

A: The cause is *circuit noise*. When the dc input is at the transition between two output codes, just a little circuit noise in even the finest dc converters will ensure that two codes will appear at the output. This is a fact of life in the converter world. In many instances, as in your case, the internal noise may be large enough to cause several output codes to appear. Consider, for example, a converter with peak-to-peak noise of just over 2 LSB. When the input of this converter is grounded, or a clean dc source is connected to the input, we will always see three—and sometimes even four—codes appear at the output. The circuit noise prevents the voltage being sampled from being confined to a voltage bin that corresponds to one digital code. Any external noise on the A/D input (including a noisy signal), on the power supplies, or on the control lines will add to the internal circuit noise—and possibly result in more bits toggling.

Q: Is there a way to determine how many codes I can expect to appear when I apply a dc signal to a converter?

A: It would not be hard in the ideal case where you knew the noise distribution, the exact size of the codes where the dc input is at and where within a code quantum the input lies (in the center, on the edge of two codes, etc.). But in reality you don't have this information. However, knowing some of the ac specifications (S/N, dynamic range, etc.) of the converter, you can make an *estimate*. From these specs you can find the magnitude of the rms converter noise relative to full scale. The noise will in all likelihood have a Gaussian amplitude distribution, so the standard deviation (sd) of the distribution equals the rms value. This also means that the codes that appear will not have equal probability of occurring. Using the fact that 99.7% of a Gaussian distribution occurs within ±3 standard deviations from the mean, we can estimate the peak-to-peak noise voltage at six times the standard deviation. If N_{rms} is the rms value of the converter noise and V_{LSB} is the size of the LSB in volts ($= V_{span}/2^b$) the peak to peak noise in terms of LSBs, N_B, is

$$N_B = \frac{6 \times N_{rms}}{V_{LSB}} = \frac{6 \times 2^b \times N_{rms}}{V_{\text{span}}}$$

In general, if the signal-to-noise ratio of a converter expresses noise power relative to full scale, we have

$$N_B = \frac{3}{\sqrt{2}} \times 2^b \times 10^{-\text{SNR}/20}$$

where b is the number of bits in the output word.

How many codes show up at the output depends where the mean of the input, i.e., the dc input value, is with respect to code transitions. If the mean is close to the boundary between two output codes, more codes are likely to appear than if the mean is half way between two output codes. It can easily be shown that N_C, the number of codes appearing for a particular value of N_B, is either INT(N_B)+1 or INT(N_B)+2, depending on the dc input value [INT(N_B) is the integer portion of N_B]. And don't be surprised to see even more codes from the less-probable noise amplitudes >±3 sd.

How many bits will N_C cause to toggle on the output? The number of bits needed to represent N_C codes is

$$\mathrm{INT}\left(\frac{\log N_C}{\log 2} + 0.5\right)$$

We can, however, see many more bits toggle, since the number of bits toggling is a function of the actual value of the converter's dc input. Consider, for example, that a one-code transition from an output word of –1 to 0 on a 2s-complement-coded converter involves inverting all the output bits.

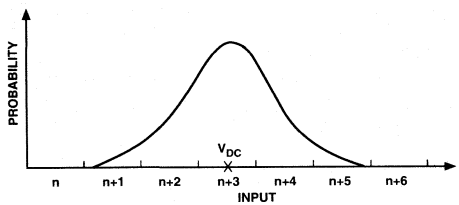
Lets look at an example using the AD1879, an 18-bit sigma-delta converter with dynamic range of 103 dB. From the definition of dynamic range we have

$$103 = 20\log\frac{S}{N_{rms}}$$

From the AD1879 data sheet, we find that the rms value of a full-scale input signal, S, is $6/\sqrt{2}$ V rms. This allows us to solve for N_{rms} which turns out to be 30 µV. We next find the LSB size by dividing the full input range by the number of possible output codes:

$$V_{LSB} = \frac{12}{2^{18}} = 45.8\,\mu\mathrm{V}$$

Thus N_B is 3.9. We can therefore expect either 4 or 5 different codes to appear at the AD1879 output when the input is grounded (ground corresponds to a midscale input for the AD1879).

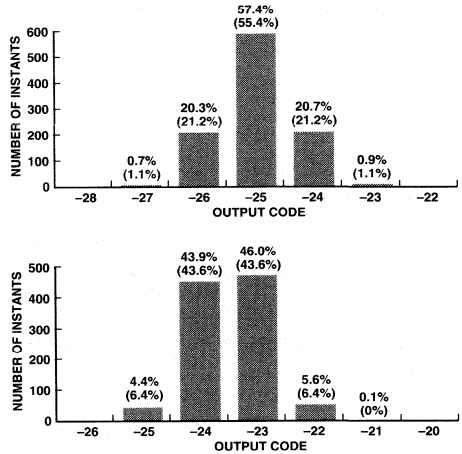


One can take this estimation one step further: If the standard deviation (the rms value) of a Gaussian distribution and the mean (the mean of the noise is 0 in this case) are known, one can use standard tables for the Gaussian distribution to calculate what percent of the time the noise will fall into a voltage interval corresponding to a specific output code. A histogram can be estimated, showing the distribution of codes at the output. Also the process can be reversed: a histogram showing the distribution of noise codes at a given value of dc output permits one to estimate the S/N ratio for a converter.

To make all this real, let's continue our example involving the AD1879. Consider two cases, one where the input lies midway between two output codes and one when the input is on the transition between two codes. From the calculations above, we found that the standard deviation (sd) of the noise (the rms value) was 30 µV. The size of one LSB in terms of sd is

$$\frac{45.78\,\mu\mathrm{V}}{30.0\,\mu\mathrm{V}} = 1.524$$

In the case where the dc input is midway between code transitions, as shown below, it is clear that any noise that falls within –0.5 LSBs to +0.5 LSBs from the input will result in the correct code at the A/D output. This corresponds to the noise being confined to a range of (–0.5 × 1.524) sd to (+0.5 × 1.524) sd from its mean (0). From standard tables one can find that the noise will fall in this range 55.4% of the time. If the noise falls within 0.5 LSBs to 1.5 LSBs, the output will be one code too high. Again from standard tables one can find that this will occur 21.2% of the time. Continuing in this manner one can calculate the whole histogram showing the distribution of output codes.



The upper figure shows an actual measurement where the dc input happened to be –25 LSBs. Five output codes, ranging from –27 to –23, appeared. 1024 measurements were taken and the percentage distribution of each code is shown on top of each column. The calculated distribution is listed in brackets on top of each column. As can be seen, the experimental results agree well with the calculated values. The lower figure shows a case where the dc input is close to the boundary between two codes. By following a similar procedure, one can calculate how the histogram should look. Again the experimental and calculated values are in excellent agreement. Note that the actual applied dc input is slightly above the border between the two codes, whereas the calculations assume it is exactly on the border.

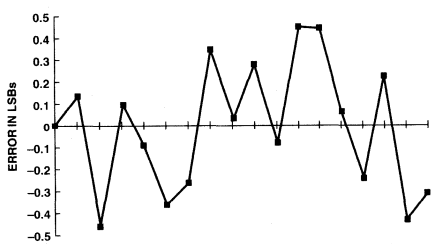
The biggest weakness of this estimating technique is the fact that in conventional converters the code width (the amount the dc input has to be increased to increase the digital output by one bit) varies from code to code. This means that if the dc input is in an area where codes are narrow, we can expect more bits to be toggling than in an area where the codes are wide. This method also assumes that the circuit noise within the converter stays constant, whether the applied signal is ac or dc. This is not exactly true in many cases.

The estimate will probably be more accurate when used with sigma-delta converters (except for "dead bands"), because neither of the two factors mentioned above is an issue in such converters.

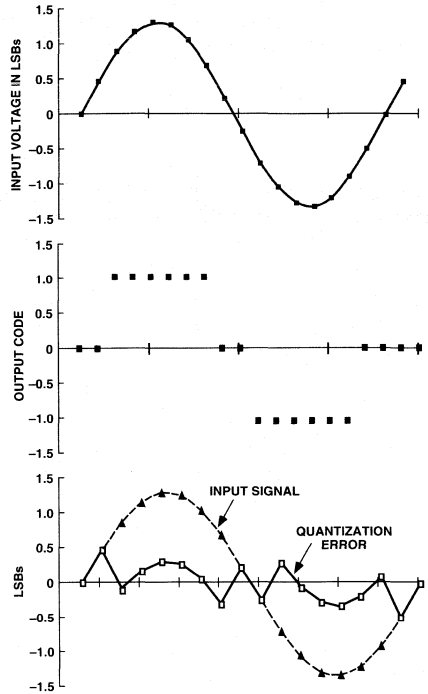
Q: Ah, now I understand why there are multiple codes at the output. But why not discard the bits that toggle and only bring out the bits that stay steady, since the others are really indeterminate? Isn't that the real resolution of the converter?

A: Many converters are designed for ac or dynamic applications where THD (total harmonic distortion) and THD+N (total harmonic distortion+noise) are the most important specs. The design therefore focuses on minimizing harmonic distortion for high- *and* low-level input signals, while keeping the noise to acceptable levels. As it turns out, these requirements somewhat contradict the requirements for a good dc converter, which is optimized for precision conversion of slow moving signals where harmonic distortion is not an issue. It is actually desirable to have some noise (called dither) superimposed on the input signal to minimize distortion at very low input signal levels; dither can also be used to improve dc accuracy where repeated measurements can be made.

To understand how this may be, let's start by looking at quantization noise. The output of an ideal A/D converter has finite accuracy because of the finite number of bits available to represent the input voltage. Each one of the 2^b quanta represents with one single value all values in the analog range from –0.5 LSB to +0.5 LSB of its nominal input value. The A/D output can therefore be thought of as a discrete version of the analog input plus an error signal (quantization noise). When a large and varying input signal (dozens, hundreds, or thousands of LSBs in amplitude) is applied to a converter, the quantization noise has very little correlation with the input signal. It is, in other words, approximately white noise. The figure shows the quantization noise of a perfect A/D converter at various instants of time when the input signal is a sinusoid of about 100 LSBs in amplitude.



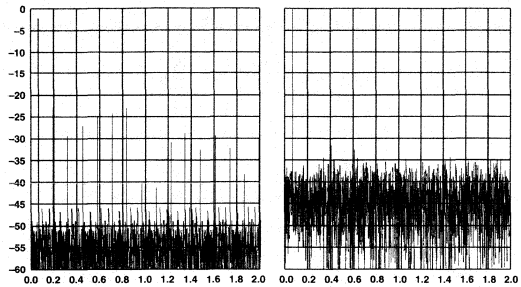
When the A/D input is very low in amplitude, so that the amplitude does not change more than a fraction of a LSB between samples, the samples stay in the same quantum, and are therefore constant for a few sample periods. This is depicted in the figure below, which shows a sinusoidal input signal that has an amplitude of only 1.5 LSBs, the A/D output and the quantization noise. Note that the quantization error follows the input waveform exactly while the samples are staying constant. The longer the samples stay constant, the more the quantization noise looks like the input waveform, i.e., the correlation between the input signal and the quantization noise increases. While the rms of the quantization error may not have changed, the quantization error will take on a non-uniform spectral shape. In fact, the correlated quantization noise shows up as harmonics in the A/D spectrum.



Another way to look at this phenomenon is to consider the case when the (sinusoidal) input signal is only around 1 LSB in size and the digital output resembles a square wave. Square waves are rich in harmonics! The harmonics, or noise modulation products, are very objectionable in many converter applications, especially audio.

To get around this problem, a technique called dithering is used to trade correlated quantization noise for white noise, which is less offensive to the human ear than correlated noise. Dithering is done by using circuit elements to *add* random noise to the input signal. While this will result in an increase of the total converter noise, the added noise breaks up the simple square wave patterns in the output code. The quantization error will not be a function of the input signal but of the instantaneous value of the dither noise. Thus the dither decorrelates the quantization noise and the input signal. The size of the dither signal is often about 1/3 LSB rms (2 LSBs peak-to-peak if the noise is Gaussian). Clearly, this will result in a converter that will have more than two codes at the output when the input is grounded. We saw an example earlier involving the AD1879 which had either four or five codes appear on the output depending on the dc input level.

The figure below shows the simulated output of an A/D converter with an undithered low level input signal. The quantization noise is a function of the input signal magnitude at the sample instant. This correlation between the quantization noise and the input signal shows up as a cluster of harmonically related sticks in the A/D output spectrum. Note that the magnitude scale in the figure is referenced to the input signal (not full scale input).



The right-hand figure shows the A/D output after a dither signal that is 4 dB above the quantization noise floor is added to the input. In this case the quantization noise depends on the magnitude of the dither signal at the instant when a sample is taken. Since the value of the dither doesn't depend on the input signal, the quantization noise becomes uncorrelated to the input and the harmonics in the A/D spectrum are eliminated, but at the cost of an overall increase in the noise floor.

Instead of actually adding noise to the A/D input, dithering can be accomplished by using the thermal noise of the converter as the dither signal and calculating enough output bits to ensure a decorrelated quantization noise.

Though I have used A/D converters in my examples, the idea of using dither also applies to D/A converters as well. Dither is applied to D/A converters by adding the output of a digital noise generator to the digital word sent to the D/A.

Q: *But in dc applications, I want to make an accurate measurement each time and may not be able to tolerate the uncertainty of having a few LSBs of error in a particular measurement.*

A: If you need n-bit dc accuracy in each conversion and you have problems finding a suitable n-bit converter, you have two options. One is to use an $(n+2)$-bit converter and simply ignore the two LSBs. However, if your hardware has the capability (and time) to do some signal processing, you can enhance the resolution of a noisy (dithered) dc converter and, in fact, get more than n-bit accuracy out of an n-bit converter if the accuracy is limited by noise.

To understand why this may be so, think of an ideal n-bit converter. For a particular value of dc input, you will get one digital code at the output. However, you do not know where the input lies within the code quantum (i.e., in the middle, close to the upper transition, etc.). That may be sufficiently accurate for your application, but if you add noise to the input of the converter—so that several codes can appear at the output—you will find that the code distribution contains information to place the dc value of the input more exactly.

In the earlier examples involving the AD1879, we saw how the code distribution looks when the input is in the vicinity of a code transition; the two most-frequent output codes are the ones on either side of the transition. Their average is therefore a good estimate of where the input lies. In fact, taking the average of a lot of conversions, while the input stays put, is an excellent way of enhancing the resolution of the converter. One has to be careful, when processing the converter output, to allow the output word length to grow without introducing roundoff errors. Otherwise one actually injects unwanted noise—called *requantization noise*—into the final output. Note that filtering out the noise is only just that; it will have no effect on other error sources of the converter, such as integral and differential nonlinearity.

This concept of resolution enhancement is an interesting one and is not restricted to the dc domain. One can actually trade resolution for bandwidth in the ac domain and combine the outputs of several converters or to construct a more-accurate output. The basic principle is that signal repetitions (which are self-correlated) add linearly, while repetitions of random noise produce root-square increases. Thus, a fourfold increase in number of samples increases S/N by 6 dB. Perhaps we can discuss useful applications of this principle in these pages in the future.

Q: *You mentioned a couple of converter ac specifications above. I am somewhat confused about how S/N, THD+N, THD, S/THD, S/THD+N, and dynamic range are measured on A/D and D/A converters and how they relate to each other. Can you shed any light on this?*

A: Your confusion is quite understandable. There is unfortunately no industry standard on exactly how these quantities are measured and therefore, what exactly they mean. Sometimes manufacturers are guilty of choosing the definition that portrays their part favorably.

Most often data sheets include a note on the testing conditions and how the different specs were calculated. The best advice I can give is to read these very carefully. By simple calculations you can often convert a specification for one part to a number that allows a fair comparison to a specification for another part.

Most specifications are not expressed in absolute units, but as relative measurements or ratios. Noise, for example, is not specified in rms volts, but as *SNR*, or the ratio between signal power and noise power under particular test conditions. These ratios are usually expressed in decibels, dB, and occasionally as percentages (%). A power ratio, x, expressed in bels, is defined as $\log_{10}x$; multiply by 10 if expressed in decibels (one tenth of a bel): $10 \log_{10}x$. *SNR* is therefore equal to $10 \log_{10}$ (signal power/noise power) dB. Evaluated in terms of rms voltage quantities, $SNR = 20 \log_{10}(V_{signal}/V_{noise})$.

Armed with this knowledge, let's see whether we can make sense out of the multiple specifications you mentioned above (many of which are redundant). Those specifications seek to describe how the imperfections of the converter affect the characteristics of an ac signal that gets processed by the converter. For dc applications, a listing of the magnitude of the actual imperfections suffices, but these can only suggest ac performance. For example, integral nonlinearity is a major factor in determining large-signal distortion (along with glitch energy for D/As) while differential nonlinearity governs small-signal distortion. To accurately determine the ac performance, at least two types of tests are performed in the case of A/Ds. The tests are as follows:

Full-scale sine (a)

A sinusoidal signal approaching full-scale is applied to the converter. The signal is large enough so that converter's imperfections cause significant harmonic components to occur at multiples of the input signal frequency. The harmonics will show up in the output spectrum, along with noise. A common performance measure is the relative magnitude of the harmonic components, usually expressed in dB. Relative to what? Two possibilities are the applied input signal and the full scale of the converter (which in most cases is different from the applied input signal). Referring the harmonics to full scale will clearly yield a lower (more attractive) number than referring them to the rms value of the actual input signal. This reference issue causes a lot of confusion when dynamic specifications are evaluated, because there is no universally accepted standard for what each performance measure should be referred to. The best advice I can give you is: never assume anything; read manufacturers' data sheets very carefully.

Sometimes the magnitudes of the individual harmonics are specified, but most often only the total harmonic distortion (THD) is specified. The THD measures the total power of the harmonics and is found by adding the individual harmonics in rss fashion. The formula then for *THD* when referred to the input signal is

$$20\log_{10}\left[\frac{\sqrt{\sum_{i=2}^{m} H^2(i)_{rms}}}{S}\right] \text{ or } 10\log_{10}\left[\frac{\sum_{i=2}^{m} H^2(i)_{rms}}{S^2}\right]$$

where $H(i)_{rms}$ refers to the rms value of ith harmonic component and S to the rms value of the input signal. Usually, harmonics 2 through 5 are sufficient. Note that the input-frequency, or *fundamental*, component is the first harmonic. To refer any harmonic to full scale, add x dB to the formula above, where x is the magnitude of the input signal relative to full scale. This simple conversion formula can be applied to other specifications, but take care to observe proper polarity of the log quantities.

Nowadays, clear distinction is usually made between total harmonic distortion plus noise (*THD+N*) and *THD*. This has not always been the case. *THD+N* includes not only the harmonics that are generated in the conversion, but also the noise. The formula for *THD+N* when referred to the input signal is:

$$20\log_{10}\left[\frac{\sqrt{N^2_{rms} + \sum_{i=2}^{m} H^2(i)_{rms}}}{S}\right]$$

or

$$10\log_{10}\left[\frac{N^2_{rms} + \sum_{i=2}^{m} H^2(i)_{rms}}{S^2}\right]$$

where N_{rms} is the rms value of the integrated noise in the bandwidth specified for the measurement.

Another commonly used specification is signal to noise-plus-distortion ($S/[N+D]$, or $S/[THD+N]$), also called *sinad*. This is essentially the inverse of *THD+N*, when referred to the signal; its dB number is the same, but with opposite polarity.

Another performance measure describing the test results is the signal to noise ratio, *S/N* or *SNR*, which is a measure of the relative noise power, most useful for estimating response to small signals in the absence of harmonics. If *S/N* is not specified, but *THD* and *THD+N* are provided, relative to the input signal, *THD* can be rss-subtracted from *THD+N* to obtain the noise to signal ratio [= $1/(S/N]$. If the numbers are given in dB, the rss subtraction formula for logarithmic quantities in the Appendix can be used as follows

$$SNR = -10\log_{10}\left(10^{(THD+N)/10} - 10^{THD/10}\right)$$

to yield the input signal power relative to noise power expressed in dB.

Low-level sine (b)

The second test usually performed is to apply a sinusoidal signal well below full scale to the converter (usually –60 dB). At this input level, sigma-delta converters usually exhibit negligible nonlinearities, so only noise (no harmonic components) appears in the spectrum. At this level, $S/N = S/N+D = -THD+N = -THD$, when all are referred to the same level. As a result, one specification indicating the noise level suffices to describe the result of this test. This specification called *dynamic range* (inversely, dynamic-range *distortion*), specifies the magnitude of the integrated noise (and harmonics if they exist) over a specific bandwidth relative to full scale, when a –60-dB input signal is applied to the converter.

Conventional (i.e. not sigma-delta) converters can exhibit harmonics in their output spectrum even with low-level input signals because all the codes may not have equal width (differential nonlinearity). In some such instances, the *S/N*, which ignores harmonics, measured with a –60-dB input signal, is different from dynamic range.

Frequently one sees *THD+N* at –60-dB and dynamic range specified for the same converter. These really are, as explained above, redundant since they only differ in the reference used. The only twist on dynamic range is that sometimes, when audio converters are specified, a filter that mimics the frequency response of the human ear is applied to the converter output. This processing of the converter output is called A-weighting (because an A-weighting filter is used); it will effectively decrease the noise floor, and therefore increase the signal-to-noise ratio, if the noise is white.

Everything discussed above applies to both A/D and D/A converters, with the possible exception of signal to noise ratio. Sometimes (particularly for audio D/A converters) *S/N* is a measure of how "quiet" the D/A output is when zero (midscale) code is sent to the converter. Under these conditions, the S/N expresses the analog noise power at the D/A output relative to full scale output.

It's important to note that the performance measures above are affected by: *bandwidth* of the measurement, the *sampling frequency*, and the input *signal frequency*. For a fair comparison of two converters, one has to make sure that these test conditions are similar for both.

Another Question

Q: I intend to use Analog's AD1800 family of audio D/A converters for a digital audio playback application. I understand that using an interpolator ahead of the D/A will make it easier to filter the D/A output, assuming I want to get rid of all the images at the D/A output. But is it really necessary to filter the output, since all the images will be above the audible range as long as sampling is at >40 kHz.

A: Good question. The audio equipment (audio amplifiers, equalizers, power amplifiers, etc.) that may eventually receive the output of your D/As are typically built to handle 20-Hz to 20-kHz signals. Since they are not intended to respond at frequencies much beyond 20 kHz—and in effect themselves function as filters—they may not have the necessary slew rate and gain to handle incoming signals from an unfiltered D/A output having significant energy well above 20 kHz. With their slew-rate and gain limitations, the amplifiers are driven into nonlinear regions, generating distortion. These distortion products are not limited to high frequencies but can affect the 20-Hz to 20-kHz range as well. Attenuating the high frequency signals at the DAC will therefore reduce the possibility of distortion. CD players often include filters steep enough to reduce the total out-of-band energy to >80 dB below full scale.

APPENDIX

RSS addition of logarithmic quantities: The root-square sum of two rms signals, S_1 and S_2, has an rms value of $\sqrt{S_1^2 + S_2^2}$. One often needs to calculate the rss sum of two numbers that are expressed in dB relative a given reference. To do this one has to take the antilogs, perform the rss addition, then convert the result back to dB. These three operations can be combined into one convenient formula: If D_1 and D_2 are ratios expressed in dB, their sum, expressed in dB, is

$$10 \log_{10}\left(10^{D_1/10} + 10^{D_2/10}\right)$$

Similarly, to find the difference between two rms quantities,

$$x = \sqrt{S_2^2 - S_1^2}$$

the result, x, expressed in dB, is

$$10 \log_{10}\left(10^{D_2/10} - 10^{D_1/10}\right)$$

References:

[1] *Oversampling Delta-Sigma Data Converters—Theory, Design, and Simulation*, edited by J.C. Candy and G.C. Temes, IEEE Press, Piscataway, NJ, 1991.

[2] J. Vanderkooy and S.P. Lipshitz, "Resolution Below the Least Significant Bit in Digital Systems with Dither," *J. Audio Eng. Soc.*, vol. 32, pp. 106-113 (1984 Mar.); correction ibid., p.889 (1984 Nov.).

[3] A.H. Bowker and G.J. Lieberman, *Engineering Statistics*, Prentice Hall, Englewood Cliffs, NJ, 1972.

ANALOG DEVICES

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APPLICATION NOTE

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Considerations for Selecting a DSP Processor (ADSP-2115 vs. TMS320C5x)

INTRODUCTION

Digital signal processing systems demand high performance processors. But high performance cannot be measured by a processor's multiplication/accumulation speed or MIPS (Millions of instructions per second) rating alone. Many times a DSP processor is characterized mainly by its MIPS rate. Since the instruction of one DSP device is not necessarily equivalent to that of another DSP device, a MIPS rating can be misleading. Other architectural and performance requirements relating to a DSP processor's capabilities in areas such as arithmetic, addressing and program sequencing may be more important. What distinguishes DSPs from other types of microprocessor and microcontroller architectures is how well they perform in each of the following areas.

1. Fast and flexible arithmetic
   A DSP processor must provide single-cycle computation for multiplication, multiplication with accumulation, arbitrary amounts of shifting, and standard arithmetic and logical operations. In addition, the arithmetic units should allow for any sequence of computation so that a given DSP algorithm can be executed without being reformulated.
2. Extended dynamic range on multiplication/accumulation
   Extended sums-of-products are fundamental to DSP algorithms. Protection against overflow in successive accumulations ensures that no loss of data or range occurs.
3. Single-cycle fetch of two operands (from either on- or off-chip)
   Again, in extended sums-of-products calculations, two operands are always needed to feed the calculation. A processor must be able to sustain two operand data throughput. Also, flexible addressing capabilities for multiple data memories is important.
4. Hardware circular buffering (both on- and off-chip)
   A large class of DSP algorithms including most filters require circular buffers. Hardware to handle address pointer wraparound or modulo addressing reduces overhead (increasing performance) and simplifies implementation.
5. Zero overhead looping and branching
   DSP algorithms are naturally repetitive and can easily be expressed as loops. Program sequencing that supports looped code with zero overhead provides the best performance and the easiest programming implementation. Likewise, overhead penalties for conditional program flow are unacceptable in signal processing applications.

Not all processors currently used for DSP and DSP-like functions meet these architectural and performance requirements equally well. This article examines these considerations for selecting a DSP processor, comparing two 16-bit fixed-point processors, the ADSP-2115 from Analog Devices and the TMS320C5x from Texas Instruments.

The three sections that follow discuss the five points above. The arithmetic section discusses items one and two, the addressing capabilities sections discusses items three and four and the program sequencing section discusses item five.

Program examples and benchmarks can be found at the end of this article.

ARITHMETIC CAPABILITIES

The basis of a successful DSP implementation is the ability to perform fast math. Arithmetic capabilities are the foundation of DSP performance.

General Purpose Math

One indicator of a good arithmetic architecture is the ability to perform a wide range of arithmetic computations. These computations should be handled in a

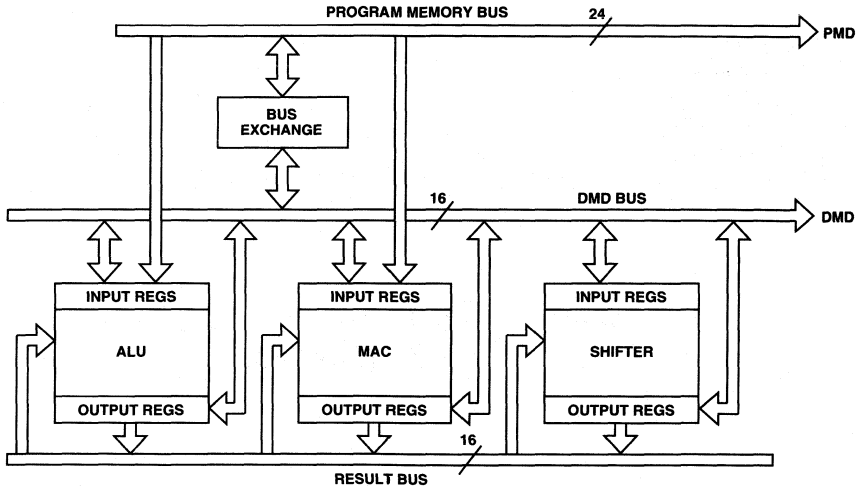


Figure 1. Block Diagram of Arithmetic Section of the ADSP-2115

flexible manner so that the algorithm can be implemented without rearranging the order of the arithmetic operations or operands. If the arithmetic architecture is fixed, too special-purpose or limited and the algorithm must be rearranged, this poses extra work for the DSP designer or programmer and delays getting a system running. Algorithm development frequently turns out to be much of the work of implementing a DSP system. If an algorithm can be used "as is" with no extra work, the design can be finished sooner and with less chance of error.

Arithmetic Architecture

Figure 1 shows a block diagram of the arithmetic section of the ADSP-2115 while Figure 2 shows that of the TMS320C50. Both of these devices utilize a modified Harvard architecture which can feed data operands from both program memory and data memory to the arithmetic section. Both of these devices work with 16-bit numbers.

ADSP-2115 Arithmetic Architecture Overview

The ADSP-2115 has three independent computational units: an ALU, a multiplier/accumulator (MAC), and a barrel shifter. They are connected (via the Result bus) so that the output register of any arithmetic unit may be operated on directly as an input by any other unit. In addition, the ALU and MAC are directly connected to both the program and data memory buses. Operands for ALU and MAC operations can come from both memories or any combination of off-chip memory and other data registers in the processor. All arithmetic operations are register based and a group of registers surrounds each arithmetic unit. A primary and secondary bank of registers is available to provide for fast context switching. All arithmetic registers can also be used as general purpose data registers.

TMS320C5x Arithmetic Architecture Overview

Figure 2 shows the block diagram of the arithmetic section of the TMS320C50. The TMS320C50 contains a multiplier, an ALU, a Parallel Logic Unit (PLU), a 16-bit scaling shifter and additional shifters at the outputs of both the accumulator and multiplier. The multiplier has an input register, TREG0, and an output register, PREG. The multiplier has direct input connections to both the program and data bus only for one operand or input. The ALU has direct access to only the data bus, not the program bus. Results are always sent to either the data bus or the accumulator registers. In some cases, the result must first be stored back in data memory before it can be used as an input for another calculation. Operations such as adding two data values from memory or multiply/accumulating with a data value can require multiple cycles.

With the TMS320C50, there is no dedicated multiplier/accumulator (MAC), which is required in many DSP algorithms. Instead the ALU must be used in conjunction with the multiplier for MAC operations. This may require some rearrangement of the algorithm or the temporary storage of intermediate results in data memory if the algorithm requires MAC operations interleaved with ALU operations. Also, there are arithmetic pipeline delays that are required to achieve sustained MAC operations. Basic multiply and ALU operations require multiple cycles as opposed to the single cycle operation of the arithmetic units in the ADSP-2115.

The availability of general purpose data registers and the flexibility of data movement in the TMS320C50 is limited. This may result in data bottlenecks and in extra cycles being required to move data into the right position prior to an arithmetic operation.

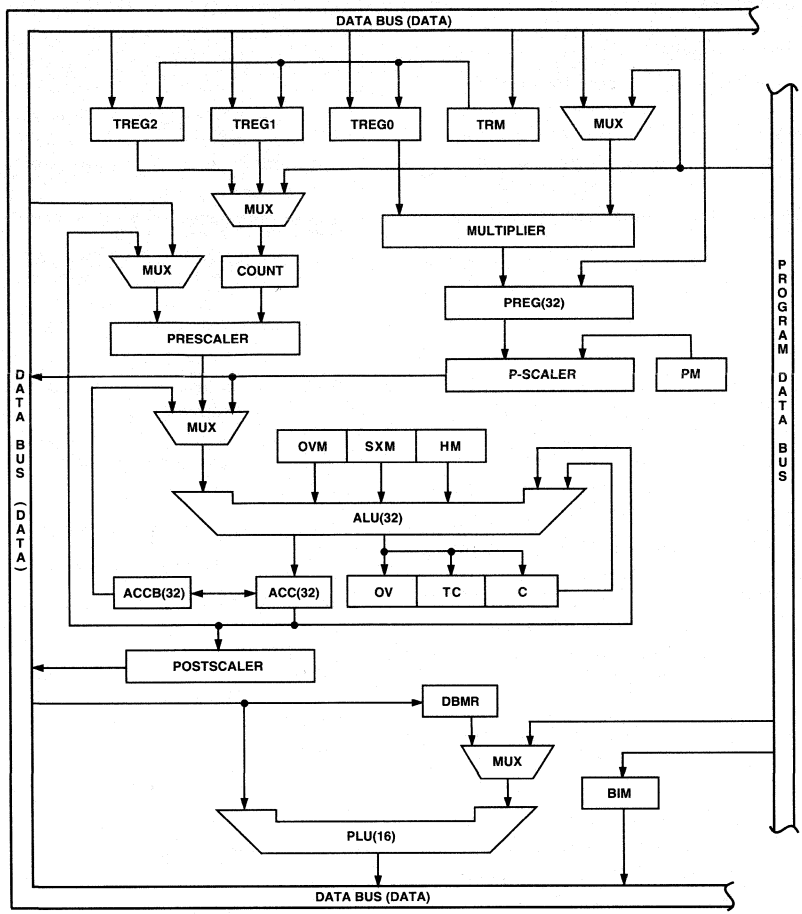


Figure 2. Block Diagram of Arithmetic Section of the TMS320C50

ADSP-2115 ALU

The ALU has two X and two Y input registers: AX0, AX1, and AY0, AY1. ALU operations are performed on any X-Y assortment of these input registers. They may be loaded from any combination of program and data memory or other data registers in the processor. The result of the operation appears in the ALU result (AR) or ALU feedback (AF) register. AR and AF can also be used as the X and Y operands (respectively) in any ALU calculation. The result registers of the MAC and barrel shifter can also be used directly as X inputs to the ALU (and vice versa).

ALU instructions are coded in a register transfer, algebraic syntax. An example of addition is shown below. This example is a multifunction instruction. The first "clause" of the instruction (up to the first comma) is the addition operation. The second clause loads the X input register from data memory ("DM") and the third clause loads the Y input from program memory. An addition (or any other ALU operation) can be executed on a sustained, single-cycle basis. (These operand fetching clauses of the instruction may be omitted, if they are not needed.)

```
AR=AX0+AY1,AX0=DM(I0,M0),AY1=PM(I4,M4)
```

All ALU operations complete in a single 50 ns cycle. (All references to cycles for the ADSP-2115 assume a 20 MHz device.) The ADSP-2115 runs at full speed even with an off-chip memory access.

TMS320C50 ALU

ALU operations require that one operand must come from the accumulator while the other comes from either the multiplier output, the accumulator buffer, or from the data bus or accumulator through a shifter. To add two numbers, the accumulator must be loaded with the first data value. After the accumulator is loaded, a second number can be added to the accumulator. The instructions for the ALU are specified with a mnemonic. The two instructions required to add two numbers are shown on the following page.

```
ZALR    <data memory address>

ADD     <data memory address>
```

For the result to be used as an input value for anything other than another ALU operation, the data must first be stored back into data memory from the accumulator. Not all ALU operations can be performed in a single 35 ns cycle; an add as shown above can be accomplished every two cycles. All references to TMS320C50 cycles assume a 28.57 MHz device with a 35 ns cycle time. Not all ALU instructions (i.e., ADD #k, SUB #k, ADD #lk, SUB #lk, ADRK) can be used with the repeat feature.

ADSP-2115 MAC

As shown in Figure 1, the ADSP-2115 multiplier/accumulator (MAC) sits next to the ALU. Like the ALU, it has two X and two Y input registers, MX0, MX1 and MY0, MY1. The unit performs both multiplications and MACs independent of the ALU. This is a key difference from the architecture of the TMS320C50.

MAC operations are performed on any X-Y assortment of input registers. They may be loaded from any combination of program and data memory or other data registers in the processor. The result of the operation appears in the MAC result register (MR) or the MAC feedback register (MF). Like the ALU, the feedback and result registers can also serve as the X and Y inputs for any multiplication or MAC operation. The result registers of the barrel shifter and ALU can also be used directly as X inputs to the MAC (and vice versa).

The instructions for the MAC are specified in a register transfer, algebraic syntax. An example is shown below. The first line shows multiplication of two signed operands and the second example shows multiplication with accumulation of one signed and one unsigned operand. (Signed and unsigned operands can be mixed in any combination.)

The second example is a multifunction instruction. The first "clause" of the instruction (up to the first comma) is the MAC operation. The second clause loads the X input register from data memory (DM) and the third clause loads the Y input from program memory. Any MAC operation can be executed on a sustained, single-cycle basis. (These operand fetching clauses of the instruction may be omitted, if they are not needed, as in the first example.)

```
MR=MX0*MY0 (SS)

MR=MR+MX1*MY1(SU), MX1=DM(I0,M0), MY1=PM(I4,M4)
```

The MR (MAC result) register is actually a 40-bit accumulator. It is divided into two 16-bit pieces (MR0 and MR1) and an 8-bit overflow register (MR2). DSP applications frequently deal with numbers over a large dynamic range. The eight "overflow" bits of MR2 allow for 256 MAC overflows before a loss of data can occur. The MAC also supports multiprecision operations as well as automatic unbiased rounding.

All multiplication and MAC operations execute in a single 50 ns cycle. (Please consult an *ADSP-21xx Data Sheet* for the most recent specifications.) Two new operands can be loaded into the input registers in parallel with the computation so that a new MAC operation with new operands can be started every cycle. The ADSP-2115 runs at full speed even with an off-chip memory access.

TMS320C50 MAC Operation

There is no dedicated multiplier/accumulator hardware in the TMS320C50. The TMS320C50 requires the use of both the multiplier and the ALU to perform a complete multiplication/accumulation operation. A multiplication is performed by loading the TREG0 register with the first operand. Once this data is loaded, a value from the data bus can be multiplied with the value in the TREG0 register. The instructions for the multiplier are specified with a mnemonic. The instructions for a multiplication are shown below.

```
LT      <data memory address>

MPY     <data memory address>
```

A product is obtained every two cycles.

A full multiplication/accumulation requires the use of the ALU as well as the multiplier. The instruction required to perform a MAC operation is shown below. This instruction requires two words of program memory storage.

```
MAC     <prog. mem. address> <data mem. address>
```

With both operands in on-chip memory, the MAC instruction takes three 35 ns cycles in non-repeat mode. In repeat mode, it will require $2 + n$ cycles, where n is the number of repeats.

There are four different mnemonics used for the multiply/accumulate function: MAC, MACD, MADD, MADS. The specific use of each of these depends upon the source of the data. For a dual operand fetch, such as that needed for a digital filter, the MADD instruction should be used. The DMOV portion of the MADD instruction will not function with external memory. All data must reside on chip.

The TMS320C50 provides one bit of extension in the accumulator (a 31-bit accumulator with an overflow bit compared to the 40-bit accumulator of the ADSP-2115). After more than one overflow, the calculation of the TMS320C50 is corrupted. Automatic rounding is not supported in the multiplier. This is unlike the ADSP-2115, where up to 256 overflows can occur with no lost data and automatic rounding is performed in the same cycle as the multiply operation.

ADSP-2115 Shifter

The barrel shifter in the ADSP-2115 has an input register, SI, and accepts as inputs any result registers in the processor (e.g., MR1, AR) including its own result register,

Table I. Summary of Arithmetic Capabilities

DSP Requirement	ADSP-2115	TMS320C50
All ALU Operations—Single Cycle	✓	No
Single-Cycle Multiplication	✓	No
Single-Cycle MAC Operations	✓	✓*
Single-Cycle Shifting	0–32 Bits Left or Right	0–16 Bits Left or Right 0–7 Bits Left 1 or 4 Bits Left 6 Bits Right
Accumulator Overflow Protection	8 Bits	1 Bit
Signed, Unsigned or Mixed-Mode Multiplications	✓	No Mixed Mode
Single-Cycle Normalization	✓	No

*Approaches single-cycle efficiency when using repeat mode.

SR. Like the MAC result register set, the 32-bit SR is divided into two 16-bit registers, SR0 and SR1. The shifter also has an exponent register, SE, which is set automatically by the exponent adjust instructions and used for normalization instructions.

The shifter can place a 16-bit input value anywhere within a 32-bit field in a single cycle. The input can be shifted any number of bits from off-scale left to off-scale right with either an arithmetic or logical shift. Other functions such as exponent detection, normalization, denormalization, block floating-point exponent maintenance, and pattern merging can also be performed with this shifter. All shifter operations are performed in a single cycle. Numbers can be normalized, regardless of the number of bits to be shifted, in a single cycle.

TMS320C50 Shifter

The TMS320C50 has three scaling shifters. The P-scaler shifts the product 0, 1, or 4 bits to the left or 6 bits to the right. The prescaler at the input of the ALU shifts data to the left or right from 0 to 16 bits. The post-scaler at the output of the ALU can shift data coming from the accumulator left from 0 to 7 bits. These shifters add the advantage of being able to scale data during the data move instead of requiring an additional shifter operation but limit the flexibility for general purpose shifting operations.

Arithmetic Summary

Table I summarizes the comparison of arithmetic capabilities of these processors.

The side-by-side arithmetic architecture of the ADSP-2115 results in easier implementation of many DSP algorithms as compared to the fixed sequence, end-to-end architecture of the TMS320C50. Due to the dependency of the ALU on the multiplier for multiplication/accumulations in the TMS320C50, MAC operations cannot be easily intermingled with ALU operations. This may require changing the order of calculations in an algorithm so that the interdependency of ALU and multiplier does not cause a problem. The local storage registers found in the ADSP-2115 make data movement for calculations easy. If data is to be used many times, it can reside in a register to eliminate the need of fetching it from memory each time. With local registers and the open architecture, it is easy to perform arithmetic operations in any order and to guarantee that input operands and results remain intact until explicitly overwritten or moved.

6

DATA ADDRESSING CAPABILITIES

A digital signal processor's ability to perform fast arithmetic is wasted if the required data cannot be fetched at sustained speed equal to the processing rate. Addressing hardware must support the dual operand fetches required to fully utilize the Harvard architecture found in most DSPs. A good DSP must have the ability to store two types of data operands, typically a coefficient and a data word. Maximum efficiency can be obtained if two different memory spaces are provided for the data operands so that two operands can be fetched in the same single cycle. Using both data memory and program memory to store data will allow maximum efficiency. Circular buffers are frequently useful in implementing DSP algorithms; hardware support of address pointer wraparound is another feature distinguishing a signal processor from other types of high-performance processors.

Figure 3 shows the address generation circuitry of the ADSP-2115 while Figure 4 shows that of the TMS320C50. The addressing capabilities of the TMS320C50 are basically the same as those of the TMS320C25 with the addition of some circular buffering logic. Flexibility is still limited since there is only one modify register (AR0) and only two simultaneous circular buffers are supported compared to the eight modify registers and eight simultaneous circular buffers of the ADSP-2115. Also, due to instruction pipelining of the TMS320C50, the auxiliary registers cannot be used for as many as two cycles after certain register load instructions. These addressing

limitations and restrictions of the TMS320C50 can present severe penalties in data addressing efficiency for DSP algorithms and can result in data bottlenecks and slower execution of DSP code.

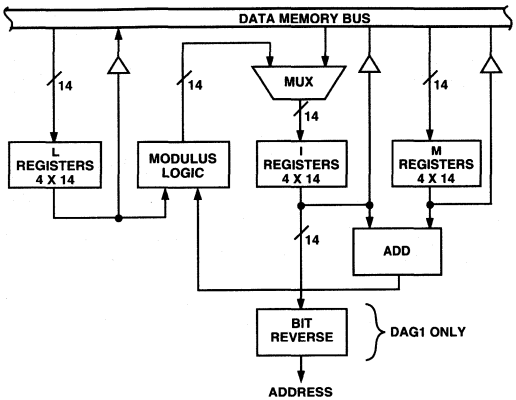


Figure 3. Block Diagram of ADSP-2115 Data Address Generators

ADSP-2115 Addressing

There are two independent address generators in the ADSP-2115. One typically supplies addresses for program memory data fetches while the other handles data memory, making efficient use of the modified Harvard architecture. Each address generator has four I (index) registers which store pointers (addresses), four M (modify) registers for address modifiers, and four L (length) registers storing buffer lengths for modulo addressing of circular buffers.

The address generator can bit-reverse an address as it is sent out to the address bus for zero-overhead bit-reversing for the FFT. The I, M, and L registers can be also used for general purpose data storage.

The address generators can also be used in conjunction with the serial ports to provide an automatic data buffering function. As data words come in or go out the serial port, data buffer addressing is automatically maintained and an interrupt is generated when the buffer is full or empty. This minimizes interrupt handling for serial port data transfers.

ADSP-2115 Indirect Addressing

With indirect addressing, the address in an I register drives either the data or program memory address bus. While the memory is being accessed, the address is simultaneously updated with the contents of any of the modify (M) registers, as shown in Figure 3. The specific pairing of I and M registers is up to the programmer. For example, I0 and M3 could be specified in the instruction as in

```
AX0=DM(I0,M3);     {load AX0 from Data Memory
                    and modify I0 by M3}
```

The ability to mix I registers and M registers is especially useful for two-dimensional addressing or for supporting pointer increment and decrement without constantly reloading a new modify value. This instruction syntax shows explicitly what registers are used to generate the address and where the data is going; nothing has to be inferred.

Loading the length of a circular buffer into the L register activates the modulus logic, guaranteeing that the address is kept inside the buffer in a modulo fashion. This

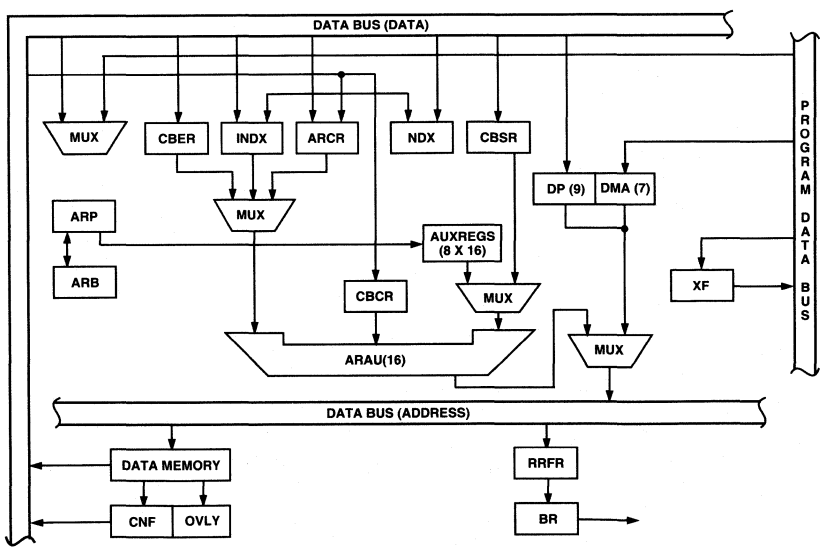


Figure 4. Block Diagram of TMS320C50 Address Generation Circuit

is maintained automatically by the address generator hardware and does not have to be calculated explicitly by the programmer. Circular buffers, such as for the delay lines of digital filters, are both transparent and require zero-overhead. Circular buffering is automatically maintained regardless of the modify value used.

ADSP-2115 Direct Addressing
Due to the 24-bit width of the ADSP-2115 instruction, a full 14-bit address can be specified within a (single-word) instruction for single-cycle access to any data. Below is an example of an instruction using direct addressing to read from data memory.

```
MX0 = DM(some_label);
```

ADSP-2115 Circular Buffering
Circular buffering is supported in hardware by the address generators of the ADSP-2115. Each address generator can maintain four simultaneous circular buffers for a total of eight. Circular buffers can be placed in either data or program memory. The length register (L registers) is simply loaded with the length of the circular buffer. The modulus logic detects when the pointer (updated index register value) has reached or exceeded the end of the buffer boundary. Operation is supported for going forwards or backwards through the buffer. The step size can be of any value that is less than the full buffer length. For applications such as interpolation filters, where the step size is equal to the interpolation factor, zero-overhead circular buffer operation is maintained.

TMS320C50 Addressing
The auxiliary register file of the TMS320C50 is used for storage of addresses and a single modifier. Only one address can be supplied at a time with the auxiliary register file so that two general purpose, indirect addressed data fetches cannot be achieved in a single cycle.

TMS320C50 Indirect Addressing
The auxiliary register file is connected to an arithmetic unit which will auto-index the contents of the auxiliary register or modify a register by the contents of auxiliary register number 0. The TMS320C50 has a single modify register. This limits the addressing capabilities for indirect addressing. Limited support is provided for circular modulo addressing; this diminishes the performance of DSP algorithms using circular buffers. Automatic circular buffering is only supported for increment and decrement address modifications. Modify values greater than 1 will not work.

TMS320C50 Direct Addressing
The TMS320C50 can directly access data within a 128-word block (compared to a 16K word block with the ADSP-2115). A 9-bit data page register is used in conjunction with the direct address to access a larger data space. To access data within a different block requires software overhead to update the 9-bit data page register. The update of the page register poses the requirement on the programmer to detect when the page boundary has been exceeded and when it is necessary to update the page register.

TMS320C50 Circular Buffering
Two circular buffers can be maintained by hardware in the address generation circuitry. A register (CBSR) is used to hold the start address of the circular buffer and a register (CBER) is used to hold the end address of the circular buffer. Since the auxiliary registers are used for pointers into the circular buffer, circular buffers in program memory (coefficients) are not possible. The circular buffer logic in the TMS320C50 checks only for a pointer equal to the end address, it does not check for a pointer that has skipped over the end address (i.e., using a step size greater than 1). For applications which require a step size greater than 1, such as interpolation filters, additional code (APL and OPL instructions) is

Table II. Summary of Data Addressing Capabilities

DSP Requirement	ADSP-2115	TMS320C50
Single-Cycle Fetch of Two Operands from On-Chip	✓	No
Single-Cycle MAC Operations	✓	✓*
Modify Two Addresses by Two Different Modify Values on Every Cycle	✓	No
Bit-Reverse Data Memory Addresses for FFT	✓	✓
Automatic Pointer Wraparound for Circular Buffers	✓	✓**
Automatic Circular Modulo Addressing	✓	No

*MAC, MACD, MADD and MADS instructions only.
**For step size of 1 only, and cannot be used for program memory.

needed to monitor the value of the pointer. This requires several cycles of overhead for each data word addressed. Also, the maximum circular buffer length supported by the TMS320C50 is 256, thus limiting the size of digital filters that can be used.

TMS320C50 Addressing Instructions

The instruction mnemonics of the TMS320C50 involve several addressing modes. Indirect and direct addressing is specified within arithmetic instructions and, depending upon the memory configuration, can impose several overhead cycles (overhead can be as high as eight cycles with external memory). Some general syntax examples are shown below.

```
ADD {*|*+|*-|*0+|*0-|*BRO+|*BRO-} [,<next ARP>]

MPY {*|*+|*-|*0+|*0-|*BRO+|*BRO-} [,<next ARP>]
```

Specific examples of these are shown below.

```
ADD    *

MPY    *0+
```

The first example uses the contents of an auxiliary register as the address and the second uses the contents of an auxiliary register as the address and adds the contents of auxiliary register 0 as a modifier. This instruction syntax can be hard to decipher because it does not directly name which auxiliary register is being used. That information is stored in the auxiliary register pointer (ARP).

The address generator can bit-reverse an address as it is sent out to the address bus for zero-overhead bit-reversing for the FFT. Auxiliary registers can also be used for general purpose data storage and the auxiliary ALU can be used for limited math.

ADDRESS GENERATION SUMMARY

Sustaining high rates of arithmetic operations demands maximum performance from the data addressing part of a processor's architecture. Table II summarizes the differences between the two processors in terms of their data addressing capabilities.

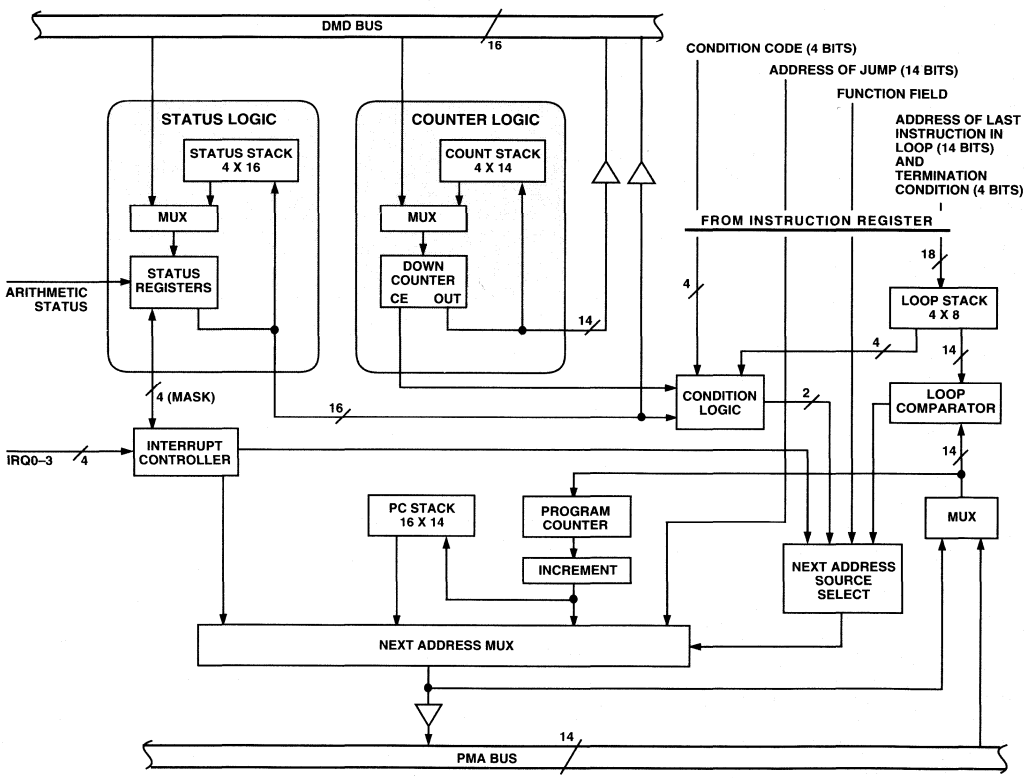


Figure 5. Block Diagram of the Program Sequencer of the ADSP-2115

PROGRAM SEQUENCING CAPABILITIES

Efficient architectures for signal processing require fast arithmetic capabilities and matching speed in data addressing and fetching capabilities. To fully deliver the performance required for real-world signal processing, a DSP machine must execute its program with little or no overhead spent on maintaining the proper flow of control.

Efficiency in program sequencing has many different aspects; they cannot all be covered in this article. The comparison focuses primarily on two features

- the execution of loops and
- how branching and branching on conditions are handled.

Loops are fundamental to the way DSP algorithms are expressed in their natural mathematical form. Operations such as sums-of-products are repetitive. If the program can be efficiently expressed in a looped form, then coding is quite straight forward and changing the program (for example, to increase the number of taps in a filter) requires very little work.

Branching is fundamental to program structure. Branching on conditions (and executing arithmetic on conditions) is a natural way to construct any program which must respond to its environment.

Program Sequencer Architecture

Figure 5 shows the architecture of the program sequencer of the ADSP-2115 and Figure 6 shows that of the TMS320C50.

ADSP-2115 Program Sequencer

The program sequencer of the ADSP-2115 contains logic that selects a program memory address source and routes the address to the program memory address bus (PMA). This address selection occurs automatically in response to the current instruction. The address placed on the address bus can come from

- the program counter (for sequential addressing),
- a 14-bit address in the instruction word itself, for direct jumps and subroutine calls,
- the PC stack, for returns from subroutines and interrupts, and
- the interrupt logic, to automatically vector to the interrupt routine upon assertion of any external interrupt.

All instructions execute in a single cycle; this applies equally to jumps, calls and interrupts. No instruction pipelining is required in the ADSP-2115 so that program flow is simple to understand.

When an interrupt occurs, the complete status of the processor (stack status, mode status, arithmetic status and interrupt mask) is automatically pushed onto the status stack as part of the interrupt vector process.

ADSP-2115 Looping Capabilities

The ADSP-2115 program sequencer supports zero-overhead "DO UNTIL" loops. Using the count stack, loop stack and loop comparator, the processor can determine whether a loop should terminate and address the next instruction (either the top of the loop or the instruction after the loop) with no overhead cycle.

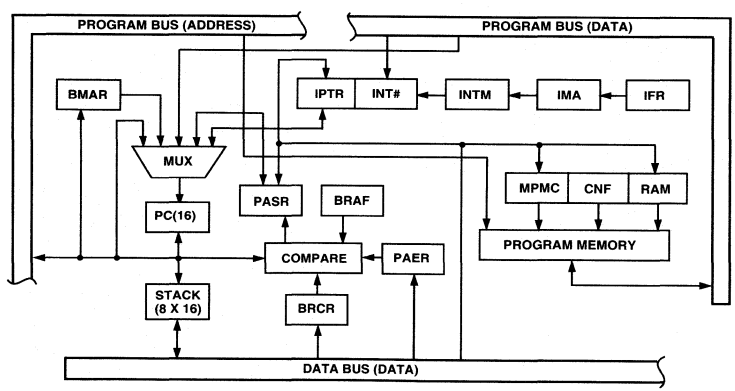


Figure 6. Block Diagram of the TMS320C50 Program Sequencer Circuit

A DO UNTIL loop may be as large as program memory size permits, or as small as one instruction. A loop may terminate when a 14-bit counter expires or when any arithmetic condition occurs. The example below shows a three instruction loop that is to be repeated 100 times.

```
        CNTR = 100;
        DO Label UNTIL CE;
            First instruction of loop;
            Second instruction of loop;
Label:  Last instruction of loop;
        First instruction outside loop;
```

The first instruction loads the counter with 100. The DO UNTIL instruction contains the address of the last instruction in the loop (in this case the address represented by the identifier, *Label*) and also contains the termination condition (in this case the count expiring, CE). The execution of the DO UNTIL instruction causes the address of the first instruction of the loop to be pushed on the PC stack and the address of the last instruction of the loop to be pushed on the loop stack. (See Figure 5.)

As instruction addresses are output to the program memory address bus and the instruction is fetched, the loop comparator checks to see if the instruction is the last instruction of the loop. If it is, the program sequencer checks the status and condition logic to see if the termination condition is satisfied. The program sequencer then either takes the address from the PC stack (to go back to the top of the loop) or simply increments the PC (to go to the first instruction outside the loop).

The looping mechanism of the ADSP-2115 is automatic and transparent to the user. As long as the DO UNTIL instruction is specified, all stack and counter maintenance and program flow is handled by the sequencer logic with no overhead. This means that in one cycle the last instruction of the loop is being executed and in the very next cycle, the first instruction of the loop is executed or the first instruction outside the loop is executed, depending upon whether the loop terminated or not.

The ADSP-2115 can support four levels of nesting for loops. DSP routines such as matrix operations and two-dimensional processing, as well as more common algorithms such as the FFT, benefit from nested looping capabilities.

ADSP-2115 Program Sequencer Instructions

There are many conditional instructions for the ADSP-2115. Most arithmetic instructions as well as jumps, subroutine calls, returns from interrupts and returns from subroutines may all be conditional. The program sequencer decides on the fly whether the condition is true and what action to take, requiring zero overhead cycles.

The coding of conditional jumps, subroutine calls and returns is straightforward. Some examples of the syntax are shown below.

```
IF condition JUMP label;
IF condition JUMP I4;
IF condition CALL label;
IF condition CALL I4;
IF condition RTS;
IF condition RTI;
```

In the above examples, I4 references an address generator register for indirect branching. *Condition* refers to any of a set of 16 arithmetic conditions in the processor and *label* refers to any address or label in the program memory space.

TMS320C5x Program Sequencer

The program sequencer logic of the TMS320C5x controls instruction execution and consists of a program counter, stack and related hardware. Figure 6 illustrates the logic used for program sequencing.

Hardware looping on the C52 is supported by the RPT (single instruction repeat) and the RPTB (multiple instruction repeat) instructions, which can execute a loop up to 65,536 times. These loops however are not interruptible. And though the RPT instruction can be nested within an RPTB, to nest an RPTB instruction within an RPBT instruction takes about 14 instructions of overhead for saving and restoring control registers. Due to the limitations of instruction pipelining, the minimum size of a loop used with a block repeat is three instructions. A two instruction zero-overhead loop is not possible.

A loop is maintained automatically but since there are no local stacks or storage for loop count, top of loop address and bottom of loop address, there is no easy way to have nested loops. Logic is also included to repeat a single instruction as many as 256 times.

Instruction execution for the TMS320C50 utilizes a four-level pipeline consisting of a prefetch, decode, operand fetch, and execution stage. The four level pipeline imposes certain restrictions and extra cycles of overhead with operations such as loading data into registers, looping, branching, and executing certain instructions after other instructions. The ADSP-2115 has no such restrictions because it does not need the extra instruction pipelining to achieve its fast speed.

Anytime the flow of the program deviates from sequential instruction fetches, the instruction pipeline must be emptied and then refilled based on the destination address of the branch, call or interrupt vector. These types of operations require at least three cycles to execute when fetching the instruction from external memory or from internal program ROM. This type of instruction pipelining is not found in the ADSP-2115 (the fast instruction execution speed is achieved by other design

Table III. Summary of Program Sequencing Capabilities

DSP Requirement	ADSP-2115	TMS320C50
PC Stack Depth	16	8
Nested Looping	4 Levels	No
Conditional Arithmetic Instructions	✓	No
Zero-Overhead Branching	✓	No
Speed Achieved without Pipelining	✓	No, 4-Level Pipeline
Automatic Status Saving During Interrupt Vector	✓	No

techniques) and no extra overhead is encountered in the ADSP-2115 for jumps, subroutines or interrupts regardless of whether they are conditional or not.

A prefetch counter (PFC) contains the address of the next instruction to be prefetched. The prefetched instruction is loaded into the instruction register (IR), unless the instruction register still contains an instruction currently executing. In this case, the prefetched instruction is temporarily stored in the queue instruction register (QIR). The instruction pipeline, in conjunction with multi-cycle instruction execution, can make program flow complex and difficult to understand. Calculating a benchmark for a particular algorithm can also become difficult for the same reason. The following code examples illustrate the counter-intuitive sequence of events due to pipeline delays and the varying number of execution cycles for different instructions.

The ADSP-2115 uses a single level of instruction pipeline where all instructions can execute in a single cycle. Therefore, none of these problems exist with the ADSP-2115.

The program counter of the TMS320C5x can supply an address for sequential addressing. The single 8-deep PC stack is used for storage of return addresses as well as for providing the ability to push and pop data for the accumulator. An interrupt flag register (IFR) is used for vectoring to an interrupt routine. Unlike the ADSP-2115, status is not automatically saved on the TMS320C50 for interrupts so that the programmer must perform any save and restore functions explicitly. Interrupt latency is 12 instruction cycles on the TM320C52 and 3 instruction cycles on the ADSP-2115. For interrupt nesting to be used in the TMS320C52, an interrupt service routine has to reenable interrupts as one of the initializing operations.

Branch instructions which contain a direct address require multiple program memory locations because both the instruction bits and the address cannot fit in the 16-bit instruction width. Delayed branches are required to minimize the overhead introduced by the instruction pipelining. Even with the use of delayed branches, as many as two cycles of overhead are required with the TMS320C50, where no overhead cycles are required with the ADSP-2115. Also, with the TMS320C50, the number of overhead cycles for a conditional branch will vary depending upon whether the condition is met or not.

6

```
PROB1   LAR     AR2,#067h   ;AR2 = 0x67.
        LACC    #064h       ;ACC = 0x64.
        SAMM    AR2         ;This update is overridden by *- updates
                            ;on the next two instructions
        LACC    *-          ;AR2 = 0x66.
        ADD     *-          ;AR2 = 0x65.

PROB2   LAR     AR2,#067h   ;AR2 = 0x67.
        LACC    #064h       ;ACC = 0x64.
        SAMM    AR2         ;LACC *- update happens before SAMM write
        LACC    *-          ;AR2 = 0x66.
        NOP                 ;AR2 = 0x64  SAMM write to AR2 happens
                            ;between instructions.
        ADD     *-          ;AR2 = 0x63.
```

TMS320C5x Program Sequencer Instructions
Arithmetic instructions cannot be conditional. Only branch instructions are conditional. Branch instructions with direct addresses require two program memory words due to the 16-bit instruction word.

```
BACC

BANZ <address>
```

There are many multiword instructions for the TMS320C50 because of the 16-bit size of the instruction word. This means that two or more fetches are required, which takes extra time. The ADSP-2115 has a 24-bit wide instruction and no multiword instructions are necessary.

PROGRAM SEQUENCER SUMMARY

Efficient looping capabilities are very important for DSP algorithms due to their repetitive nature. Also, zero-overhead jump and conditional branching is important where many decisions have to be made such as in speech processing. Table III summarizes the program sequencer capabilities of the ADSP-2115 and TMS320C50.

I/O HANDLING CAPABILITIES

A final area of efficiency is that of I/O handling. Memories, A/D and D/A converters, as well as EPROM for program booting will need to efficiently interface to the DSP processor to minimize extra logic and software overhead to drive external peripherals. The ADSP-2115 has several features relating to I/O handling which simplify DSP system design and which are not found on the TMS320C50.

Automatic Boot Loading From External Byte-Wide Memory
The ADSP-2115 directly interfaces to a single byte-wide EPROM for efficient program boot loading. No extra components are needed since the EPROM can directly connect to the address and data lines of the ADSP-2115 . A boot memory select pin (BMS) on the ADSP-2115 is tied directly to the chip select pin of the EPROM and the read line (RD) is directly connected to the output enable pin of the EPROM. The boot memory space consists of an external 64K x 8 space divided into eight separate 8K x 8 pages. At reset, boot page 0 is automatically transferred in to the internal RAM of the ADSP-2115. Under program control, any of the eight pages can be boot loaded into the internal RAM of the ADSP-2115 with access time being programmable.

Flexible Serial Ports
Both devices have two serial ports. The serial ports of the ADSP-2115 have some additional features which makes their operation more flexible. The word width of the data to be transmitted and received is programmable and can be set for any size from 3 bits to 16 bits. On the TMS320C50, the word width is limited to 8 or 16 bits.

The address generators of the ADSP-2115 can be used in conjunction with the serial ports to provide an automatic data buffering capability. Normally, an interrupt is generated after each word is transferred through the serial port. If many words are to be transferred (i.e., data buffers filled for a speech application), there can be an excess of interrupt overhead associated with the serial ports. The ADSP-2115 allows autobuffering where a length is specified along with a buffer start address and a modify value (any integer value which is used to update the address). As each word is transferred through the serial port, the data is automatically read from or written to data memory, transparent to the user, with no interrupt being generated. An interrupt is generated only when the buffer is full or empty. One of the serial ports of the ADSP-2115 also supports a multichannel word stream for easy interface to a T1 or CEPT data stream. The TM320C52 does not support a TDM (multichannel) mode of operation. The other members of the family support only 8 channels. One ADSP-2115 serial port supports multichannel transfers of either 24 or 32 channels. Serial ports on the ADSP-2115 support the G.711 recommendation for μ-law and A-law companding in hardware of data for interface to voice band codecs. Companding is an operation that is used to logarithmically compress data from 16 bits to 8 bits or expand 8-bit wide compressed data to 16 bits. Zero overhead companding of data is supported during transmit and receive. Internal companding is also supported for local compression and expansion purposes.

SUMMARY

The DSP processors available on the market today vary drastically in their ability to meet the five key requirements of DSP processing. In fact, some DSP-oriented processors, like the TMS320C50, are better high-speed microcontrollers than they are DSP processors. Analyzing the requirements of your DSP system and matching them to the capabilities of a DSP architecture will assure efficient operation. Overall the straightforward architecture and the algebraic syntax of the instruction set for the ADSP-2115 processor allows the programmer to spend more time concentrating on a complex DSP algorithm instead of spending time optimizing code for an unnecessarily complex architecture.

Due to space limits, this article does not cover many topics in detail. Consult the *ADSP-2100 Family User's Manual* and the *ADSP-2100 Family Assembler Tools Manual* for a greater depth of information on this processor.

APPENDIX: PROGRAM EXAMPLE

To illustrate some of the issues discussed above, a code example is shown below for the ADSP-2115 and the TMS320C50. To avoid long listings and confusion, a short program which performs the LMS adaption of FIR filter coefficients is shown. Both processors perform

```
        AR=DM(Error);                                   {Get Err Value From Mem }
        MY1=Beta;                                       {Load Beta Value        }
        MF=AR*MY1(RND), AY0=PM(I4,M4), MX0=DM(I0,M0);   {MF=Beta*Err, Get Ck, A }
        MR=MX0*MF(RND);                                 {MR=Beta*Error*A(n)     }

        CNTR=A;                                         {Set Loop Counter       }
        DO uloop UNTIL CE;                              {Tap Update Loop        }
           AR=MR1+AY0, AY0=PM(I4,M6), MX0=DM(I0,M1);    {AR=Ck+Beta*Error*A(n)  }
uloop:     PM(I4,M7)=AR, MR=MX0*MF(RND);                {Store CK+1, Do Next    }
        RTS;                                            {Return}
```

identical tasks so that no interpretation of the type of algorithm is required. Both code examples do not show any initialization of pointers or the set up of any modes. For simplicity, the examples only focus on the core operation.

Because these examples are short, the performance advantages of the ADSP-2115 is not as apparent as in a more sophisticated example. Nevertheless, the ease of coding and the benefits of the instruction syntax and the architecture can be seen.

ADSP-2115 Code Example Description
The example shown implements an adaptive update of FIR filter coefficients. The formula used is expressed as

`Ck+1=Ck+Beta*Error*A(n).`

The program segment shown was taken from the book *Digital Signal Processing Applications Using The ADSP-2100 Family, Volume I*, published by Prentice Hall.

The code shown uses the looping capabilities of the ADSP-2115 and can be easily expanded for a larger number of coefficients by simply changing the number of loops (the value loaded into the counter). Indirect addressing is used to address the coefficient buffer Ck and the input data buffer A(n). The address registers I0 and I4 are used for addressing of these two buffers.

The first advantage of the ADSP-2115 is its algebraic syntax for assembly language code. The routine starts with a fetch of the error term from data memory. This value is loaded into the register AR. AR is the ALU result register, but it is used as a general purpose data register in this example. The next line of code loads an immediate value, the beta value, into register MY1. MY1 is one of the input registers of the multiplier for the Y operand.

With the error value in register AR and the beta value in register MY1, a multiplication of these two values is specified. The multiplication is performed with the result rounded to the most significant 16-bits with an unbiased rounding scheme. This multifunction instruction also specifies the fetch of the coefficient , Ck, from program memory and the data value A(n) from data memory. Note that the I register specifies which address register is used as a pointer and the M register specifies how the address is modified. This ADSP-2115 addressing capability is a key advantage to that of the TMS320C50. The multiplication, the program memory fetch and the data memory fetch all occur in a single cycle. The result of the multiplication is loaded into MF, the multiplier feedback register. This value is used immediately in the next cycle where a multiplication is performed using the MX0 register (holding the A(n) term) and the MF register (holding the product beta*error). Rounding is again specified.

The counter is next loaded with the number of coefficients to be updated and a DO UNTIL instruction is specified to set up the loop logic of the ADSP-2115. The core instructions of the loop calculate the result Ck+1 and also set up the calculations for the next update. Results are written into program memory in the last instruction of the loop.

Finally, a return from subroutine instruction is specified to return control back to the calling program.

ADSP-2115 Performance Benchmark
The code section shown uses the looping capabilities of the ADSP-2115 and can be easily modified for any number of coefficients by simply changing the counter value. A total of nine instructions are used in the LMS adaption of FIR filter coefficients where each instruction executes in a single processor cycle. The two instructions in the core of the loop are repeated for each coefficient update. Therefore, the benchmark for the number of cycles required for this routine can be generally expressed as *7+n*2*, where *n* is the number of coefficients to be updated.

For a 127 TAP filter (which requires 127 coefficients), an update can be performed in 7+127*2 = 261 cycles.

TMS320C50 Code Example Description
The example shown implements an adaptive update of FIR filter coefficients. The formula used is expressed as

`a0(i+1)=a0(i)+Beta*err*X(i).`

This is the same LMS adaptive update as shown for the ADSP-2101, the equation has just been stated with different terms. The program segment shown is described in the book *TMS320C5x User's Guide* published by Texas Instruments.

This is an example of looped code based on the RTPB (repeat block) instruction. Indirect addressing is used to address the coefficient buffer a(i) and the input data buffer x(i). The auxiliary registers AR2 and AR3 are used to address these two buffers.

```
        LT      ERR                 ; T=Err
        MPY     BETA                ; P=Beta*Err(i)
        PAC                         ; errf(i)=Beta*Err(i)
        ADD     ONE, 14             ; Round The Results
        SACH    ERRF,1              ; Save errf(i)

        LACC    #126
        SAMM    BRCR                ; 127 Coeffs To Update In The Loop
        LAR     AR2, #COEFFD        ; Point To The Coefficients
        LAR     AR3, #LASTAP        ; Point To The Data Samples
        LT      ERRF
        MPY     *-,AR2              ; P=Beta*Err(i)*x(i-255)

        RPTB    LOOP-1              ; For I=0, I<=126, I++
ADAPT   ZALR    *,AR3               ; Load ACCH With Ak(i)
        MPYA    *-,AR2              ; P=Beta*Err(i)*X(i-k-1),
                                      ACC=ak(i)+Beta*err(i)*x(i-k)
        SACH    *+                  ; Store ak(i+1)

LOOP    ZALR    *,AR3               ; Final Update Last Coefficient a0(i)
        RETD                        ; Delayed Return
        APAC                        ; ACC=a0(i)+Beta*Err(i)*x(i)
        SACH    *+                  ; Save a0(i+1)
```

The LMS adaption routine starts by loading the error stored in the memory location "ERR" into the TREG0 register for multiplication. The LT instruction is used to load the T register. Once the error is loaded, then the error is multiplied by the Beta value stored in the memory location "BETA". The results (error*beta) resides in the P register of the multiplier. Because of the inflexibility of the TMS320C50 architecture, the multiplier result must be moved explicitly into the accumulator. PAC is used to place the product into the accumulator for further computation. The error*beta term can then be rounded to 16-bit precision with the instruction "ADD ONE,14" and stored into a memory location with the SACH instruction. The rounding takes an extra instruction. On the ADSP-2115, this function can be performed as part of the multiply.

At this point in the program, the loop to calculate all of the new coefficients can be set up. There are 127 coefficients in this example, so the loop counter BRCR can be initialized with the constant 126. On the ADSP-2115, the programmer loads the loop counter directly with the number of loop iterations. Two instructions are required to load the loop counter, LACC and SAMM.

Indirect accesses using the auxiliary registers AR2 and AR3 are used within the loop. These registers can be initialized with the LAR instruction prior to entering the loop.

The error*beta term can then be reloaded back into the T register for multiplication with the tapped delay line values. The "LT ERRF" instruction loads this value and the "MPY *-,AR2" performs the first multiply outside of the loop. This reloading of partial results is required because of the inflexibility of the TMS320C50 architecture.

The algorithm needs to be rearranged due to limitations of the hardware. The ADSP-2115 makes use of a more flexible bus structure where data can be fed back immediately without the need for temporary storage of intermediate results in memory.

The RTPB instruction performs the block repeat. As an argument, this instruction needs the end of loop address minus one. The three instructions ZALR, MPYA and SACH are executed in the loop 127 times. Notice that the programmer must label the instruction after the last instruction in the loop. The ADSP-2115 uses a much more understandable looping format where the last instruction in the loop is labeled. Any size loop is possible on the ADSP-2115 . The TMS320C50 block repeat is useful only for loops of three instructions or larger.

After completion of the loop, the last tap is updated and a delayed return is executed. A delayed return is necessary because of the instruction pipelining found in the TMS320C50. This type of instruction pipelining is not found in the ADSP-2115 and delayed instructions are, therefore, not necessary.

TMS320C50 Performance Benchmark

A total of 19 instructions are used in the LMS adaption of FIR filter coefficients. All instructions, however, will not execute in a single processor cycle. The three instructions in the core of the loop are repeated for each coefficient update. Therefore, the benchmark for the number of cycles required for this routine can be generally expressed as

$17+n*3$, where n is the number of coefficients to be updated.

For a 127 TAP filter (which requires 127 coefficients), an update can be performed in 17+127*3 = 398 cycles.

Table IV. ADSP-2115 vs. TMS320C50

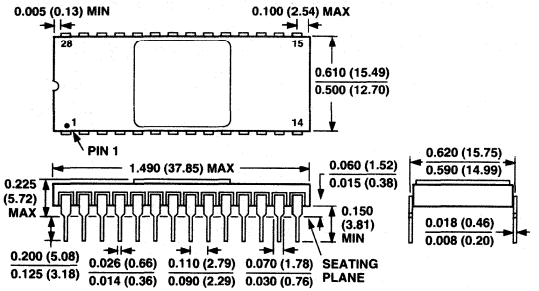
Function	2115KP-80	C52-57
Cycle Time	50 ns	35 ns
MIPS	20	28.57
Biquad IIR Filter	350 ns	350 ns
LMS Adaptive Filter Tap Update	100 ns	140 ns
1024-Point Complex FFT	1.86 ms	2.45 ms
256-Point FFT	685 µs	731 µs

Don't be fooled—you can't judge a DSP by cycle or MIPS alone! Even though the TMS320C52 has higher MIPS than the ADSP-2115, the ADSP-2115 does much better in benchmarks. Look closely at the biquad IIR filter benchmark—it takes the TMS320C52 over 28 MIPS to do what the ADSP-2115 can do with less MIPS! The ADSP-2115 executes faster because it's architecture is optimized for signal processing.

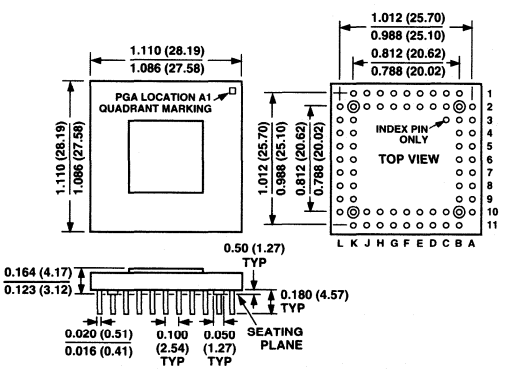
Package Information
Contents

Package Outline Dimensions

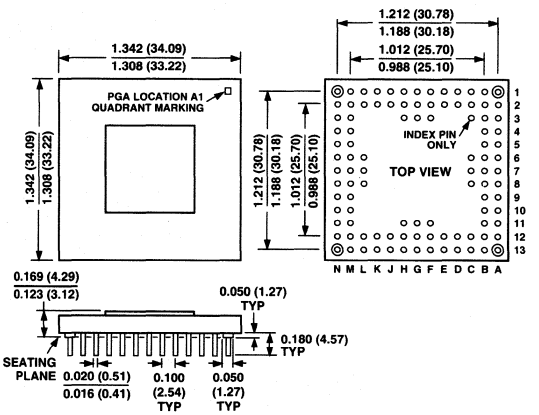
D-28
28-Lead Side Brazed DIP (Ceramic)



G-68A
68-Pin Ceramic Pin Grid Array (PGA)



G-100A
100-Pin Ceramic Pin Grid Array (PGA)



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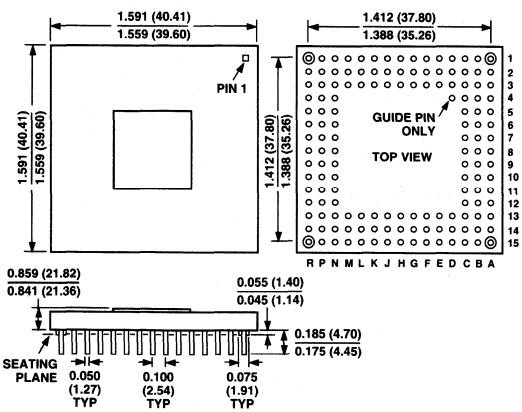
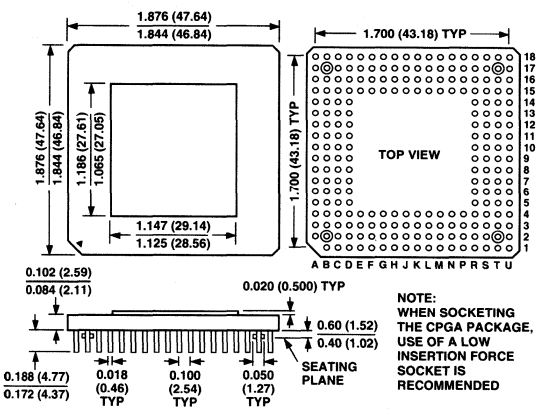
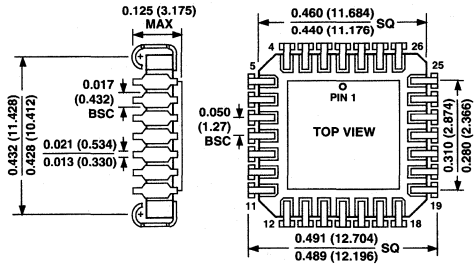


G-223
223-Pin Ceramic Pin Grid Array (PGA)

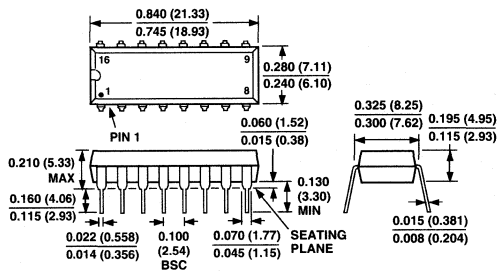


7

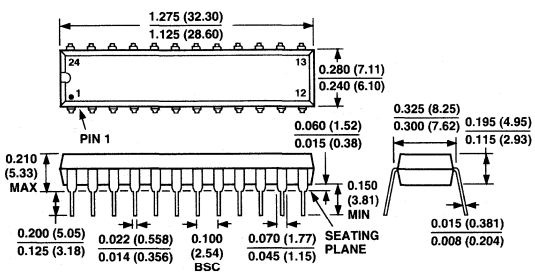
J-28
28-Lead J-Leaded Chip Carrier



N-16
16-Lead Plastic DIP (Narrow)



N-24
24-Lead Plastic Dip (Narrow)



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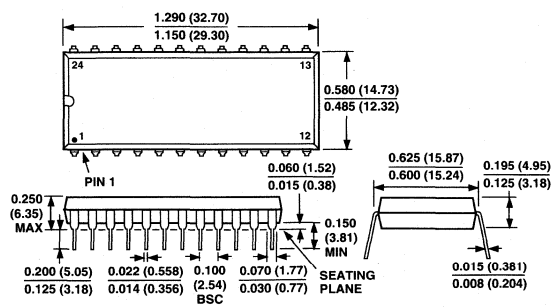
24-Lead Plastic DIP (Double Width)



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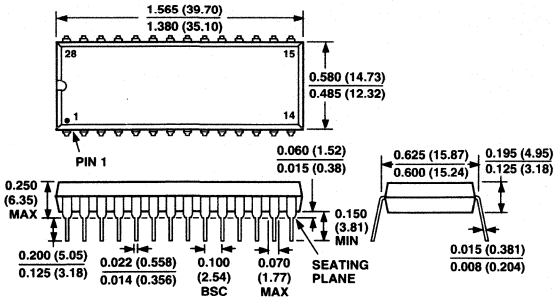

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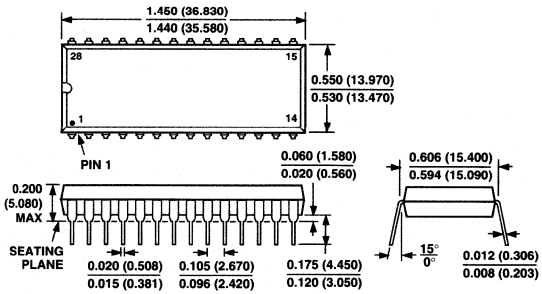
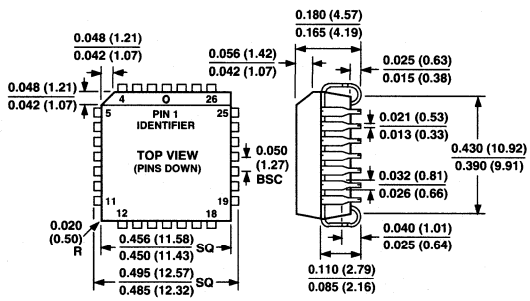
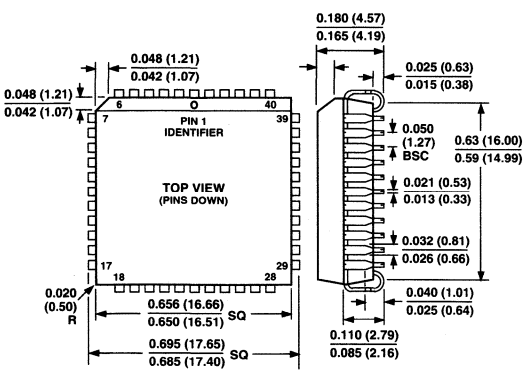


P-28A
28-Lead Plastic Leaded Chip Carrier (PLCC)



P-44A
44-Lead Plastic Leaded Chip Carrier (PLCC)



P-68A
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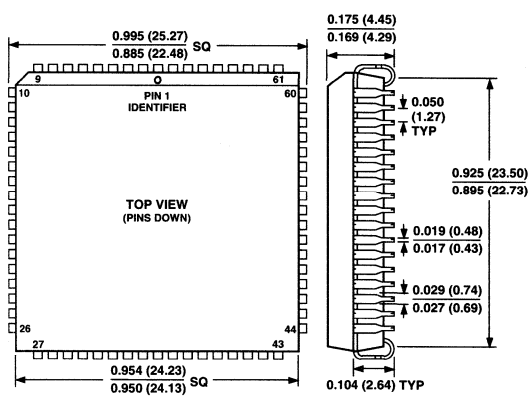
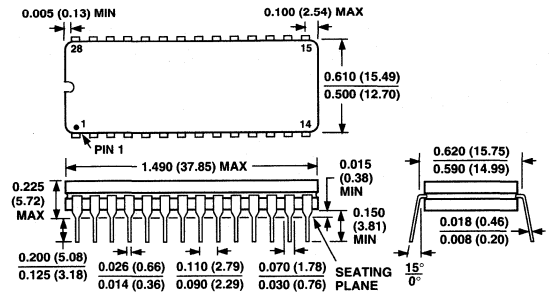
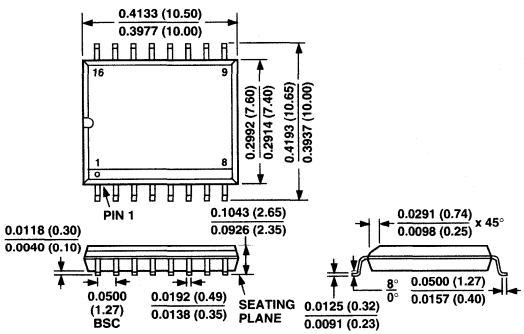


Q-28
28-Lead Cerdip



R-16
16-Lead Wide Body (SOIC)



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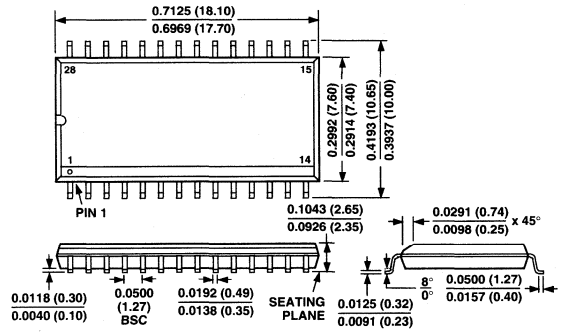
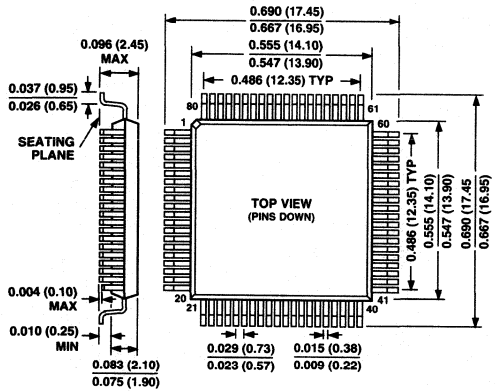
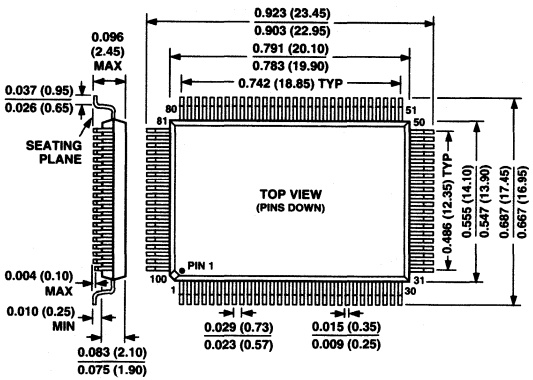


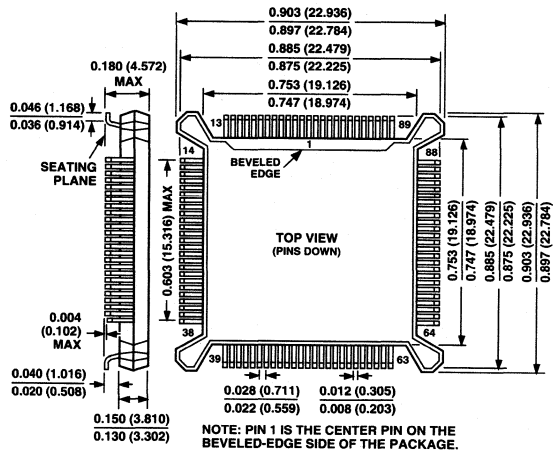
S-80
80-Terminal Plastic Quad Flatpack (PQFP)



S-100
100-Terminal Plastic Quad Flatpack (PQFP)



S-100A
100-Lead Bumpered Plastic Quad Flatpack (PQFP)



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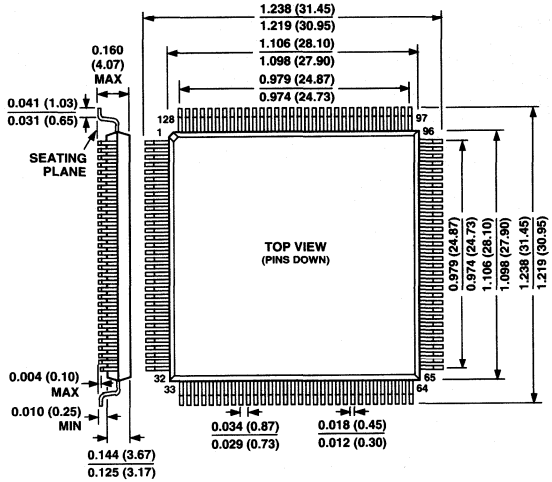
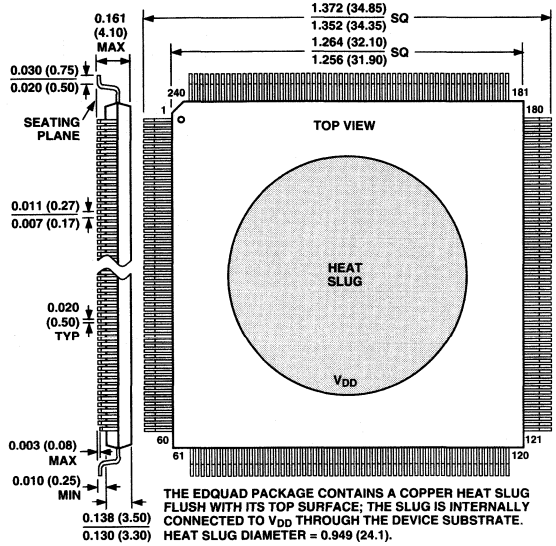
S-128
128-Terminal Plastic Quad Flatpack (PQFP)

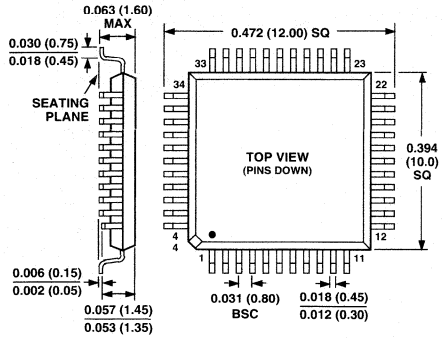


S-240
240-Terminal EDQUAD Thermally Enhanced Plastic Quad Flatpack (PQFP)

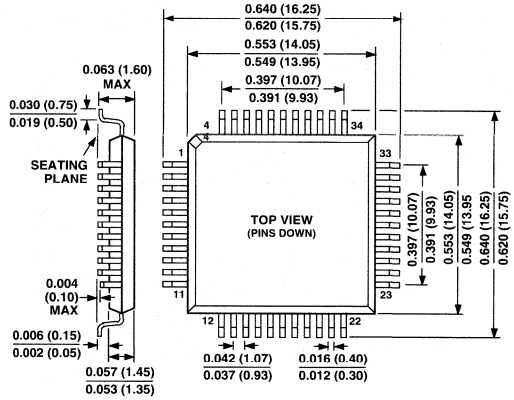


THE EDQUAD PACKAGE CONTAINS A COPPER HEAT SLUG FLUSH WITH ITS TOP SURFACE; THE SLUG IS INTERNALLY CONNECTED TO V_{DD} THROUGH THE DEVICE SUBSTRATE. HEAT SLUG DIAMETER = 0.949 (24.1).

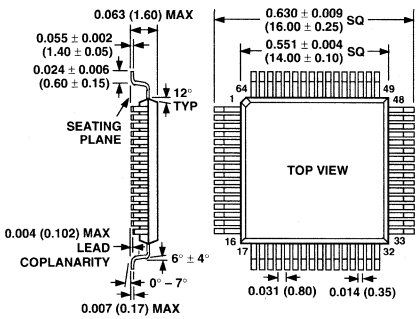
ST-44
44-Terminal Plastic Thin Quad Flatpack (TQFP)



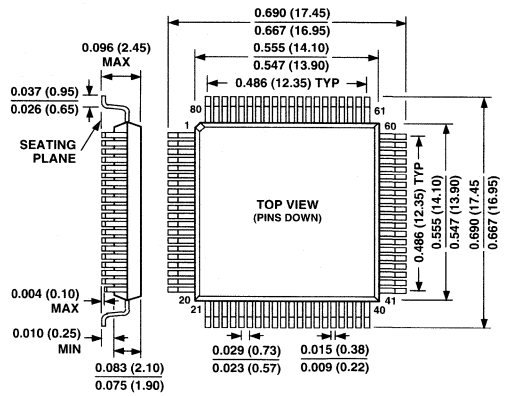
ST-44A
44-Terminal Plastic Thin Quad Flatpack (TQFP)



ST-64
64-Terminal Plastic Thin Quad Flatpack (TQFP)



ST-80
80-Terminal Plastic Thin Quad Flatpack (TQFP)



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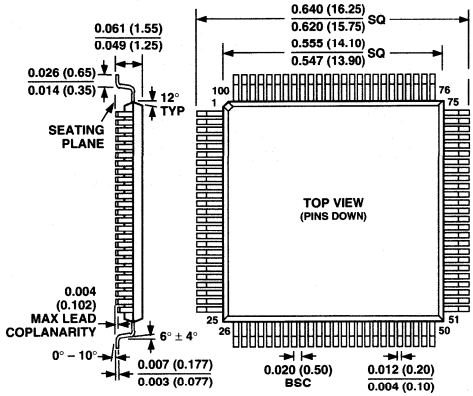
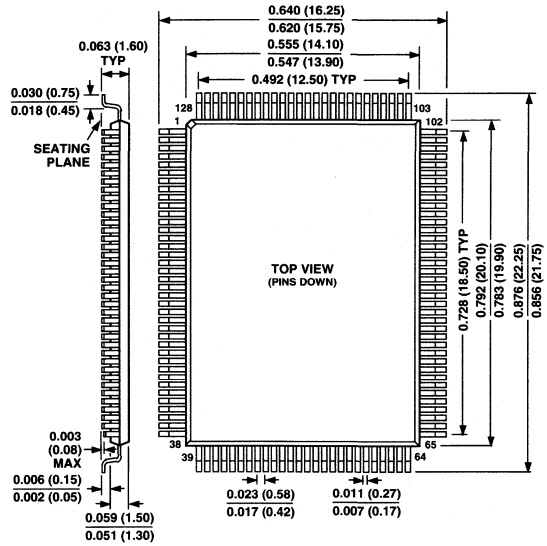
ST-100
100-Terminal Plastic Thin Quad Flatpack (TQFP)



ST-128
128-Terminal Plastic Thin Quad Flatpack (TQFP)



Appendix Contents

8

Ordering Guide

INTRODUCTION

This Ordering Guide should make it easy to order Analog Devices products. It will help you:

1. Find the correct part number for the options you want.
2. Get a price quotation and place an order with us, or one of our authorized distributors.
3. Know our warranty.

For answers to further questions, call the nearest sales office (listed on pages 8–16 and 8–17) or our main office in Norwood, Massachusetts, U.S.A. (617-329-4700).

MODEL NUMBERING

In this reference manual many of the data sheets for products having a number of standard options contain an Ordering Guide. Use it to specify the correct part number for the exact combination of options you want. This manual contains two model numbering schemes. The first model numbering scheme is used in designating DSP processors. The second conforms to the Analog Devices standard in designating computer audio components and digital audio components.

Figure 1 shows the form of model number used for our DSP processors. It consists of an "AD" (Analog Devices) prefix, a 4-to-8-digit number, an alphabetic performance/temperature-range designator and a package designator. An additional letter may immediately follow the digits ("A" for second-generation redesigned DSPs).

Figure 2 shows a different numbering scheme used for our standard computer audio components and digital audio components. It consists of an "ADSP" prefix, a 4-to-9-digit number, an alphabetic performance/temperature-range designator and a package designator.

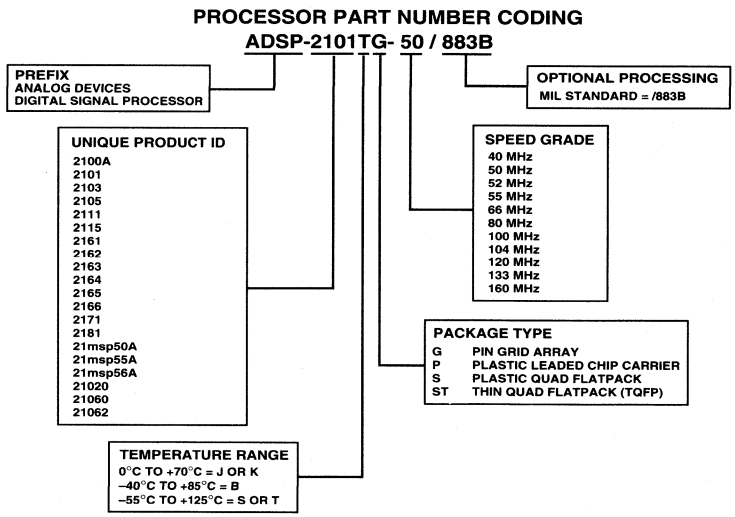


Figure 1. Model-Number Designations for DSP Processors

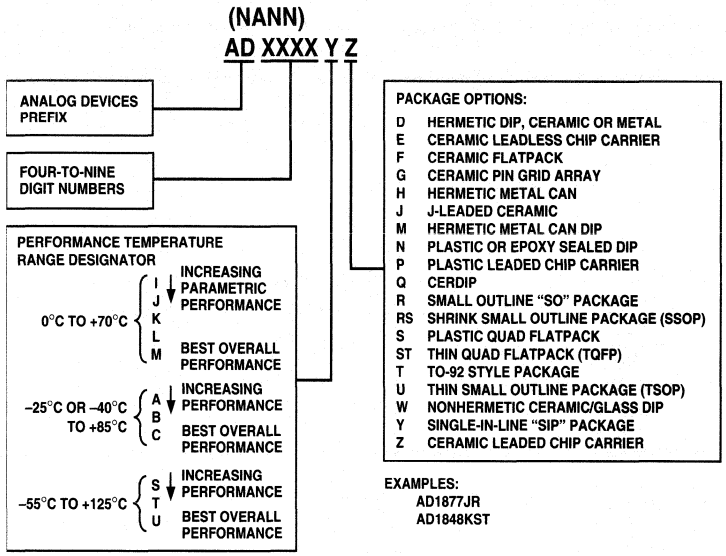


Figure 2. Model-Number Designations for Standard Analog Devices Computer Audio Components and Digital Audio Components

ORDERING FROM ANALOG DEVICES

When placing an order, please provide specific information regarding model type, number, option designations, quantity, ship-to and bill-to address. Prices quoted are list; they do not include applicable taxes, customs, or shipping charges. All shipments are F.O.B. factory.

Eligible customers may place their orders through our regional customer service centers by dialing 1-800-262-5645 (U.S.A. only) or through our representatives or authorized distributors. (The telephone numbers for our representatives or authorized distributors are listed on pages 8–16 and 8–17.) Analog Devices' minimum order value is $500.00.

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WARRANTY AND REPAIR CHARGE POLICIES

All Analog Devices, Inc., products are warranted against defects in workmanship and materials under normal use and service for one year from the date of their shipment by Analog Devices, Inc., except that components obtained from others are warranted only to the extent of the original manufacturers' warranties, if any, except for component test systems, which have a 180-day warranty. This warranty does not extend to any products which have been subjected to misuse, neglect, accident, or improper installation or application, or which have been repaired or altered by others. Analog Devices' sole liability and the Purchaser's sole remedy under this warranty is limited to repairing or replacing defective products. (The repair or replacement of defective products does not extend the warranty period. This warranty does not apply to components which are normally consumed in operation or which have a normal life inherently shorter than one year.) Analog Devices, Inc., shall not be liable for consequential damages under any circumstances.

THE FOREGOING WARRANTY AND REMEDY ARE IN LIEU OF ALL OTHER REMEDIES AND ALL OTHER WARRANTIES, WRITTEN OR ORAL, STATUTORY, EXPRESS, OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

Product Families Still Available

The information published in this Reference Manual is intended to assist the user in choosing components for the design of *new* equipment, using the most cost-effective products available from Analog Devices. The popular product types listed below may have been designed into your circuits in the past, but they are no longer likely to be the most economic choice for your new designs. Nevertheless, we recognize that it is often a wise choice to refrain from redesigning proven equipment, and we are continuing to make these products available for use in existing designs. Data sheets on these products are available upon request.

Model	Model	Model	Model	Model
AC1226	AD532	AD2700	AD7576	ADC1130
AC2626	AD533	AD2701	AD7578	ADC1131
AD2S44	AD535	AD2702	AD7579	ADC1140
AD2S47	AD545	AD2710	AD7580	ADC1143
AD2S65	AD545A	AD2712	AD7581	AD DAC08
AD2S66	AD561	AD5200 Series	AD7582	AD DAC71
AD2S75	AD562	AD5210 Series	AD7586	AD DAC72
AD2S110	AD563	AD7001	AD7590DI	ADEB770
AD203	AD567	AD7002	AD7592DI	ADG221
AD230	AD572	AD7010	AD7672	ADG222
AD231	AD578	AD7011	AD7716	ADG445
AD231A	AD579	AD7110	AD7769	ADG506A
AD232	AD582	AD7118	AD7773	ADG507A
AD232A	AD611	AD7228	AD7774	ADG526A
AD233	AD632	AD7237	AD7775	ADG527A
AD233A	AD639	AD7240	AD7820	ADG528A
AD234	AD651	AD7245	AD7848	ADG529A
AD235	AD675	AD7247	AD7850	AD OP07
AD236	AD730	AD7248	AD9003	AD OP27
AD237	AD741	AD7341	AD9003A	AD OP37
AD238	AD773	AD7371	AD9005A	ADV101
AD239	AD774	AD7501	AD9007	ADV453
AD241	AD796	AD7502	AD9014	ADV471
AD246	AD803	AD7503	AD9034	ADV473
AD346	AD805	AD7506	AD9502	ADV475
AD363	AD880	AD7507	AD9505	ADV476
AD363R	AD890	AD7510DI	AD9560	ADV477
AD364	AD891	AD7511DI	AD9610	ADV478
AD364R	AD891A	AD7512DI	AD9611	ADV7120
AD365	AD892T/E	AD7520	AD9686	ADV7121
AD380	AD896	AD7522	AD9703	ADV7122
AD386	AD897	AD7523	AD22001	ADV7128
AD389	AD899	AD7525	AD22050	ADV7141
AD390	AD1139	AD7533	AD22150	ADV7146
AD394	AD1154	AD7534	AD75019	ADV7148
AD395	AD1170	AD7535	AD75069	ADV7150
AD396	AD1315	AD7536	AD75089	ADV7151
AD503	AD1317	AD7541	AD75090	ADV7152
AD504	AD1320	AD7541A	AD79024	ADVFC32
AD506	AD1324	AD7542	AD ADC71	AMP03
AD507	AD1334	AD7543	AD ADC72	AMP05
AD507SH/883B	AD1341	AD7545	AD ADC80	BUF03
AD510	AD1362	AD7545A	AD ADC84	CAV1210
AD515	AD1376	AD7546	AD ADC85	CMP01
AD515A	AD1377	AD7548	ADC170	CMP02
AD517	AD1378	AD7549	ADC908	CMP05
AD518	AD1380	AD7572	ADC910	CMP08
AD521	AD1403	AD7572A	ADC912	CMP404
AD522	AD2026	AD7574	ADC912A	DAC01

Model	Model	Model	Model	Model
DAC02/03	OP09	PM157A	SDC1740/RDC1740	2B31
DAC05/06	OP10	PM219	SDC1741/RDC1741	2B34
DAC10	OP11	PM239	SDC1742/RDC1742	2B50
DAC20	OP12	PM248	SMP10	2B52
DAC86	OP14	PM308	SMP11	2B53
DAC88	OP15	PM355	SMP81	2B54
DAC89	OP16	PM356	SSM2013	2B55
DAC100	OP17	PM562	SSM2014	2B56
DAC210	OP20	PM725	SSM2015	2B57
DAC888	OP21	PM741	SSM2016	2B58
DAC1136	OP22	PM747	SSM2018	2B59
DAC1138	OP32	PM0820	SSM2044	2S50
DAC1146	OP41	PM0828	SSM2045	2S80A
DAC1408A	OP43	PM1008	SSM2047	2S81A
DAC1508A	OP44	PM1012	SSM2100	2S82A
DAC8012	OP50	PM2108	SSM2110	3B Series
DAC8143	OP61	PM4136	SSM2120	4B Series
DAC8212	OP64	PM6012	SSM2122	5B Series
DAC8841	OP65	PM7224	SSM2125	6B Series
DAS1152	OP80	PM7226	SSM2126	7B Series
DAS1153	OP111	PM7226A	SSM2131	277
DAS1158	OP147	PM7524	SSM2132	281
DAS1159	OP150	PM7528	SSM2134	284J
DRC1745	OP160	PM7533	SSM2139	286J
DRC1746	OP166	PM7541	SSM2210	289
HDS1240E	OP207	PM7541A	SSM2220	290
HDS1250A	OP215	PM7542	SSM2300	290A
HOS050/050A/050C	OP227	PM7543	SW01/02	292
HOS060/060A	OP260	PM7545	SW201	292A
HTC0300A	OP421	PM7548	SW202	310
HTS0010	OSC1758	PM7574	SW7510/7511	365
HTS0025	PKD01	PM7628	1B21	429
IPA1764	PM108/208/308	PM7645	1B22	451
JM38510/11301/11302	PM111/211	REF03	1B31	453
LIU01	PM119	REF05	1B32	460
MUX88	PM139	REF08	1B41	741A
OP01	PM148/248	REF10	1B51	755
OP02	PM155	RPT82	1S74	757
OP04	PM155A	RPT83	2B20	759
OP05	PM156	RPT85	2B22	950
OP08	PM156A	RPT86	2B23	
OP08	PM157	RPT87	2B24	

Substitution Guide

The products listed in the left-hand column are no longer available from Analog Devices. In many cases, comparable functions and performance may be obtained with newer models, but—as a rule—they are not directly interchangeable. The closest recommended Analog Devices equivalent, physically and electrically, is listed in the right-hand column. If no equivalent is listed, or for further information, contact your local sales office.

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
AD2S34	None	AD1147/48	AD669	AD7527	AD7548
AD2S46	None	AD1175	RTI870	AD7530	AD7533
AD101A	PM1008	AD1321	AD1324	AD7531	AD7541A
AD108/208/308	AD705	AD1322	AD1324	AD7544	AD7548
AD108A/208A/308A	AD705	AD1332	None	AD7550	Consult ADI
AD111/211/311	AD790	AD1408	AD558	AD7552	Consult ADI
AD201A	PM2008	AD1508	AD558	AD7555	Consult ADI
AD206	None	AD1678	AD678	AD7560	None
AD293	AD210	AD1679	AD679	AD7570	AD7579/AD7580
AD294	AD210	AD1779	AD779	AD7571	AD7579/AD7580
AD295	AD210	AD1885	None	AD7583	AD7880+MUX
AD301A	PM3008	AD2002	None	AD7772	Consult ADI
AD345	AD1324	AD2003	None	AD9005	AD9005B
AD351	AD790	AD2004	None	AD9006	None
AD362	AD1362	AD2006	None	AD9011	AD9002
AD367	None	AD2008	None	AD9016	None
AD368	None	AD2009	None	AD9020SE/883B	AD9020SZ/883B
AD369	None	AD2010	None	AD9020TE/883B	AD9020TZ/883B
AD370/371	AD767	AD2016	None	AD9028	None
AD376	AD1376	AD2020	None	AD9038	None
AD381	AD744	AD2021	None	AD9040	AD9040A
AD382	AD744/AD845	AD2022	None	AD9060SE/883B	AD9060SZ/883B
AD392	AD664	AD2023	None	AD9060TE/883B	AD9060TZ/883B
AD395/883B	AD394/883B	AD2024	None	AD9300TE/883B	AD9300TQ/883B
AD501	AD711	AD2025	None	AD9521	AD640
AD502	AD711	AD2027	None	AD9615	AD9611/AD9617
AD505	AD843	AD2028	None	AD9630AQ	AD9630AN
AD506SH/883B	AD42626	AD2033	None	AD9630SQ/883B	AD9630AN
AD508	AD517	AD2036	None	AD9685	AD96685
AD509	AD843	AD2037	None	AD9687	AD96687
AD511	AD711	AD2038	None	AD9688	AD9002
AD512	AD711	AD2040	None	AD9712	AD9712B
AD513	AD711	AD2050	None	AD9713	AD9713B
AD514	AD711	AD2051	None	AD9768JQ	AD9768JD
AD516	AD711	AD2060	None	AD9768SQ	AD9768SD
AD520	AD524	AD2061	None	AD9768SE	AD9768SD
AD523	AD549	AD2070	None	AD9950	AD9955
AD528	AD711/744	AD2071	None	AD75062	None
AD530	AD533	AD3554	None	AD75068	None
AD531	AD532	AD3860	AD567	AD ADC816	AD7820/AD7821
AD540	AD544	AD5010/6020	AD9000	ADC8S	AD673
AD559	AD557/AD558	AD5201	AD578	ADC10Z	AD574A
AD565	AD565A	AD5202	AD5212	ADC12QL	AD7578
AD566	AD566A	AD5204	AD5214	ADC12QM	None
AD575	AD573	AD5205	AD5215	ADC12QZ	AD574A
AD583	AD585	AD5211	AD578	ADC14I/17I	AD1170
AD612	AD524	AD5240	AD ADC85	ADC16Q	None
AD614	AD524	AD6012	AD565A	ADC1100	AD1170
AD674A	AD674B	AD7005	AD7011/AD7013	ADC1102	AD7870
AD682	AD781	AD7115	AD7111	ADC1103	AD7572A
AD689	AD587	AD7513	ADG201A	ADC1105	Consult ADI
AD770	Consult ADI	AD7516	AD7510DI	ADC1109	AD7572A
AD801	AD711	AD7519	None	ADC1111	AD574A
AD1145	AD7846	AD7521	AD7541A	ADC1121	AD7880

Model	Closest Recommended Equivalent
ADC1123	AD7880
ADC1133	AD574A
ADCQM	None
ADCQU	AD574A
AD DAC100	AD561
ADG200	None
ADG201	ADG201A
ADLH0032	None
ADLH0033	None
ADLH0032G/CG	AD843
ADLH0033G/CG	AD9620/AD9630
ADM501	None
ADP501	None
ADREF01	REF01
ADREF02	REF02
ADSHC85	AD585
ADSHM5	HTC0300A
ADSP-1008A	None
ADSP-1009A	None
ADSP-1010A	None
ADSP-1010B	None
ADSP-1012A	None
ADSP-1016A	None
ADSP-1024A	None
ADSP-1080A	None
ADSP-1081A	None
ADSP-1101	None
ADSP-1110A	None
ADSP-1401	None
ADSP-1402	None
ADSP-1410	None
ADSP-3128A	None
ADSP-3201	None
ADSP-3202	None
ADSP-3210	None
ADSP-3211	None
ADSP-3212	None
ADSP-3220	None
ADSP-3221	None
ADSP-3222	None
AMP01BX	AMP01AX
AMP01BX/883C	AMP01AX/883C
AMP05BX	AMP05AX
AMP05BX/883C	AMP05Z/883C
API1620/1718	Consult ADI
BDM1615/16/17	None
BUF03BJ/883C	BUF03AJ/883C
CAV0920/1020	AD9020/9060
CAV1202	AD9007
CAV1205	AD9007
CMP01Z	CMP01J
CMP05BJ	CMP05CJ
CMP05BZ	CMP05CZ
CMP05GJ	CMP05CJ
CMP404BY	CMP404AY
CMP404BY/883C	CMP404AY/883C
DAC02ACX1	DAC02CCX1
DAC05AX1	DAC02CCX1
DAC05EX1	DAC02CCX1
DAC10BX	DAC10FX
DAC10CX	DAC10GX
DAC10DF	AD568
DAC10H	None
DAC10Z	None
DAC12QS	AD667
DAC12QZ	AD667
DAC12M	AD7845
DAC14QM	AD1139
DAC16QM	AD1139
DAC100AAQ7	DAC100ACQ7
DAC100AAQ8	DAC100ACQ8
DAC100ABQ7	DAC100ACQ7
DAC100ABQ8	DAC100ACQ8
DAC100BBQ5/883C	DAC100ACQ5/883C
DAC100BCQ7	DAC100BBQ7
DAC100DDQ7	DAC100CCQ7
DAC312BR	DAC312ER
DAC888AX	DAC888EX
DAC888BX	DAC888EX
DAC1009	AD767
DAC1106	AD568
DAC1108	AD568
DAC1112	AD667
DAC1117	None
DAC1118	AD767
DAC1122	AD7541A
DAC1125	AD7533
DAC1132	AD667
DAC1137	None
DAC1408-6P	DAC1408-8P
DAC1408-7P	DAC1408-8P
DAC1408-7Q	DAC1408-8Q
DAC1408-GQ	DAC1408-8Q
DAC1420	None
DAC1422	None
DAC1423	None
DAC1508A-8Q	DAC1408-8Q
DAS09	AD8401
DAS1128	AD1341
DAS1150	None
DAS1151	None
DAS1155	None
DAS1156	None
DAS1157	DAS1158
DRC1605/06/07	Consult ADI
DRC1705/1706	Consult ADI
DRC1765/66	AD2S65/66
DSC1605/06/07	Consult ADI
DSC1705/1706	Consult ADI
DSC1765/66	None
DTM1716/17	None
HAS0802	HAS1202A
HAS1002	HAS1202A
HAS1202	HAS1202A
HDD1015	AD9712B
HDD1409	None
HDG Series	AD9701
HDG0805	AD9701
HDH0802	AD9713B
HDH1003	AD9713B
HDH1205	AD9713B
HDL3805	ADV453/ADV478
HDL3806	ADV453/ADV478
HDM1210	AD668/AD9713B
HDS0810E	AD9712B
HDS0820	AD9713B
HDS1015E	AD9712B
HDS1025	AD9713B
HDS1250	HDS1250A
HOS100AH/SH	None
HOS200	AD9620/30
HTC0300	HTC0300A
HTC0500	HTC0300A
IPA1751	IPA1764
IRDC1730/31/33	AD2S80A/82A
IVS100	None
MAH0801	AD9005B
MAH1001	AD9005B
MAS0801	AD9005B
MAS1001	AD9005B
MAS1202	AD9005B
MAT01/883C	MAT01AH/883C
MAT02BH	MAT02AH
MAT02BH/883C	MAT02AH/883C
MATV0811	AD9012/48
MATV0816	AD9012/48
MATV0820	AD9012/48
MCI1794	AD2S80A/82A
MDA Family	AD9712B/13B
MDD Series	AD9713B
MDH Family	AD9712B/13B
MDMS Family	AD9712B/13B
MDS Family	AD9712B/13B
MDSL Family	AD9712B/13B
MOD1005/20	AD9020/60
MOD1205	AD9005B
MUX08AQ	MUX08BQ
MUX24AQ	MUX24EQ
MUX24BQ	MUX24FQ
MUX16AT	MUX16ET
MUX16BT	MUX16FT
MUX200	None
OP01HJ	OP01J
OP01HZ	OP01HP
OP02BJ	OP02AJ
OP02BJ/883C	OP02AJ/883C
OP02EJ	OP07DJ
OP02EP	OP177GP
OP02EZ	OP177GZ
OP02J	OP02AJ
OP02/883C	OP02AZ/883C
OP04DY	OP04CY
OP04GBC	OP04NBC

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
OP04Y/883C	OP04AY/883C	RTI1243	None	2S58	Consult ADI
OP05Z	OP05AZ	RTI1250	None	5S70/5S72	AD2S75
OP05/883C	OP05AZ/883C	RTI1251	None	9S70/71/72	None
OP06BJ/883C	OP06AJ/883C	RTI1252	None	9S75/76/79	None
OP06EZ	OP06GZ	RTI1270	None	40	AD711
OP06FZ	OP06GZ	RTM Series	Consult ADI	41	AD515A
OP08AJ	PM1008AJ	SAC1763	None	42	AD549
OP08AJ/883C	PM1008AJ/883C	SBCD1752/53/		43	AD549
OP08AZ/883C	PM1008AZ/883C	56/57	None	44	AD845
OP08CZ/883C	PM1008AZ/883C	SCDX1623	None	45	AD744
OP08EJ	PM1008EJ	SCM1677	None	46	AD844
OP08EZ	PM1008EZ	SDC1602/3/4	Consult ADI	47	AD845
OP09ARC/883C	OP11ARC/883C	SDC1700	Consult ADI	48	AD845
OP09FY	OP09EY	SDC1702	Consult ADI	50	AD844
OP12BZ	OP12AZ	SDC1703	Consult ADI	51	AD844
OP12CZ	OP12AZ	SDC1704	Consult ADI	52	AD707
OP12GZ	OP12FZ	SDC1711	None	102	AD845
OP14DZ	OP14CZ	SDC1721	None	106	AD711
OP14GRBC	OP14GBC	SDC1725	Consult ADI	107	AD711
OP14J/883C	OP14AJ/883C	SDC1726	Consult ADI	108	AD845
OP15BJ	OP15AJ	SDC1728	Consult ADI	110	AD845
OP15BZ	OP15AZ	SDC1767	Consult ADI	118	AD711
OP16BJ	OP16AJ	SDC1768	Consult ADI	120	AD844
OP17BZ/883C	OP17AZ/883C	SERDEX	None	141	AD711
OP17CJ	OP17AJ	SHA1A	AD585	142	AD845
OP17FJ	OP17EJ	SHA2A	AD781	143	AD845
OP17FZ	OP17EZ	SHA3	AD585	146	AD382
OP20CJ	OP20BJ	SHA4	AD585	148	AD549
OP21GRBC	OP21GBC	SHA5	None	149	AD844
OP215BJ	OP215AJ	SHA6	None	153	AD517
OP215BJ/883C	OP215AJ/883C	SHA1114	AD585	161	None
OP215BZ	OP215AZ	SHA1134	None	163	None
OP215CZ/883C	OP215BZ/883	SHA1144	None	165	None
OP21BJ	OP21AJ	SHC85	AD585	170	None
OP21BZ	OP21AZ	SHM5/SHM5K	None	171	None
OP21EJ	OP21AJ	SMP10BY	SMP10AY	180	AD OP07
OP220BJ	OP220AJ	SMP10BY/	SMP10AY/	183	AD707
OP22AJ	OP22AJ/883C	883C	883C	184	AD707
OP22EJ	OP22AJ/883C	SPA1695	None	220	None
OP32BZ	OP32AZ	SSCT1621	AD2S80A/82A	230	None
QMX01	None	SSCT1622/23	None	231	None
RDC1725	Consult ADI	STB03	None	232	None
RDC1726	Consult ADI	STM Series	Consult ADI	233	None
RDC1728	Consult ADI	SW01BQ	SW01FQ	234	None
RDC1767	Consult ADI	SW7510AQ	SW7510EQ	235	None
RDC1768	Consult ADI	SW7510BQ	SW7510FQ	260	AD707
RSCT1621	AD2S80A/82A	SW7511AQ	SW1577BQ	261	OP177
RTI870	None	THC Family	HTC0300A	272	None
RTI980	None	THS Family	HTC0300A	273	None
RTI1200	RTI711 Series	TSL1612	Consult ADI	274J	284J
RTI1201	RTI711 Series	1S10/20	AD2S80A/82A	275	AD210
RTI1202	RTI711 Series	1S14/24/44/64/74	AD2S83	276	None
RTI1230	None	1S60/61	AD2S80A/82A	279	286J
RTI1231	None	2B30	2B31	280	281
RTI1232	None	2B35	None	282J	292A
RTI1240	None	2S20	AD2S80A/82A	283J	292A
RTI1241	None	2S54	Consult ADI	285	Consult ADI
RTI1242	None	2S56	Consult ADI	287	None

Model	Closest Recommended Equivalent	Model	Closest Recommended Equivalent
288	AD210	953	966
293	AD210	956	None
294	AD210	959	960
301	310 (Module)	964	None
302	310 (Module)	965	940
311	AD549	967	None
350	None	968	945
422	None	971	None
424	AD534	972	None
425	AD534	973	975
426	AD534	974	None
427	None	977E	977
428	AD538		
432	None		
433	AD534		
434	AD534		
435	AD734		
436	AD734		
440	None		
441	None		
442	None		
450	AD652		
452	None		
454	AD537		
456	AD537		
458	460		
602J10	AD524		
602J100	AD524		
602K100	AD524		
603	AD524		
605	AD524		
606	AD625		
610	AD625		
751	None		
752	759		
756	None		
901	9022		
903	905		
904	9022		
906	905		
907	None		
908	None		
909	None		
915	9022		
921	None		
926	None		
927	None		
928	922		
931	None		
932	None		
933	None		
935	None		
942	None		
944	None		
946	None		
947	Consult ADI		
948	Consult ADI		
951	None		
952	970		

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MILITARY/AEROSPACE REFERENCE MANUAL—1994. Information and data on products available with processing in accordance with MIL-STD-883. Data sheets and selection guides on Operational Amplifiers, A/D and D/A Converters, Digital Signal Processing, Instrumentation Amps, Multipliers/Dividers, V/F & F/V Converters, Switches & Multiplexers, Sample/Track-Hold Amplifiers, Voltage References and Special Function Components.

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Personal Sound Architecture. An 8-page brochure describing a programmable architecture for integrating sound into personal computers using software-based technologies and IC chipsets (including Analog Devices DSPs, codecs, and other peripherals) for sound cards.

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AMPLIFIER APPLICATIONS GUIDE, by the Applications Engineering Staff of Analog Devices and edited by Walt Kester, published by Analog Devices (1992). 648 pages of timely and practical information on amplifiers—including operational, audio, instrumentation, video, and log amps. Topics include: Introduction; Precision transducer interfaces; High impedance, low current; Single-supply, low-power; Audio; Filtering, Driving ADCs; Video and other high-speed applications; Nonlinear circuit applications; Unusual applications; Subtleties; Hardware techniques; Simulation; and a complete Index. $20.00

ANALOG-DIGITAL CONVERSION HANDBOOK: Third Edition, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Englewood Cliffs, NJ: Prentice Hall (1986). A comprehensive guide to A/D and D/A converters and their applications. This third edition of our classic is in hardcover and has more than 700 pages, an Index, a Bibliography, and much new material, including: video-speed, synchro-resolver, V/F, high-resolution, and logarithmic converters, ICs for DSP, and a "Guide for the Troubled." Seven of its 22 chapters are totally new. $32.95

DIGITAL SIGNAL-PROCESSING APPLICATIONS USING THE ADSP-2100 FAMILY, Vol. I, by the Applications Staff of Analog Devices, DSP Division; edited by Amy Mar (628 pages). Englewood Cliffs, NJ: Prentice Hall (1990). Bridge the gap between DSP algorithms and their real-world implementation on state-of-the-art signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips. Comprehensive source-code listings are complete with comments and accompanied by explanatory text. Programs are listed on a pair of supplementary diskettes—furnished with the book. Application areas include fixed- and floating-point arithmetic, function approximation, digital filters, one- and two-dimensional FFTs, image processing, graphics, LP speech coding, PCM, ADPCM, high-speed modem algorithms, DTMF coding, sonar beam-forming. Additional topics include memory interface, multiprocessing, and host interface. The book can serve as a companion to *Digital Signal Processing in VLSI.* **Now in paperback;** its price includes a diskette. $30.00

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DIGITAL SIGNAL. PROCESSING IN VLSI, by Richard J. Higgins. Englewood Cliffs, NJ: Prentice Hall (1990). An introductory 614-page guide for the engineer and scientist who needs to understand and use DSP algorithms and special-purpose DSP hardware ICs—and the software tools developed to carry them out efficiently. Real-World Signal Processing; Sampled Signals and Systems; The DFT and the FFT Algorithm; Digital Filters; The Bridge to VLSI; Real DSP Hardware; Software Development for the DSP System; DSP Applications; plus Bibliography and Index. $38.00

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NONLINEAR CIRCUITS HANDBOOK: Designing with Analog Function Modules and ICs, by the Engineering Staff of Analog Devices, edited by Daniel H. Sheingold. Norwood, MA: Analog Devices, Inc. (1974). A 540-page guide to multiplying and dividing, squaring and rooting, rms-to-dc conversion, and multifunction devices. Principles, circuitry, performance, specifications, testing, and application of these devices—contains 325 illustrations. $5.95

TRANSDUCER INTERFACING HANDBOOK: A Guide to Analog Signal Conditioning, edited by Daniel H. Sheingold. Norwood, MA: Analog Devices, Inc. (1980). A book for the electronic engineer who must interface transducers for temperature, pressure, force, level, or flow to electronics, these 260 pages tell how transducers work—as circuit elements—and how to connect them to electronic circuits for effective processing of their signals. $14.50

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Product Index

Alphanumeric by Model Number

**A = Amplifier Reference Manual; C I = Data Converter Reference Manual, Volume I; C II = Data Converter Reference Manual, Volume II; D = Data Sheet; DI = Design-In Reference Manual; DM = DSP/MSP Products Reference Manual; SL = Special Linear Reference Manual.*

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